PICMG® COM.0

COM Express® Module Base Specification

Revision 3.0
March 31, 2017

Open Modular
Computing Specifications

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Revision History

Revision	Date	Action
1.0	July 10, 2005	Revision 1 0
2.0	August 8, 2010	
2.1	May 14, 2012	
3.0	March 31, 2017	See overview in Section 1.2 'COM.0 R3.0 Changes from R2.1' on page 3

1 Introduction

A Computer-On-Module, or COM, is a Module with all components necessary for a bootable host computer, packaged as a super component. A COM requires a Carrier Board to bring out I/O and to power up. COMs are used to build computer solutions and offer OEMs fast time-to-market with reduced development cost. Like integrated circuits, they provide OEMs with significant freedom in meeting form-fit-function requirements. For all these reasons the COM methodology has gained much popularity with OEMs in the embedded industry.

COM Express® is an open industry standard for Computer-On-Modules. It is designed to be future proof and to provide a smooth transition path as technology advances.

Key features include:

- Rich complement of contemporary high bandwidth serial interfaces, including PCI Express, Serial ATA, USB, and Gigabit & 10Gb Ethernet
- Extended power-management capabilities
- Robust thermal and mechanical concept
- Cost-effective design
- Legacy-free design (no Super I/O, PS2 keyboard or mouse)
- Small Module size with multiple footprint options to satisfy a range of performance requirements
- High-performance mezzanine connector with several pin-out types to satisfy a range of applications
- Extensive video port support, including VGA, LVDS, DP, eDP, DVI and HDMI terminal drivers plus x16 PEG port to Carrier Board graphics controller

The COM Express® specification has been created to appeal to a range of vertical embedded markets. It has also been formulated to be applicable to a broad range of form factors, from floor-installed to bench-top to handheld. Markets and applications include but are not limited to:

- Healthcare - clinical diagnostic imaging systems, patient bedside monitors, etc.
- Retail & advertising - electronic shopping carts, billboards, kiosks, POS systems, etc.
- Test & measurement - scientific and industrial test and measurement instruments
- Gaming & entertainment - simulators, slot machines, etc.
- Industrial automation - industrial robots, vision systems, etc.
- Security - digital Closed Circuit Television, luggage scanners, intrusion detectors, etc.
- Defense & government - unmanned vehicles, rugged laptops, wearable computers, etc.

Systems based on the COM Express® Specification require the implementation of an application-specific Carrier Board that accepts the Module. User-specific features such as external connector choices and locations and peripheral circuits can be tailored to suit the application. The OEM can focus on application-specific features rather than CPU board design. The OEM also benefits from a wide choice of Modules providing a scalable range of price and performance upgrade options.

1.1 Objective

This specification defines COM Express® Modules at a level of detail sufficient to allow interoperability between independent vendors' Modules and Carrier Boards.

1.2 COM.0 R3.0 Changes from R2.1

Removed legacy Type 1, Type 2, Type 3, Type 4, and Type 5 text. Designs should focus on Types 6, 7 and 10.

Type 6

- Removed SDVO support
- Removed ExpressCard support
- Removed AC´97
- Added support for IEEE1588
- Added Host/Client support on USB0
- Added Rapid Shutdown support
- Added eSPI interface multiplexed over LPC

Type 10

- Removed SDVO support
- Removed ExpressCard support
- Removed AC´97
- Added support for IEEE1588
- Added eSPI interface multiplexed over LPC
- Added Host/Client support on USB0

Type 7

A new module Type was created to support high bandwidth networking.

Following is a list of differences when comparing to an R2.1 Type 6.

- Removed LVDS, DDI, and VGA graphics interfaces
- Removed audio support
- Removed ExpressCard support
- Reduced the number of SATA channels from 4 to 2 to gain 2 additional PCIe lanes
- Reduced the number of USB 2.0 ports from 8 to 4 to gain 4 additional PCIe lanes
  Note that all 4 USB ports support USB 3.0
- Added 8 PCIe lanes for a total of up to 32
- Added four 10GbE interfaces with Phy sideband signals to support optical and copper Phys
- Added NC-SI interface
- Added support for IEEE1588
- Added Rapid Shutdown support
- Added eSPI interface multiplexed over LPC
- Added Host/Client support on USB0

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1.4.1 Necessary Claims (referring to mandatory or recommended features)

Tyco Electronics has the following patents, which may cover some aspects of the PICMG® COM Express® Module and Carrier Board Connector as detailed in Section 6. Contact Tyco Electronics for further information.

- USA patent 6,095,832 “Cap housing for electrical connectors”
- USA patent 6,159,021 “Electrical connector for printed circuit boards”
- USA patent 6,558,195 “Electrical connector for printed circuit boards”
- Japan patent 11-040243 “ELECTRICAL CONNECTOR CAP AND ELECTRICAL CONNECTOR ASSEMBLY”
- Japan patent 11-074027 “BOARD-MOUNTING TYPE CONNECTOR”
- Japan patent 11-260464 “CAP ON ELECTRIC CONNECTOR”
- Japan patent 11-354227 “BASE BOARD INSTALLING TYPE CONNECTOR ASSEMBLY”
- Japan patent 2000-003751 “SUBSTRATE MOUNTING TYPE CONNECTOR ASSEMBLY”
- Japan patent 2000-048876 “ELECTRICAL CONNECTOR FOR CONNECTING MUTUAL BOARDS”

Foxconn Electronics (Hon Hai Precision) has the following patents, which may cover some aspects of the PICMG® COM Express® Module and Carrier Board Connector as detailed in Section 6. Contact Foxconn Electronics for further information.

- USA patent 7,578,701 “Electrical connector for PCB”
- China patent 200720131412.4 “Electrical Connector for PCB”
- Taiwan patent M339102 “Electrical Connector for PCB”

1.4.2 Unnecessary Claims (referring to optional features or non-normative elements)

No disclosures in this category were made during subcommittee review.

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1.6 Acronyms / Definitions

Table 1.1: Terms and Definitions

Term	Definition
10GBASE-KR	10 Gbit internal copper interface. Operates over a single lane and uses the same physical layer coding (defined in IEEE 802.3 Clause 49) as 10GBASE-LR (Single Mode Fiber 1310 nm) /ER (Single Mode Fiber 1550 nm) /SR (Multi Mode Fiber 850 nm)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
Basic Module	COM Express® 125mm x 95mm Module form factor.
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
BMC	Baseboard Management Controller
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer.
Carrier Board	An application specific circuit board that accepts a COM Express® Module.
Compact Module	COM Express® 95x95 Module form factor
CVBS	Composite Video Baseband Signal
DDC	Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor
DDI	Digital Display Interface – containing DisplayPort and HDMI/DVI
DIMM	Dual In-line Memory Module
DisplayPort **DP**	DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA). It defines a new license free, royalty free, digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use TMDS.
EAPI	Embedded Application Programming Interface Software interface for COM Express® specific industrial functions • System information • Watchdog timer • I2C Bus • Flat Panel brightness control • User storage area • GPIO
eDP	Embedded DisplayPort
EEPROM	Electrically Erasable Programmable Read-Only Memory
Embedded DisplayPort **eDP**	Embedded Display Port (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video.
eSPI	Enhanced Serial Peripheral Interface
Extended Module	COM Express® 155mm x 110mm Module form factor.
FR4	A type of fiber-glass laminate commonly used for printed circuit boards.
Gb	Gigabit
GbE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output

Term	Definition
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio.
HDMI	High Definition Multimedia Interface
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
LAN	Local Area Network
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice. Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device.
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LS	Least Significant
LVDS	Low Voltage Differential Signaling – widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications.
MAFS	Term for Master Attached Flash Sharing where the Flash component is attached to the processor interface.
MDIO	Management Data Input/Output, or MDIO, is a 2-wire serial bus that is used to manage PHYs or physical layer devices in media access controllers (MACs).
ME	Management Engine
Mini Module	COM Express® 84x55mm Module form factor
MS	Most Significant
NA	Not Available
NC	No Connect
NC-SI	Network Controller Sideband Interface
OEM	Original Equipment Manufacturer
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PCI Express **PCIE**	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
PHY	Ethernet controller physical layer device
Pin-out Type	A reference to one of eight COM Express® definitions for the signals that appear on the COM Express® Module connector pins.
R_a	Roughness Average – a measure of surface roughness, expressed in units of length.
ROM	Read Only Memory – a legacy term – often the device referred to as a ROM can actually be written to, in a special mode. Such writable ROMs are sometimes called Flash ROMs. BIOS is stored in ROM or Flash ROM.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
S0, S1, S2, S3, S4, S5	System states describing the power and activity level S0 — Full power, all devices powered S1 — CPU powered. CPU and bus clocks off S2 S3 Suspend to RAM — System context stored in RAM; RAM is in standby S4 Suspend to Disk — System context stored on disk S5 Soft Off — Main power rail off, only standby power rail present

Term	Definition
SAFS	Term for Slave Attached Flash Sharing where the Flash component is attached behind a BMC component.
SATA	Serial AT Attachment: serial-interface standard for hard disks
SCSI	Small Computer System Interface – an interface standard for high end disk drives and other computer peripherals
SDP	Software-Definable Pin
SGMII	Serial Gigabit Media Independent Interface
SM Bus	System Management Bus
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
SPI	Serial Peripheral Interface
Super I/O	An integrated circuit, typically interfaced via the LPC bus that provides legacy PC I/O functions including PS2 keyboard and mouse ports, serial and parallel port(s) and a floppy interface.
TFT	Thin Film Transistor – refers to technology used in active matrix flat-panel displays, in which there is one thin film transistor per display pixel.
TMDS	Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. TMDS is used for the DVI digital signals.
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
USB	Universal Serial Bus
VGA	Video Graphics Adapter – PC-AT graphics adapter standard defined by IBM.
WDT	Watch Dog Timer.
XAUI	10 Gigabit / sec Attachment Unit Interface.
XGMII	10 Gigabit Media Independent Interface

1.7 Applicable Documents and Standards

The following publications are used in conjunction with this standard. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- 10GBASE-KR: 802.3ap-2007 - Amendment to IEEE Std 802.3-2005 - IEEE Standard for Information technology-- Local and metropolitan area networks - Specific requirements - Part 3: CSMA/CD Access Method and Physical Layer Specifications - Amendment: Ethernet Operation Over Electrical Backplanes
  http://standards.ieee.org/getieee802/download/802.3bw-2015.pdf
- ACPI Advanced Configuration and Power Interface Specification Revision 4.0, June 16, 2009
  Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved.
  http://www.acpi.info/
- DDC Display Data Channel Command Interface Standard (formerly DDC2Bi)
  Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved.
  http://www.vesa.org
- DisplayPort Interoperability Guideline Version 1.1a dated February 5, 2009
  http://www.vesa.org/vesa-standards/free-standards/
- DisplayPort Standard Version 1.4
  http://www.vesa.org/
- Embedded Display Port (eDP) Specification Rev. 1.4b, Oct 10, 2015
  http://www.vesa.org
- eSPI Enhanced Serial Peripheral Interface, Interface Base Specification
  Revision 1.0, Copyright © 2016, Intel Corporation. January 2016
  https://downloadcenter.intel.com/download/22112
- HDA - High Definition Audio Specification, Revision 1.0, April 15, 2004
  Copyright © 2002 Intel Corporation. All rights reserved.
  http://www.intel.com/standards/hdaudio/
- High-Definition Multimedia Interface specification version 1.3
  http://www.hdmi.org
- IEEE 802.3-2015, IEEE Standard for Information technology, Telecommunications and information exchange between systems-Local and metropolitan area networks-Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications."
  http://www.ieee.org
- IEEE1588 - 2008. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, July 24, 2008, Copyright 2016 IEEE
  http://standards.ieee.org/findstds/standard/1588-2008.html
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved.
  http://developer.intel.com/design/chipsets/industry/lpc.htm
- LVDS ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- NC-SI Network Controller Sideband Interface Specification
  Document Number: DSP0222, Jul 21, 2009, Version: 1.0.0
  Copyright© 2009 Distributed Management Task Force, Inc. (DMTF).
  http://www.dmtf.org/sites/default/files/standards/documents/DSP0222_1.0.0.pdf

- PCI Express Base Specification Revision 3.1, December 7, 2015, Copyright © 2002-2006 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 2.0, April 11, 2007, Copyright © 2002-2007 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 3.0, February 3, 2004 Copyright © 1992, 1993, 1995, 1998, and 2004 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PICMG® EAPI - Embedded Application Software Interface Specification, Revision 1.0, 2010, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239.
  http://www.picmg.org/
- SDIO, Secure Digital Input/Output
  SD Specifications Part E1 SDIO Specification Version 2.00, February 8, 2007
  Copyright 2007 SD Card Association
  http://www.sdcard.org
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/
- SFP+, SFF-8083 Rev 3.1, SFF-8083 Specification for SFP+ 1X 10 Gb/s Pluggable Transceiver Solution (SFP10)
  Rev 3.1, Sep. 13, 2014
  ftp://ftp.seagate.com/sff/SFF-8083.PDF
- Smart Battery Data Specification Revision 1.1, December 11, 1998.
  www.sbs-forum.org
- SPI, Serial Peripheral Interface Bus
  http://elm-chan.org/docs/spi_e.html
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Trusted Platform Module (TPM), Trusted Computing Group Specification 1.2 Revision 103, July 9, 2007
  http://www.trustedcomputinggroup.org
- USB 3.0 Specification, Revision 1.0, November 12, 2008, 2000
  Copyright © 2007-2008 Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, NEC Corporation, ST-NXP Wireless and Texas Instruments. All rights reserved.
  http://www.usb.org/

1.8 Special Word Usage

In this specification the following key words (in ***bold*** text) will be used:

Table 1.2: Special Word Usage

may	Indicates flexibility of choice with no implied preference.
should	Indicates flexibility of choice with a strongly preferred implementation. The use of ***should not*** (in ***bold*** text) indicates a flexibility of choice with a strong preference that the choice or implementation should be prohibited.
shall	Indicates a mandatory requirement Designers ***shall*** implement such mandatory requirements to ensure interchangeability and to chlaim conformance with this specification. The use of ***shall not*** (in ***bold*** text) indicates an action or implementation that is prohibited.

Note: When not in bold text, the words “may,” “should,” and “shall” are being used in the traditional sense; that is, they do not adhere to the strict meanings described above.

1.9 Statement of Compliance

Statements of compliance with this specification take the form specified in the PICMG® Policies and Procedures for Specification Development:
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A simple claim of compliance with a subsidiary specification indicates the presence of all features defined as being mandatory by the use of the keyword "***shall***" in the body of that specification and must not include any feature prohibited by the use of the keyword "***shall not***". Because subsidiary specifications may also provide for recommended and permitted features beyond the mandatory minimum set and a range of performance capabilities, more complete descriptions of product compliance are encouraged.
Normative language in the appendices is not in the enumerated requirements format, but is considered normative and required for compliance.

2 Module Overview

2.1 Module Configuration

Four Module sizes are defined: the Mini Module, Compact Module, Basic Module and the Extended Module. The primary difference between the different size Modules is the over-all physical size and the performance envelope supported by each. The Extended Module is larger and can support larger processor and memory solutions. The Compact Module, Basic Module and Extended Module use the same connectors and pin-outs whereas the 84x55 Mini Module targets, but is not limited to use the COM Express A-B connector, Type 10 pin-out. In addition the Mini Module allows for wide range power supply operation. The different size Modules share several common mounting hole positions. This level of compatibility allows that a Carrier Board can be designed to accommodate multiple Module sizes.

Up to 440 pins of connectivity are available between COM Express Modules and the Carrier Board. New Interfaces include high speed serial interconnects such as PCI Express, Serial ATA, USB 2.0 / 3.0, Gigabit and 10 Gigabit Ethernet. To enhance interoperability between COM Express Modules and Carrier Boards, several common signaling configurations (Pin-out Types) have been defined to ease system integration. Pin-out Type 10 definition require only a single 220-pin connector and pin-out types 6 and 7 require both 220-pin connectors to supply all the defined signaling.

2.2 Feature Overview - Size

2.2.1 Mini Module

The Mini Module targets the next generation of mobile applications that require highest level of integration, high-end graphics combined with longer battery life. Key features of the Mini Module include:

- Module size: 84mm x 55mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- Wide-range power supply input (4.75-20V)
- Single 220-pin connector (2nd connector not normally used)
- Reduced Z height for components (optional)

Although not a requirement, Mini Modules are often implemented with memory and SSD storage soldered down on the Module. This facilitates their use in ruggedized, small form factor mobile systems.

2.2.2 Compact Module

The Compact Module is intended for mobile systems and space-constrained stationary systems. Key features of the Compact Module include:

- Module size: 95mm x 95mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- 18mm 'z' height with heat-spreader (using the 5mm stack option)
- Accommodates a single (or two stacked) horizontal mount SO-DIMM
- Dual 220-pin connectors for up to 440 pins

2.2.3 Basic Module

The Basic Module is intended for mobile systems and space-constrained stationary systems. Key features of the Basic Module include:

- Module size: 125mm x 95mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- 18mm 'z' height with heat-spreader (using the 5mm stack option)
- Accommodates a single (or two stacked) horizontal mount SO-DIMM
- Dual 220-pin connectors for up to 440 pins

2.2.4 Extended Module

The Extended Module, which targets OEM applications that require larger amounts of system memory, features a larger Module size to accommodate full size DIMMs and larger chipset and CPU packages.

The key features of the Extended Module include:

- Module size: 155mm x 110mm
- 5mm and 8mm stack height options (Module bottom to Carrier Board top)
- 18mm 'z' height with heat-spreader (using the 5mm stack option)
- Accommodates 2 full-size DIMM or mini DIMM memories or 2 horizontal mount or vertical mount SO-DIMMs

- Dual 220-pin connectors for up to 440 pins
- Allows for the use of higher performance CPUs that can not be supported on the Compact Module or Basic Module

2.3 Feature Overview - Pin-Out Types

For legacy Types (1-5) which are not recommended for new designs, see the previous revision of the specification for more information.

2.3.1 Pin-Out Type 10

- Single 220-pin connector (A-B connector)
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- USB 3.0 support on up to 2 ports
- USB Client support on USB0 and USB7
- Up to 2 Serial ATA ports
- Up to 4 PCI Express lanes
- Single 24-bit LVDS channel with option to overlay with eDP
- One Digital Display Interface configurable as DP or TMDS
- HDA digital audio interface (external CODEC(s) required)
- Single Ethernet interface with integrated PHY – pinned for Gigabit Ethernet
- SPI Support
- LPC/eSPI interface
- IEEE 1588 support
- Two TX/RX serial pairs with option to overlay CAN interface on one port
- Fan control
- TPM support
- 8 GPIO pins
- 68W maximum input power over Module connector pins
- +12V primary power supply input for Compact, Basic and Extended form factor
- Wide input voltage range for Mini form factor
- +5V standby and 3.3V RTC power supply inputs

2.3.2 Pin-Out Type 6

- Dual 220-pin connectors (A-B and C-D, 440 pins total)
- Up to 22 PCI Express lanes (up to 6 on A-B and up to 16 on C-D)
- Up to 8 USB 2.0 ports
- Up to 4 SuperSpeed ports for USB 3.0 support
- USB Client support on USB0 and USB7
- Up to 4 Serial ATA ports
- Dual 24-bit LVDS channels
- Analog VGA
- HDA digital audio interface (external CODEC(s) required)
- Single Ethernet interface with integrated PHY
- LPC/eSPI interface
- IEEE 1588 support
- SPI Support
- 8 GPIO pins
- Up to 3 Digital Display Interfaces
- Allow eDP overlay of LVDS Channel A
- Two TX/RX serial pairs with option to overlay CAN interface on one port
- 137W maximum input power over Module connector pins
- +12V primary power supply input
- +5V standby and 3.3V RTC power supply inputs

2.3.3 Pin-Out Type 7

All Pin-out Type 6 features with the exception of the following:

- Removed all video interfaces (3x DDI, LVDS, VGA)
- Removed audio interface
- Reduced SATA to 2 ports
- Removed 4 sets of USB 2.0 signals
- Added 8 PCI Express lanes for a total of 32 PCI Express lanes (16 on the PEG port)
- Added 4 x 10 Gb Ethernet with side band signals
- Added NC-SI for GbE port

3 Required and Optional Features

3.1 Module Pin-Out Type Definitions

Several pin-out types are defined. Pin-out Type 10 Modules have a single 220-pin connector, the A-B connector. Module Pin-out Types 6 and 7 use a pair of 220-pin connectors, designated A-B and C-D, for a total of 440 pins. The variations in Pin-out Type definitions are summarized in the table below.

Table 3.1: Module Pin-out Type Overview

Types	Connector Rows	PCI Express Lanes	PEG	SATA Ports	LAN Ports	USB 2.0 / SuperSpeed USB	Display Interfaces
Type 6	A-B C-D	Up to 24	1	4	1	8 / 4[1]	VGA, LVDS/eDP,PEG, 3xDDI
Type 7	A-B C-D	Up to 32	-	2	5 (1x 1G, 4x 10G)	4 / 4[1]	-
Type 10	A-B	Up to 4	-	2	1	8 / 2[1]	LVDS/ eDP,1xDDI

For Module Pin-out Type 6, a subset of the PCI Express lanes are commonly used as PCI Express Graphics (PEG) lanes. Type 10 features one DDI, but no PEG lanes.

eSPI is introduced as an alternative for the legacy LPC bus on types 6, 7, & 10.

Type 10 Modules support a single 24 bit LVDS panel interface, a single DDI and an eDP overlayed on LVDS Channel A and an option to allow a CAN bus to share SER1 pins. Two of the 8 USB ports can be used as USB 3.0.

Type 6 Modules support up to 24 PCI Express lanes, up to three DDIs and 4 of the 8 USB ports can be used as USB 3.0. Type 6 Modules support a single or dual channel 18/24 bit LVDS panel interface, three DDIs and an eDP overlayed on LVDS Channel A and an option to allow a CAN bus to share SER1 pins.

Type 7 Based on Type 6. Modules trades all audio and video interfaces, 2 SATA ports and four USB 2.0 for additional PCI Express lanes, four 10 Gb Ethernet ports and an NC-SI management interface for the GbE port.

1 *The SuperSpeed USB ports are not in addition to the USB 2.0 ports. Ports that support SuperSpeed, USB 3.0, also support USB 2.0.*

3.2 Module Pin-Out Types 6-7 & 10 - Required and Optional Features

COM Express Required and Optional features are summarized in the following table. The features identified as Minimum (Min.) ***shall*** be implemented by all Modules. Features identified up to Maximum (Max) ***may*** be additionally implemented by a Module.

Table 3.2: Module Pin-out - Required and Optional Features

Feature	Type 10 Min / Max	Type 6 Min / Max	Type 7 Min / Max
System I/O			
PCI Express Lanes 0 - 5	1 / 4	1 / 6	6 / 6
PCI Express Lanes 6 - 15	NA	0 / 2	0 / 10
PCI Express Lanes 16 - 31	NA	0 / 16	0 / 16
PCI Express Graphics (PEG)	NA	0 / 1	NA
10G LAN Ports 0 - 3	NA	NA	0 / 4
NC-SI	NA	NA	0 / 1
1Gb LAN Port 0	1 / 1	1 / 1	1 / 1
DDI 0	0 / 1	NA	NA
DDIs 1 - 3	NA	0 / 3	NA
LVDS Channel A	0 / 1	0 / 1	NA
LVDS Channel B	NA	0 / 1	NA
eDP on LVDS CH A pins	0 / 1	0 / 1	NA
VGA Port	NA	0 / 1	NA
Serial Ports 1 - 2	0 / 2	0 / 2	0 / 2
CAN interface on SER1	0 / 1	0 / 1	0 / 1
SATA Ports	1 / 2	1 / 4	0 / 2
HDA Digital Interface	0 / 1	0 / 1	NA
USB 2.0 Ports	4 / 8	4 / 8	4 / 4
USB0 Client	0 / 1	0 / 1	0 / 1
USB7 Client	0 / 1	0 / 1	NA
USB 3.0 Ports	0 / 2	0 / 4	0 / 4
LPC Bus or eSPI	1 / 1	1 / 1	1 / 1
SPI (Devices)	1 / 2	1 / 2	1 / 2
Rapid Shutdown	NA	0 / 1	0 / 1
System Management			
SDIO (muxed on GPIO)	0 / 1	0 / 1	0 / 1
General Purpose I/O	8 / 8	8 / 8	8 / 8
SMBus	1 / 1	1 / 1	1 / 1
I2C	1 / 1	1 / 1	1 / 1
Watchdog Timer	0 / 1	0 / 1	0 / 1
Speaker Out	1 / 1	1 / 1	1 / 1
Carrier Board BIOS Flash Support	0 / 1	0 / 1	0 / 1
Reset Functions	1 / 1	1 / 1	1 / 1

Feature	Type 10 Min / Max	Type 6 Min / Max	Type 7 Min / Max
Trusted Platform Module	0 / 1	0 / 1	0 / 1
Power Management			
Thermal Protection	0 / 1	0 / 1	0 / 1
Battery Low Alarm	0 / 1	0 / 1	0 / 1
Suspend/Wake Signals	0 / 3	0 / 3	0 / 3
Power Button Support	1 / 1	1 / 1	1 / 1
Power Good	1 / 1	1 / 1	1 / 1
VCC_5V_SBY Contacts	4 / 4	4 / 4	4 / 4
Sleep Input	0 / 1	0 / 1	0 / 1
Lid Input	0 / 1	0 / 1	0 / 1
Carrier Board Fan Control	0 / 1	0 / 1	0 / 1
Power			
VCC_12V Contacts	12 / 12	24 / 24	24 / 24

3.3 Feature Fill Order

COM Express allows a variable number of ports to be implemented for several interfaces, per Table Table 3.2 above. Ports ***shall*** be populated in a "low to high" manner, per the following table.

Table 3.3: Module Feature Fill Order

Feature	Number of Ports	Fill Order
LAN	1	GbE channel 0
10G LAN	1	10GbE Port 0
	2	10GbE Port 0, 1
	3	10GbE Port 0, 1, 2
	4	10GbE Port 0, 1, 2, 3
LVDS	Single Channel	LVDS channel A
	Dual Channel	LVDS channels A,B
SATA	2	SATA channels 0,1
	3	SATA channels 0,1,2
	4	SATA channels 0,1,2,3
USB 2.0 Host	4	USB channels 0,1,2,3
	5	USB channels 0,1,2,3,4
	6	USB channels 0,1,2,3,4,5
	7	USB channels 0,1,2,3,4,5,6
	8	USB channels 0,1,2,3,4,5,6,7
USB 2.0 Client	1	USB channel 0 for new designs
	2	USB channel 0, 7
USB 3.0 SuperSpeed[2]	1	USB channel 0
	2	USB channels 0,1
	3	USB channels 0,1,2
	4	USB channels 0,1,2,3
DDI	1	DDI 1
	2	DDI 1, 2
	3	DDI 1, 2, 3

The COM Express PCI Express lanes also have a prescribed fill order, described in Section 5.2 'PCI Express Link Configuration Guidelines' on page 89.

2 *The number of USB 2.0 channels must be equal to or greater than the number of USB 3.0 channels*

3.4 EAPI - Embedded Application Programming Interface

All COM Express Modules ***should*** support the Revision 1.1 of the PICMG defined Software API EAPI. This API allows for an easier interoperability of COM Express Modules.

Addressed functions are:

- System information
- Watchdog timer
- I2C Bus
- Flat Panel brightness control
- User storage area
- GPIO

4 Signal Descriptions

4.1 Signal Naming Convention

Active-low signals are indicated by a trailing '#' sign: REQ#
Differential pairs are indicated by trailing '+' and '-' signs: TX+, TX-
Bused signals are indicated by brackets, with LS bit first, MS bit last: A[0:31]
Bus brackets may appear anywhere in the signal name: CBE[0:3]#

4.2 Pin and Signal Buffer Types

Pin and Buffer type definitions apply to the signals in the Signal List Section below.

4.2.1 Pin Types

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input / output signal
OD	Open drain output

4.2.2 Buffer Types

CMOS	Logic input or output. Input thresholds and output levels ***shall*** be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
CMOS-T	Logic input or output are the same as specified in CMOS. Tolerant of higher voltages. See Section 4.2.3
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (Module outputs) ***shall*** be AC coupled on the Module. PCIE receive pins (Module inputs) ***shall*** be DC coupled on the COM Express Module and ***shall*** be assumed to be AC coupled off-Module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the Module PCIE receive lanes (target PCIE device transmit lanes) ***shall*** be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals ***shall*** be AC coupled on the add-in card, not on the Carrier Board.
PCI	PCI 2.3 compatible signal. Please refer to the PCI Rev. 2.3 Specification for details.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM Express SATA signals ***shall*** be AC coupled on the Module
LVDS	Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.
USB	USB 2.0 compatible differential signal. Please refer to the USB 2.0 Specification for details.
REF	Reference voltage output. ***May*** be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.
Analog	Inputs and Outputs used for LAN, and VGA are analog signals.
Power	Inputs used for power delivery to the Module electronics.
KR	10GBASE-KR compatible signal

4.2.3 Power Rails and Tolerances

Pins are marked in Section 4.3 'Signal List' with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance may be different. For example, the serial ports are defined as having 5V power rail meaning that the output rails will only be driven to 5V, but the pins are tolerant of 12V signals.

An additional label, “Suspend” indicates that the pin is active during suspend states (S3,S4,S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

4.3 Signal List

COM Express signal descriptions are described in the following table. The Pin Availability column in the table indicates in which Pin-out Types the signal is available. Module Pin-out Types 6, 7 and 10 are designated T6 ,T7, T10 in the Pin Availability column. A notation of “All” indicates that the signal is available to all (T6, T7, and T10) Module Pin-out Types.

4.3.1 High Definition Audio

Table 4.1: HDA Signals, Pin Types, and Descriptions

High Definition Audio	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
HDA_RST#	O CMOS	3.3V Suspend/ 3.3V	Reset output to CODEC, active low.	T6,T10
HDA_SYNC	O CMOS	3.3V / 3.3V	Sample-synchronization signal to the CODEC(s).	T6,T10
HDA_BITCLK	I/O CMOS	3.3V / 3.3V	Serial data clock generated by the external CODEC(s).	T6,T10
HDA_SDOUT	O CMOS	3.3V / 3.3V	Serial TDM data output to the CODEC.	T6,T10
HDA_SDIN[0:2]	I/O CMOS	3.3V Suspend/ 3.3V	Serial TDM data inputs from up to 3 CODECs.	T6,T10

The HDA signal level from some chipsets might be 1.5V. Module designers must add any necessary voltage translation circuitry to meet the COM Express 3.3V signaling requirement for HDA signals.

The HDA codec on a COM Express Carrier Board ***shall*** be connected as the primary codec with the codec ID 00 using the data input line 'HDA_SDIN0'. Up to two additional codecs with ID 01 and ID 10 ***may*** be connected to the COM Express Module by using the other designated signals HDA_SDIN[1:2].

4.3.2 Gb Ethernet

One Gigabit Ethernet port is defined, designated GBE0. The ports ***may*** operate in 10, 100, or 1000 Mbit/sec modes. Magnetics are assumed to be on the Carrier Board. All COM Express Modules ***shall*** implement at least one Ethernet port on the GBE0 pin slot and this ***should*** be capable of at least 10/100 mode.

Table 4.2: Gigabit Ethernet Signals, Pin Types, and Descriptions

Gigabit Ethernet	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	I/O Analog	3.3V max Suspend	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:	All
GBE0_ACT#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 activity indicator, active low.	All
GBE0_LINK#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 link indicator, active low.	All
GBE0_LINK100#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	All
GBE0_LINK1000#	OD CMOS	3.3V Suspend/ 3.3V	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	All
GBE0_CTREF	REF	GND min 3.3V max	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output ***shall*** be current limited on the Module. In the case in which the reference is shorted to ground, the current ***shall*** be limited to 250 mA or less.	All
GBE0_SDP	I/O	3.3V Suspend / 3.3V	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.5 for details.	All

	1000BASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

4.3.3 NC-SI

The NC-SI ('Network Controller Sideband Interface') is an electrical interface and protocol defined by the Distributed Management Task Force (DMTF), which enables the connection of a BMC (Baseboard Management Controller) to enable out-of-band remote manageability.
If implemented, the NC-SI ***shall*** be assigned to the GBE0 interface. NC-SI architecture also enables multiple endpoints to be connected to the same management controller. In this configuration, the bus arbitration can also be implemented by hardware using a token ring configuration. The NCSI_ARB_IN pin of one controller must be connected to the NCSI_ARB_OUT of another controller to form a ring configuration. A maximum of four network controllers can be connected in this manner and all controllers sharing the same NC-SI interface pins must support this feature in order to use hardware-based arbitration. NCSI_ARB_IN and NCSI_ARB_OUT are to be left unconnected on the Carrier if there is no Carrier network controller.

Table 4.3: NC-SI Signals, Pin Types, and Descriptions

NC-SI	Pin Type	Pwr Rail / Tolerance	Description	PU/PD	Pin Availability
NCSI_CLK_IN	I CMOS	3.3V Suspend / 3.3V	NC-SI Clock reference for receive, transmit, and control interface.	PD 10K	T7
NCSI_RXD[0:1]	O CMOS	3.3V Suspend / 3.3V	NC-SI Receive Data (from NC to BMC).		T7
NCSI_TXD[0:1]	I CMOS	3.3V Suspend / 3.3V	NC-SI Transmit Data (from BMC to NC).	PD 10K	T7
NCSI_CRS_DV	O CMOS	3.3V Suspend / 3.3V	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.		T7
NCSI_TX_EN	I CMOS	3.3V Suspend / 3.3V	NC-SI Transmit enable.	PD 10K	T7
NCSI_RX_ER	O CMOS	3.3V Suspend / 3.3V	NC-SI Receive error.		T7
NCSI_ARB_IN	I CMOS	3.3V Suspend / 3.3V	NC-SI hardware arbitration input.	PU 10K	T7
NCSI_ARB_OUT	O CMOS	3.3V Suspend / 3.3V	NC-SI hardware arbitration output.		T7

4.3.4 10Gb Ethernet

10GBASE-KR support was added to COM Express with revision 3.0 of the specification. Type 7 supports up to four 10GBASE-KR interfaces. The 10G MAC is located on the Module and the PHY is located on the Carrier. 10GBASE-KR uses a single transmit and a single receive ac coupled differential pair for data and a sideband bus for the PHY control and configuration. COM Express supports both MDIO and I2C control interfaces for the PHY. The PHY control interfaces are grouped into pairs. 10G Ports 0 and 1 share a common PHY control interface and 10G ports 2 and 3 share a common PHY control interface. The PHY interface selection is made using the 10G_PHY_CAP_01 and 10G_PHY_CAP_23 pins. The Carrier design can select the PHY that is appropriate for the design. The Module designer ***should*** design the module in such a way that it can provide the PHY interface that is selected regardless of the capabilities of the silicon used on the Module. Appropriate level shifters ***shall*** be used.

A two wire I2C bus (designated 10G_LED_SDA and 10G_LED_SCL) is defined to serialize the outbound (Module to Carrier) MAC LED and PHY strapping signals, conserving COM Express pins. The Carrier ***should*** use a PCA9539 or compatible I2C I/O expander. The Carrier PCA9539 ***shall*** be mapped to I2C address 1110 100x (x=R/W bit). Table Table 4.5 below defines the port pin mapping for the I/O expander.

There are two pairs of PHY strapping signals defined. The first pair is designated as 10G_PHY_CAP_01 and 10G_PHY_CAP_23. These are actual COM Express pins. They are inputs to the COM Express Module. The Carrier ***may*** either tie these lines to GND or leave them NC on the Carrier. If 10G_PHY_CAP_01 is tied low on the Carrier, this indicates to the Module that the PHY on the Carrier for 10G interfaces 0 and 1 can be configured by either I2C or by MDIO. If the Carrier leaves the line NC, then this indicates to the Module that the Carrier PHY can only be configured by MDIO. Similarly for strap signal 10G_PHY_CAP_23 and 10G interfaces 2 and 3.

The second pair of PHY strapping signals are outputs from the Module, serialized onto the 10G_LED_Sxx I2C bus. They are deserialized on the Carrier I/O expander and ***may*** used to set Carrier PHY strapping pins to set the desired Carrier PHY configuration mode, if the PHY is capable of multiple configuration modes.

This arrangement with a pair of input straps (telling the Module what configuration modes are possible on the Carrier PHY) and a pair of serialized output straps (telling the Carrier PHY what configuration mode to use) allow Module designs that can use a variety of PHYs. In particular, Intel Broadwell DE Modules that can be used with either Intel "Coppervale" PHYs or with Inphy / Cortina PHYs can be realized. Block diagram examples may be found in Appendix 9.5 ‘Example 10 GB Ethernet Designs’ of this document.

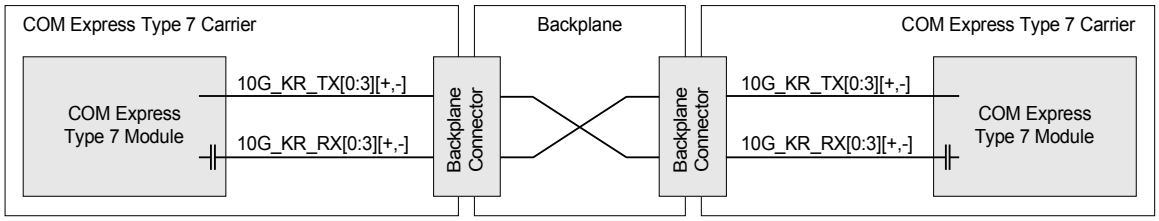
Table 4.4: 10Gigabit Ethernet Pin Types and Descriptions

10Gigabit Ethernet	Pin Type	Pwr Rail / Tolerance	Description	PU/PD	Pin Availability
10G_KR_TX[0:3]+ 10G_KR_TX[0:3]-	O KR	AC coupled at receiver	10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling		T7
10G_KR_RX[0:3]+ 10G_KR_RX[0:3]-	I KR	AC coupled on Module	10GBASE-KR ports, receive input differential pairs.		T7
10G_PHY_MDIO_SDA[0:3]	O CMOS	3.3V Suspend / 3.3V	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.		T7
	I/O OD CMOS	3.3V Suspend / 3.3V	**I²C Mode:** I²C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	PU 2K2	T7
10G_PHY_MDC_SCL[0:3]	O CMOS	3.3V Suspend / 3.3V	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY.		T7
	I/O OD CMOS	3.3V Suspend / 3.3V	**I²C Mode:** I²C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	PU 2K2	T7
10G_PHY_CAP_01	I CMOS	3.3V Suspend / 3.3V	Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I²C interface (see Table 4.4)	PU 10K	T7
10G_PHY_CAP_23	I CMOS	3.3V Suspend / 3.3V	Phy mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I²C interface (see Table 4.4)	PU 10K	T7
10G_SFP_SDA[0:3]	I/O OD CMOS	3.3V Suspend / 3.3V	I²C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	PU 2K2	T7
10G_SFP_SCL[0:3]	I/O OD CMOS	3.3V Suspend / 3.3V	I²C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	PU 2K2	T7
10G_LED_SDA	I/O OD CMOS	3.3V Suspend / 3.3V	I²C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs. Refer to the details in table Table 4.5 'I2C Data Mapping to Carrier Board Based PCA9539 I/O Expander'	PU 2K2	T7
10G_LED_SCL	I/O OD CMOS	3.3V Suspend / 3.3V	I²C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs.	PU 2K2	T7
10G_INT[0:3]	I CMOS	3.3V Suspend / 3.3V	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	PU 2K2	T7
10G_SDP[0:3]	I/O CMOS	3.3V Suspend / 3.3V	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.5 for details.		T7
10G_PHY_RST_01	O CMOS	3.3V Suspend / 3.3V	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used).		T7
10G_PHY_RST_23	O CMOS	3.3V Suspend / 3.3V	Output signal that resets an Optical PHY on port 2 and port 3 (with Copper PHY this signal is not used).		T7

AC Coupling of 10G_KR_TX Signals

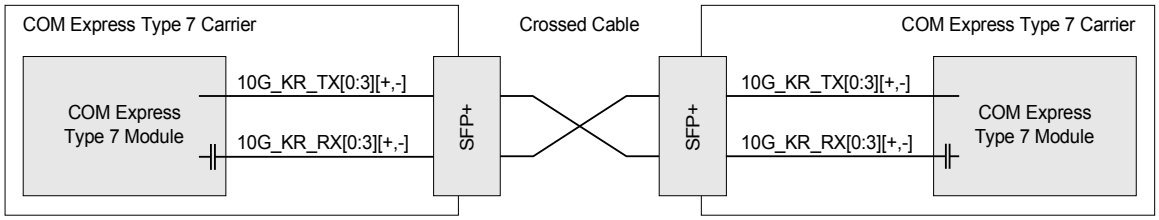
Situation A: Backplaned system (eg VPX®, CPCI®, ..)
Coupling is at receiver, in this case on both modules at receive pair. No coupling on carrier.

Figure 4-1: 10G Ethernet AC coupling – backplane system



Situation B: Direct attached module-to-module connection.
Coupling is at receiver, in this case on both modules at receive pair. No coupling on carrier.

Figure 4-2: 10G Ethernet AC coupling – direct cable



Situation C: PHY on Carrier
Only in this situation the coupling is on the Carrier (at PHY). But this situation is not the only primary function for KR interface (backplane metallic connection).

Figure 4-3: 10G Ethernet AC coupling – PHY on Carrier

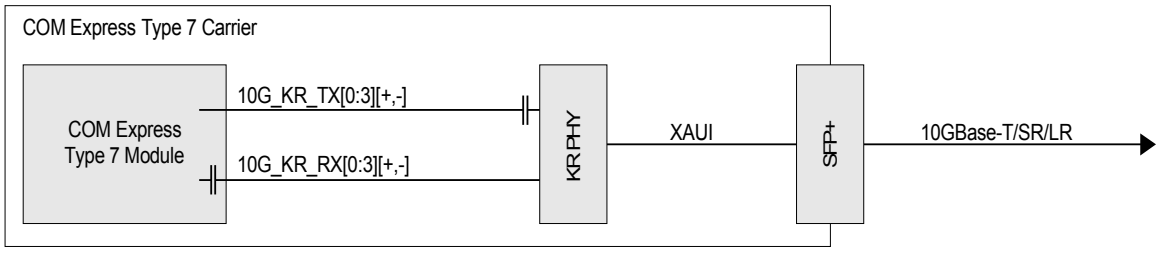


Table 4.5: I2C Data Mapping to Carrier Board Based PCA9539 I/O Expander

Port Pin	Signal Name	Signal Function
P0_0	10G_KR_LED0_0#	PHY 0, LED 0 - STATUS/ACT
P0_1	10G_KR_LED0_1#	PHY 0, LED 1 - LINK SPEED MAX
P0_2	10G_KR_LED0_2#	PHY 0, LED 2 - LINK SPEED
P0_3	10G_KR_LED1_0#	PHY 1, LED 0 - STATUS/ACTIVITY
P0_4	10G_KR_LED1_1#	PHY 1, LED 1 - LINK SPEED MAX
P0_5	10G_KR_LED1_2#	PHY 1, LED 2 - LINK SPEED
P0_6	10G_KR_STRAP01	PHY 0-1, 0 = PHY to use I2C, 1 = PHY to use MDIO
P0_7	10G_KR_STRAP23	PHY 2-3, 0 = PHY to use I2C, 1 = PHY to use MDIO
P1_0	10G_KR_LED2_0#	PHY 2, LED 0 - STATUS/ACT
P1_1	10G_KR_LED2_1#	PHY 2, LED 1 - LINK SPEED MAX
P1_2	10G_KR_LED2_2#	PHY 2, LED 2 - LINK SPEED
P1_3	10G_KR_LED3_0#	PHY 3, LED 0 - STATUS/ACT
P1_4	10G_KR_LED3_1#	PHY 3, LED 1 - LINK SPEED MAX
P1_5	10G_KR_LED3_2#	PHY 3, LED 2 - LINK SPEED
P1_6	RSVD	TBD
P1_7	RSVD	TBD

4.3.5 SDP Pins

The Software Defined Pins (SDP) can be used to provide a timing communication path between the Module and Carrier. A board level signal that communicates time is a key element that facilitates clock synchronization between elements of a platform. Examples of such elements include, but are not limited to, CPU, Chipset, FPGA and others.

Modules ***should*** connect the SDP signal to a module element pin capable of propagating (transmitting) time, and/or time-stamping (receiving) the signal to extract time information from it. If implemented, the direction of the signal with respect to the module element ***should*** be able to be determined by system software.

Pulse Per Second (PPS):

A PPS signal conveys both frequency and phase and can be used to transfer time information between elements within a platform. It is commonly used because it encapsulates both frequency and time into a single signal. It is preferred over other methods that require more complex implementations of hardware and software. A GPS is probably the most widespread, high-quality, clock source capable of generating a PPS signal.

Platform-Level Synchronization Implementation Examples:

Example1: The Network Interface Controller (NIC) on the COM Module is Precision Time Protocol (PTP) capable and the COM designer has connected a software configurable, timing aware, pin on the NIC to the SDP pin on the module/carrier interface. Software can configure the NIC to output a PPS signal onto this pin that connects it to one or more elements on the module and/or carrier board.

Example2: The carrier board has provisions for connecting a PPS output from a GPS to the SDP signal connection to the module. The module element (i.e. NIC, CPU, Chipset) can receive the timing information from the carrier board and adjust its time accordingly.

Precision Time Protocol - Background

Standards such as IEEE 1588, 802.1AS, and Time Sensitive Networking (TSN) provide standards for synchronizing time between nodes on a local area network. Additional benefits of the standards may include lower latency and improved network traffic Quality of Service (QoS). Systems that commonly require synchronization include those made up of distributed nodes that perform measurement, control, and compute functions. These nodes may have clock sources with varying degrees of accuracy and stability.

System-wide time synchronization with sub-microsecond accuracy is supported, by PTP standards, with minimal network and compute resource utilization.

It is the merger of the platform-level synchronization and network level synchronization pieces that enable real-time distributed systems. Additional information regarding the aforementioned standards can be found in their respective specifications and widely available supporting documents.

Software Implementation:

The software architecture and features required to support platform and network level synchronization are outside the scope of this specification.

4.3.6 Serial ATA

Serial ATA links for support of existing SATA-150 (revision 1.0, 1.5Gb/s), SATA-300 (revision 2.0, 3Gb/s), and SATA-600 (revision 3.0, 6Gb/s) devices.

Table 4.6: SATA Signals, Pin Types, and Descriptions

Serial ATA	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SATA0_TX+ SATA0_TX-	O SATA	AC coupled on Module	Serial ATA Channel 0 transmit differential pair.	All
SATA0_RX+ SATA0_RX-	I SATA	AC coupled on Module	Serial ATA Channel 0 receive differential pair.	All
SATA1_TX+ SATA1_TX-	O SATA	AC coupled on Module	Serial ATA Channel 1 transmit differential pair.	All
SATA1_RX+ SATA1_RX-	I SATA	AC coupled on Module	Serial ATA Channel 1 receive differential pair.	All
SATA2_TX+ SATA2_TX-	O SATA	AC coupled on Module	Serial ATA Channel 2 transmit differential pair.	T6
SATA2_RX+ SATA2_RX-	I SATA	AC coupled on Module	Serial ATA Channel 2 receive differential pair.	T6
SATA3_TX+ SATA3_TX-	O SATA	AC coupled on Module	Serial ATA Channel 3 transmit differential pair.	T6
SATA3_RX+ SATA3_RX-	I SATA	AC coupled on Module	Serial ATA Channel 3 receive differential pair.	T6
(S)ATA_ACT#	I/O CMOS	3 3V / 3.3V	Serial ATA (activity indicator, active low.	All

4.3.7 General Purpose PCI Express Lanes

The number of available PCI Express lanes varies with the Module Pin-out Type (refer to Section 5.2 'PCI Express Link Configuration Guidelines' on page 89). If the Module supports off-Module x16 PCI Express Graphics, then PCI Express Lanes 16-31 ***shall*** be used to implement this.

Table 4.7: PCI Express Lanes Signals, Pin Types, and Descriptions

PCI Express Lanes (General Purpose)	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PCIE_TX[0:3]+ PCIE_TX[0:3]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 0 through 3	All
PCIE_RX[0:3]+ PCIE_RX[0:3]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 0 through 3	All
PCIE_TX[4:5]+ PCIE_TX[4:5]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 4 through 5	T6,T7
PCIE_RX[4:5]+ PCIE_RX[4:5]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 4 through 5	T6,T7
PCIE_TX[6:7]+ PCIE_TX[6:7]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 6 through 7	T6,T7
PCIE_RX[6:7]+ PCIE_RX[6:7]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 6 through 7	T6,T7
PCIE_TX[8:15]+ PCIE_TX[8:15]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 8 through 15 Different connector layout for Type 7	T7
PCIE_RX[8:15]+ PCIE_RX[8:15]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 8 through 15 Different connector layout for Type 7	T7
PCIE_TX[16:31]+ PCIE_TX[16:31]-	O PCIE	AC coupled on Module	PCI Express Differential Transmit Pairs 16 through 31 These are same lines as PEG_TX[0:15]+ and -	T6,T7
PCIE_RX[16:31]+ PCIE_RX[16:31]-	I PCIE	AC coupled off Module	PCI Express Differential Receive Pairs 16 through 31 These are the same lines as PEG_RX[0:15] + and -	T6,T7
PCIE_CLK_REF+ PCIE_CLK_REF-	O PCIE	PCIE	Reference clock output for all PCI Express and PCI Express Graphics lanes.	All

4.3.8 PEG PCI Express Lanes

In Type 6 the PEG lanes are the same lanes as PCI Express lanes 16-31.

Table 4.8: PEG Signals, Pin Types, and Descriptions

PCI Express Lanes x16 Graphics	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PEG_TX[0:15]+ PEG_TX[0:15]-	O PCIE	AC coupled on Module	PCI Express Graphics transmit differential pairs. These are the same lines as PCIE_TX[16:31]+ and - in Module pin-out Type 6	T6
PEG_RX[0:15]+ PEG_RX[0:15]-	I PCIE	AC coupled off Module	PCI Express Graphics receive differential pairs. These are the same lines as PCIE_RX[16:31]+ and - in Module pin-out type 6	T6
PEG_LANE_RV#	I CMOS	3.3V / 3.3V	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order.	T6

4.3.9 USB

All USB interfaces ***shall*** be USB 2.0 compliant. The minimum of 4 USB channels provides support for keyboard, mouse, CD/DVD drive, and one additional device. Up to four of the eight USB 2.0 ports ***may*** support the extended signaling for SuperSpeed USB 3.0. USB0 or USB7 ***may*** optionally be configured as a USB client.

Table 4.9: USB Signals, Pin Types, and Descriptions

USB	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
USB[0:3]+ USB[0:3]-	I/O USB	3 3V Suspend/ 3 3V	USB differential pairs, channels 0 through 3. For type 7 only, USB0 ***may*** be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, ***shall*** be host ports.	All
USB[4:7]+ USB[4:7]-	I/O USB	3 3V Suspend/ 3 3V	USB differential pairs, channels 4 through 7. USB7 ***may*** be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, ***shall*** be host ports.	T6, T10
USB_0_1_OC#	I CMOS	3 3V Suspend/ 3 3V	USB over-current sense, USB channels 0 and 1. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_2_3_OC#	I CMOS	3 3V Suspend/ 3 3V	USB over-current sense, USB channels 2 and 3. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	All
USB_4_5_OC#	I CMOS	3 3V Suspend/ 3 3V	USB over-current sense, USB channels 4 and 5. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	T6, T10
USB_6_7_OC#	I CMOS	3 3V Suspend/ 3 3V	USB over-current sense, USB channels 6 and 7. A pull-up for this line ***shall*** be present on the Module. An open drain driver from a USB current monitor on the Carrier Board ***may*** drive this line low. Do not pull this line high on the Carrier Board.	T6, T10
USB_SSTX[0:3]+ USB_SSTX[0:3]-	O PCIE	AC coupled on Module	Additional transmit signal differential pairs for the SuperSpeed USB data path.	T6, T7
USB_SSRX[0:3]+ USB_SSRX[0:3]-	I PCIE	AC coupled off Module	Additional receive signal differential pairs for the SuperSpeed USB data path.	T6,T7
USB_SSTX[0:1]+ USB_SSTX[0:1]-	O PCIE	AC coupled on Module	Additional transmit signal differential pairs for the SuperSpeed USB data path.	T10
USB_SSRX[0:1]+ USB_SSRX[0:1]-	I PCIE	AC coupled off Module	Additional receive signal differential pairs for the SuperSpeed USB data path.	T10
USB0_HOST_PRSNT	I CMOS	3 3V Suspend/ 3 3V	Module USB client ***may*** detect the presence of a USB host on USB0. A high value indicates that a host is present.	All
USB7_HOST_PRSNT	I CMOS	3 3V Suspend/ 3 3V	Module USB client ***may*** detect the presence of a USB host on USB7. A high value indicates that a host is present.	All

4.3.10 LVDS Flat Panel

Low voltage differential signaling flat-panel interface. The Module pin-out allows one single channel display interface (1 pixel per clock) with up to 24 bit color. Alternatively, one dual channel display (2 pixels per clock) with up to 24 bit color, 48 bits per clock is allowed. Includes panel backlight control and EDID support.
The LVDS A channel and the control signals are pin shared with eDP signals. Refer to Section 4.3.29 'eDP - Embedded DisplayPort'

Table 4.10: LVDS Signals, Pin Types, and Descriptions

LVDS Flat Panel	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
LVDS_A[0:3]+ LVDS_A[0:3]-	O LVDS	LVDS	LVDS Channel A differential pairs	T6, T10
LVDS_A_CK+ LVDS_A_CK-	O LVDS	LVDS	LVDS Channel A differential clock	T6, T10
LVDS_B[0:3]+ LVDS_B[0:3]-	O LVDS	LVDS	LVDS Channel B differential pairs	T6
LVDS_B_CK+ LVDS_B_CK-	O LVDS	LVDS	LVDS Channel B differential clock	T6
LVDS_VDD_EN	O CMOS	3.3V / 3.3V	LVDS panel power enable	T6, T10
LVDS_BKLT_EN	O CMOS	3.3V / 3.3V	LVDS panel backlight enable	T6, T10
LVDS_BKLT_CTRL	O CMOS	3.3V / 3.3V	LVDS panel backlight brightness control	T6, T10
LVDS_I2C_CK	I/O OD CMOS	3.3V / 3.3V	I2C clock output for LVDS display use	T6, T10
LVDS_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	I2C data line for LVDS display use	T6, T10

4.3.11 LPC and eSPI Interface

The Module LPC and eSPI interfaces share connector pins. A Module design ***may*** support either LPC or eSPI or both, at the Module vendor's discretion. Module pin ESPI_EN# is available for the Carrier to signal to the Module whether LPC or eSPI is to be used. The Carrier ***shall*** leave the ESPI_EN# unconnected on the Carrier for LPC operation. The Carrier ***shall*** tie ESPI_EN# to GND for eSPI operation. The Module ***shall*** terminate ESPI_EN# as appropriate to facilitate this.

The LPC bus is a 3.3V bus and eSPI is a 1.8V bus. There is the possibility of a mismatch – an eSPI only Module mated with a LPC only Carrier, or an LPC only Module on an eSPI Carrier. Module designers ***should*** protect the Module eSPI interface against accidental exposure to 3.3V Carrier LPC signals. Carrier designers ***should*** protect a Carrier eSPI interface against accidental exposure to 3.3V Module LPC signals. In both cases, a simple and low cost protection scheme ***may*** be realized with low value in-line series resistors (typically 33 ohms) and BAT54 Schottky diodes on each line. The diode anode is tied to the eSPI device pin and the cathode to the 1.8V supply rail. Ideally, that 1.8V supply rail can sink current. In the event of a mismatch, the offending (Module or Carrier) 3.3V rail is discharged through the series resistor and the Schottky diode to the (Carrier or Module) 1.8V rail and not through the eSPI device.

Table 4.11: LPC/eSPI, Pin Types, and Descriptions

LPC/eSPI Interface	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
LPC_AD[0:3] / ESPI_IO_[0:3]	I/O CMOS	3.3V / 3.3V	LPC Mode: LPC multiplexed address, command and data bus	All
		1.8V Suspend / 1.8V	ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. Multiplexed with LPC_AD[0:3]	
LPC_FRAME# / ESPI_CS0#	O CMOS	3.3V / 3.3V	LPC Mode: LPC Frame indicates the start of a LPC cycle.	All
		1.8V Suspend / 1.8V	ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.	
LPC_CLK / ESPI_CK	O CMOS	3.3V / 3.3V	LPC Mode: LPC clock output, 33MHz	All
		1.8V Suspend / 1.8V	ESPI Mode: eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations.	
LPC_DRQ[0:1]# / ESPI_ALERT[0:1]#	I CMOS	3.3V / 3.3V	LPC Mode: LPC serial DMA request	All
		1.8V Suspend / 1.8V	ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master.	
LPC_SERIRQ / ESPI_CS1#	I/O CMOS	3.3V / 3.3V	LPC Mode: LPC serial interrupt	All
	O CMOS	1.8V Suspend / 1.8V	ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.	
SUS_STAT# / ESPI_RESET#	O CMOS	3.3V Suspend / 3.3V	LPC Mode: SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state. (See Power Management section 4.3.11 for details)	All
		1.8V Suspend / 1.8V	ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.	
ESPI_EN#	I CMOS	NA	This signal is used by he Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on he carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier ***should*** only float his line or pull it low.	All
BIOS_DIS[0:1]#	I CMOS	NA	Selection strap to determine the BIOS boot device. The Carrier ***should*** only float these or pull them low, please refer to Table 4.13 for strapping options of BIOS disable signals.	All

4.3.12 SPI Interface

The SPI bus is used to support SPI-compatible flash devices. The SPI flash device can be up to 16 MB (128 Mb). The SPI bus is clocked at either 20 MHz, 25 MHz, 33 MHz or 50 MHz. SPI devices selected ***should*** support one of these frequencies.
In COM.0 Rev 2, the SPI interface was defined as a 3.3V interface. With COM.0 Rev 3, the SPI interface ***may*** be either 3.3V or 1.8V, as is best for the Module chipset at hand.

Table 4.12: SPI Signals, Pin Types, and Descriptions

SPI Interface[3]	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SPI_CS#	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V	Chip select for Carrier Board SPI - ***may*** be sourced from chipset SPI0 or SPI1	All
SPI_MISO	I CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V	Data in to Module from Carrier SPI	All
SPI_MOSI	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V	Data out from Module to Carrier SPI	All
SPI_CLK	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V	Clock from Module to Carrier SPI	All
SPI_POWER	O	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V	Power supply for Carrier Board SPI – sourced from Module – nominally 3 3V. The Module ***shall*** provide a minimum of 100mA on SPI_POWER. Carriers ***shall*** use less than 100mA of SPI_POWER. SPI_POWER ***shall*** only be used to power SPI devices on the Carrier Board.	All

3 *SPI support is introduced in COM.0 R2.0*

SPI Power

Introducing a SPI_POWER pin is desirable because some Module implementations will have the SPI power domain in power state S0 and others in S5. It is easier for Carrier Board designers to take the Carrier SPI power from a pin on the Module.

The SPI_POWER voltage level was defined as 3.3V in COM.0 Rev. 2. With COM.0 Rev. 3, the SPI_POWER voltage level ***may*** be 3.3V or 1.8V. This allows the Carrier SPI interface to operate at the level appropriate for the Module chipset, without the use of level shifters.

Module designs that implement a 1.8V Carrier SPI interface ***should*** protect themselves against possible exposure to 3.3V Carrier SPI signals.

Carrier designs that implement a 1.8V SPI interface ***should*** protect themselves against possible exposure to 3.3V Module SPI signals.

Module Vs Carrier Board Pull-ups

There ***shall*** not be any Carrier Board pull-ups or pull-downs on the five SPI_x signals. All such terminations ***shall*** be on the Module. The Module designer ***shall*** determine the correct power domain that these signals are terminated to.

Note: Carrier Board ***shall*** implement pull-ups to SPI_POWER on the SPI flash pins HOLD# and WP# which are not supported on the COM Express connector.

4.3.13 BIOS Boot Selection

Historical Context

On COM.0 R1.0, there was a single pin dedicated to the BIOS boot selection function. The pin was named BIOS_DISABLE#. If the Carrier Board left BIOS_DISABLE# unconnected, then the Module booted from the BIOS on the Module. That Module BIOS was allowed to be on any bus the Module designer chose (LPC, SPI, etc.). If the Carrier Board pulled BIOS_DISABLE# to GND, then the on-Module BIOS was disabled and the Module booted from a Carrier Board firmware hub (FWH) on the LPC bus.
On COM.0 R2.0, the BIOS options were expanded to support a SPI device on the Carrier. A second BIOS source selection pin (BIOS_DIS1#) was added. The BIOS_DISABLE# pin was renamed to BIOS_DIS0#. Additional pins were added to the COM Express interface to bring the SPI signals to the Carrier. Both SPI and Carrier LPC FWH were supported in COM.0 R2.0.
For COM.0 R3, the Module Carrier based BIOS options have been expanded to support eSPI devices. A third pin that affects the BIOS location, named ESPI_EN#, works in conjunction with BIOS_DIS1# and BIOS_DIS0# to define the BIOS boot path. Additionally, the concepts of Master Attached Flash Sharing (MAFS) and Slave Attached Flash Sharing (SAFS) are introduced.
LPC bus BIOS FWH support is removed in COM.0 R3. SPI and eSPI BIOS options are supported.

SPI Boot Flash Background

Contemporary Intel x86 systems require that the SPI boot flash to be divided into a number of regions that may include:

- Descriptor
- BIOS code
- Management Engine (ME) code
- GbE parameters
- Platform data

The Descriptor defines where the other regions are in the SPI device(s). The Descriptor is always at the bottom of the first SPI device, the SPI device that is selected by chipset SPI0 chip-select (chipset SPI_CS0#).
The first two regions, the Descriptor and the BIOS, are mandatory. The other regions are optional. The regions may all be packed into the same SPI device, or may be divided between more than one SPI device, although the Descriptor has to be at the bottom of the first SPI device. In most situations, all the SPI regions are packed into a single SPI device that is either on the Module or on the Carrier. Designers may have reasons for dividing the SPI boot flash regions between devices.
COM Express Rev 2 and Rev 3 define a SPI interface on the COM Express connector. The COM Express SPI interface has only one chip select. Chipsets typically have 2 SPI chip

selects. Module hardware may steer those chipset chip selects to an on-Module SPI device or devices or to a single off-module SPI device. The chip select steering is defined by the ESPI_EN#, BIOS_DIS1# and BIOS_DIS0# signals. Details on this are in Table Table 4.13 'BIOS Selection Straps' below.
The BIOS Entry point ***may*** be in SPI0 or SPI1 as determined by the descriptor table in the SPI0 device. The Module ***may*** have one or two SPI devices. Carrier Boards ***may*** have zero or one SPI devices, depending on the Module configuration.

MAFS and SAFS BIOS Configurations

Master Attached Flash Sharing (MAFS) is defined as the BIOS Flash directly attached to the processor SPI bus.
Slave Attached Flash Sharing (SAFS) is defined as the BIOS Flash being attached behind a board Management Controller (BMC) or Embedded Controller (EC).
MAFS and SAFS configurations apply to both LPC and eSPI enabled configurations. Refer to Figure 4-4 'BIOS Selection LPC Mode' and Figure 4-5 'BIOS Selection eSPI Mode' below. Please note that some of the features shown in these figures are mutually exclusive.

Figure 4-4: BIOS Selection LPC Mode

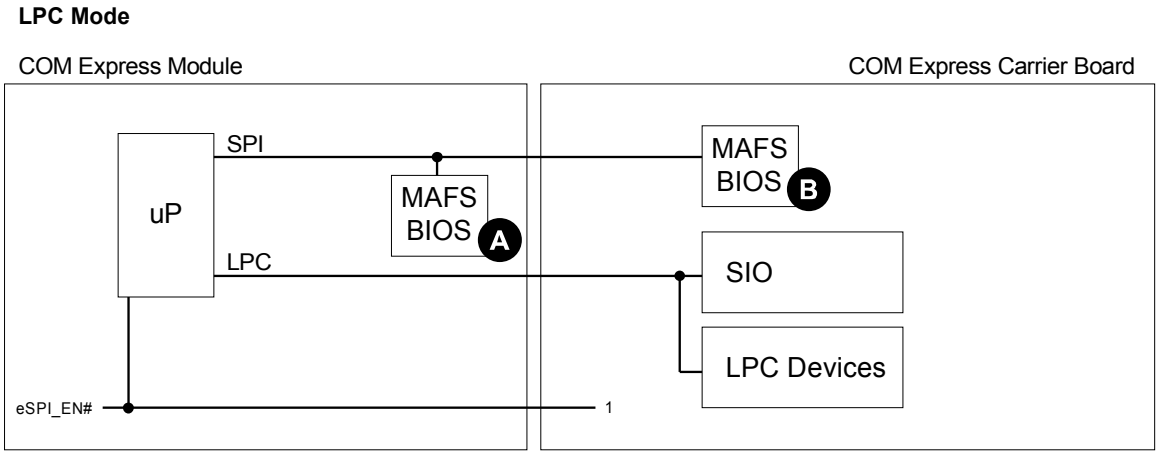
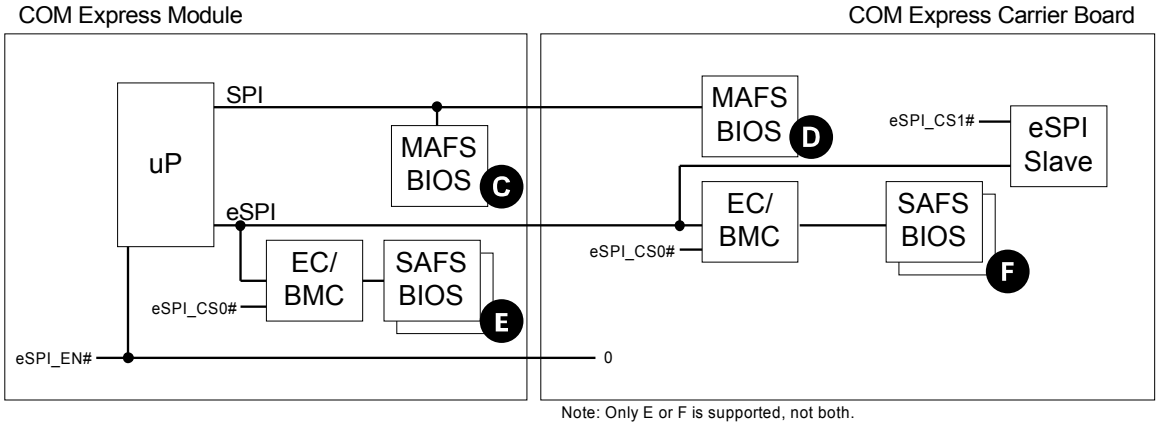


Figure 4-5: BIOS Selection eSPI Mode

eSPI Mode



Note: Only E or F is supported, not both.

The A and B notations in figure 4-4 above and the B, C, D and F notations in figure 4-5 above are referenced in the table and text sections below. Note also that some of the features shown in these figures are mutually exclusive.

Table 4.13: BIOS Selection Straps

ESPI_EN#	BIOS_DIS1#	BIOS_DIS0#	Boot Bus	BBS	Chipset ESPI_CS0# Destination	Carrier ESPI_CS0# Pin	Chipset SPI_CS1# Destination	Chipset SPI_CS0# Destination	Carrier SPI_CS# Pin	SPI Descriptor	Ref to Images Above	Notes
1	0	0	SPI	0	-	-	Carrier	Module	SPI1	Module	A	MAFS on Module LPC bus enabled
1	0	1	SPI	0	-	-	Module	Carrier	SPI0	Carrier	B	MAFS on Carrier LPC bus enabled
1	1	0	-	0	-	-	-	-	High	-	-	Not used - was FWH
1	1	1	SPI	0	-	-	Module	Module	High	Module	A	MAFS on Module LPC bus enabled
0	0	0	SPI	0	-	-	Carrier	Module	SPI1	Module	C	MAFS on Module ESPI bus enabled
0	0	1	SPI	0	-	-	Module	Carrier	SPI0	Carrier	D	MAFS on Carrier ESPI bus enabled
0	1	0	eSPI	1	Module	-	-	-	SPI0	Module	E	SAFS and BMC on Module ESPI bus enabled
0	1	1	eSPI	1	Carrier	Chipset ESPI_CS0#	-	-	SPI0	Carrier	F	SAFS and BMC on Carrier ESPI bus enabled

The BBS (BIOS Boot Select) is a signal to the chipset that indicates if the system is using a MAFS (Master Attached File Sharing) or SAFS (Slave attached File Sharing) setup. The BBS signal ***may*** be formed by Module logic looking for ESPI_EN# low and BIOS_DIS1# high.

The ESPI_CS1# line is not used for BIOS boot functions; it may be used to attach a secondary slave device to the eSPI bus, if the chip select is available.

SPI BIOS MAFS Considerations – LPC Enabled

The first four lines in Table Table 4.13 above are backwards compatible with the SPI BIOS options described in COM.0 Rev. 2, except that LPC FWH support is removed in COM.0 Rev 3. The LPC bus is enabled and is available for use on the Module or the Carrier for peripheral devices such as Board Management Controllers (BMC), Embedded Controllers (EC), Super I/O (SIO) or other general purpose devices.

SPI BIOS MAFS Considerations – eSPI Enabled

In an eSPI enabled MAFS system, the BIOS flash is attached to the system SPI bus, either on-Module or off-Module, much as in the LPC enabled MAFS system described above. The eSPI bus replaces the LPC bus for use with peripheral devices such as BMCs, ECs, SIOs etc. but the BIOS boot path is on the SPI bus.

eSPI BIOS SAFS Considerations – eSPI Enabled

In an eSPI enabled SAFS system, the SPI boot device is located on the far side of a BMC or EC. The system can boot from either a Module SAFS (E in Figure 4-5 above) or a Carrier SAFS (F in Figure 4-5 above). The BIOS boot traffic is routed through the BMC or EC to the system eSPI bus and on to the chipset.

It is possible for both a Module and a Carrier SAFS to be present in a system, but only one can be enabled. This is accomplished by routing the ESPI_CS0# signal to the Module or the Carrier, but never both. This is by definition of the eSPI specification. A second ESPI_CS1# is available to select eSPI slave devices. Slave devices can be on the Module or the Carrier. Two eSPI alert pins are provided. Additional alert pins are permitted by the eSPI specification through alert pin sharing on the EC/BMC or by signal tunneling.

4.3.14 Analog VGA

Analog RGB interface for CRT monitor and DDC support.

Table 4.14: VGA Signals, Pin Types, and Descriptions

Analog VGA	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
VGA_RED	O Analog	Analog	Red for monitor. Analog DAC output, designed to drive a 37 5Ω equivalent load.	T6
VGA_GRN	O Analog	Analog	Green for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	T6
VGA_BLU	O Analog	Analog	Blue for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	T6
VGA_HSYNC	O CMOS	3 3V / 3.3V	Horizontal sync output to VGA monitor	T6
VGA_VSYNC	O CMOS	3 3V / 3.3V	Vertical sync output to VGA monitor	T6
VGA_I2C_CK	I/O OD CMOS	3 3V / 3.3V	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	T6
VGA_I2C_DAT	I/O OD CMOS	3 3V / 3.3V	DDC data line.	T6

4.3.15 Digital Display Interfaces (DDI) - Module Type 6 and 10

Module Types 6 and 10 use Digital Display Interfaces (DDI) to provide DisplayPort and HDMI/DVI interfaces. Type 10 Modules can contain a single DDI (DDI[0]) that can support DisplayPort and HDMI/DVI. Type 6 Modules can support up to 3 DDIs (DDI[1:3]) which can support DisplayPort, HDMI/DVI, or dual DP / HDMI modes.
This specification leverages the work done by VESA to provide guidance on how a Carrier might support DP or HDMI/DVI from a DDI using a cable adapter to convert from DisplayPort to HDMI/DVI. Note that a Carrier can contain the same circuit that VESA shows in the cable adapter for a direct connect HDMI/DVI interface. The DisplayPort Interoperability Guideline Version 1.1a dated February 5, 2009 can be downloaded from the VESA website after registration at http://www.vesa.org/vesa-standards/free-standards. The VESA specification uses the term Dual-Mode Source to define a source that can be configured for DisplayPort or TMDS (HDMI/DVI) - this is equivalent to a Module DDI. Figure 4-6 shows a conceptual example circuit that could be used on a Module. Actual circuit implementations will vary.

Figure 4-6: Dual-Mode COM Express Module Implementation

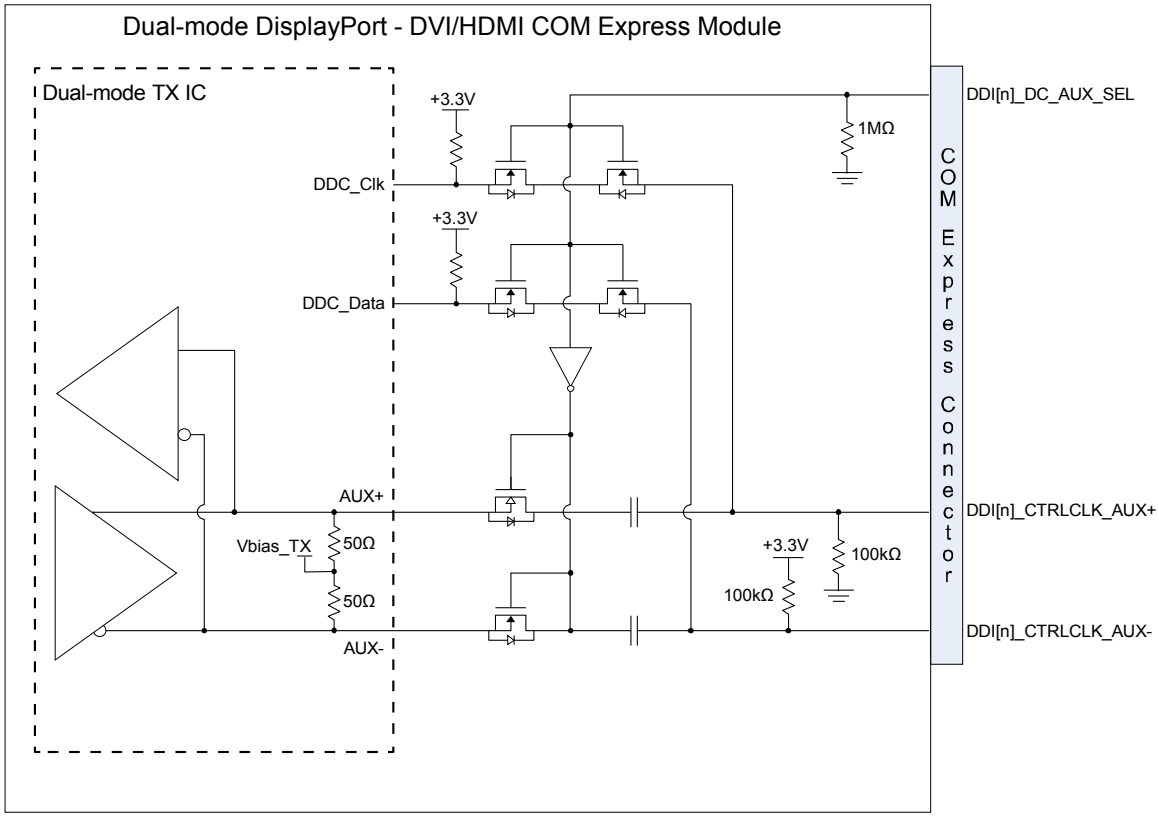


Table 4.15 'Module and Carrier Combinations' provides an idea of the type of circuit that

might be necessary for Carriers supporting DisplayPort, HDMI/DVI.

Table 4.15: Module and Carrier Combinations

Module	Carrier / Cable Adapter Requirements	Destination
DP only	None - Straight through to DP receptacle	DisplayPort
	N/A – not a valid combination	DVI/HDMI
DVI/HDMI	N/A – not a valid combination	DisplayPort
	None - Straight through to DVI/HDMI receptacle	DVI/HDMI
Dual Mode	None - Straight through to DP receptacle	DisplayPort
	Level shifters on DDC before DVI/HDMI connector. (Optional level shifters on data, per Module requirements.)	DVI/HDMI

Requirements

Module DDI[0:3] ***may*** support any combination of DisplayPort and DVI/HDMI.
Module DDI ports ***should*** support more than DVI/HDMI.
Modules that support Dual-Mode DDI interface ***shall*** implement the necessary muxing circuitry and control logic to ensure that the Module works properly with Carriers expecting DisplayPort or DVI/HDMI.
Modules ***shall*** meet the voltage and tolerance requirements as defined in the Signals, Pin Types, and Descriptions, Tables Table 4.16 and 4.17. This ***may*** require that a Module contain level shifters.

The pin map uses a generic name for the DDI pins. Table Table 4.18 below, details the mapping between the DDI pins and the different types of video interfaces supported.

Table 4.16: Type 6 DDI Signals, Pin Types, and Descriptions

DDI	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
DDI[1:3]_PAIR[0:3]+ DDI[1:3]_PAIR[0:3]-	O PCIE	AC coupled off Module	DDI 1 to 3 Pair[0:3] differential pairs	T6
DDI[1:3]_DDC_AUX_SEL	I CMOS	3.3V / 3.3V	Selects the function of DDI[1:3]_CTRLCLK_AUX+ and DDI[1:3]_CTRLDATA_AUX-. This pin ***shall*** have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	T6
DDI[1:3]_CTRLCLK_AUX+	I/O PCIE	AC coupled on Module	DP AUX+ function if DDI[1:3]_DDC_AUX_SEL is no connect	T6
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLCLK if DDI[1:3]_DDC_AUX_SEL is pulled high	T6
DDI[1:3]_CTRLDATA_AUX-	I/O PCIE	AC coupled on Module	DP AUX- function if DDI[1:3]_DDC_AUX_SEL is no connect	T6
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLDATA if DDI[1:3]_DDC_AUX_SEL is pulled high	T6
DDI[1:3]_HPD	I CMOS	3.3V / 3.3V	DDI Hot-Plug Detect	T6

Table 4.17: Type 10 DDI Signals, Pin Types, and Descriptions

DDI	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
DD 0_PAIR[0:3]+ DD 0_PAIR[0:3]-	O PCIE	AC coupled off Module	DDI 0 Pair[0:3] differential pairs	T10
DDI[0]_DDC_AUX_SEL	I CMOS	3.3V / 3.3V	Selects the function of DDI[0]_CTRLCLK_AUX+ and DDI[0]_CTRLDATA_AUX-. This pin ***shall*** have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	T10
DDI[0]_CTRLCLK_AUX+	I/O PCIE	AC coupled on Module	DP AUX+ function if DDI[0]_DDC_AUX_SEL is no connect	T10
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLCLK if DDI[0]_DDC_AUX_SEL is pulled high	T10
DDI[0]_CTRLDATA_AUX-	I/O PCIE	AC coupled on Module	DP AUX- function if DDI[0]_DDC_AUX_SEL is no connect	T10
	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C CTRLDATA if DDI[0]_DDC_AUX_SEL is pulled high	T10
DD 0_HPD	I CMOS	3.3V / 3.3V	DDI Hot-Plug Detect	T10

Table 4.18: Type 6 DDI

	Pin Name	Type 6 Pin Number	DP	HDMI/DVI (TMDS Signaling)
DDI 1	DDI1_PAIR0+	D26	DP1_LANE0+	TMDS1_DATA2+
	DDI1_PAIR0-	D27	DP1_LANE0-	TMDS1_DATA2-
	DDI1_PAIR1+	D29	DP1_LANE1+	TMDS1_DATA1+
	DDI1_PAIR1-	D30	DP1_LANE1-	TMDS1_DATA1-
	DDI1_PAIR2+	D32	DP1_LANE2+	TMDS1_DATA0+
	DDI1_PAIR2-	D33	DP1_LANE2-	TMDS1_DATA0-
	DDI1_PAIR3+	D36	DP1_LANE3+	TMDS1_CLK+
	DDI1_PAIR3-	D37	DP1_LANE3-	TMDS1_CLK-
	DDI1_PAIR4+	C25		
	DDI1_PAIR4-	C26		
	DDI1_PAIR5+	C29		
	DDI1_PAIR5-	C30		
	DDI1_PAIR6+	C15		
	DDI1_PAIR6-	C16		
	DDI1_HPD	C24	DP1_HPD	HDMI1_HPD
	DDI1_CTRLCLK_AUX+	D15	DP1_AUX+	HMDI1_CTRLCLK
	DDI1_CTRLDATA_AUX-	D16	DP1_AUX-	HMDI1_CTRLDATA
	DDI1_DDC_AUX_SEL	D34		
DDI 2	DDI2_PAIR0+	D39	DP2_LANE0+	TMDS2_DATA2+
	DDI2_PAIR0-	D40	DP2_LANE0-	TMDS2_DATA2-
	DDI2_PAIR1+	D42	DP2_LANE1+	TMDS2_DATA1+
	DDI2_PAIR1-	D43	DP2_LANE1-	TMDS2_DATA1-
	DDI2_PAIR2+	D46	DP2_LANE2+	TMDS2_DATA0+
	DDI2_PAIR2-	D47	DP2_LANE2-	TMDS2_DATA0-
	DDI2_PAIR3+	D49	DP2_LANE3+	TMDS2_CLK+
	DDI2_PAIR3-	D50	DP2_LANE3-	TMDS2_CLK-
	DDI2_HPD	D44	DP2_HPD	HDMI2_HPD
	DDI2_CTRLCLK_AUX+	C32	DP2_AUX+	HDMI2_CTRLCLK
	DDI2_CTRLDATA_AUX-	C33	DP2_AUX-	HDMI2_CTRLDATA
	DDI2_DDC_AUX_SEL	C34		
DDI 3	DDI3_PAIR0+	C39	DP3_LANE0+	TMDS3_DATA2+
	DDI3_PAIR0-	C40	DP3_LANE0-	TMDS3_DATA2-
	DDI3_PAIR1+	C42	DP3_LANE1+	TMDS3_DATA1+
	DDI3_PAIR1-	C43	DP3_LANE1-	TMDS3_DATA1-
	DDI3_PAIR2+	C46	DP3_LANE2+	TMDS3_DATA0+
	DDI3_PAIR2-	C47	DP3_LANE2-	TMDS3_DATA0-
	DDI3_PAIR3+	C49	DP3_LANE3+	TMDS3_CLK+
	DDI3_PAIR3-	C50	DP3_LANE3-	TMDS3_CLK-
	DDI3_HPD	C44	DP3_HPD	HDMI3_HPD
	DDI3_CTRLCLK_AUX+	C36	DP3_AUX+	HDMI3_CTRLCLK
	DDI3_CTRLDATA_AUX-	C37	DP3_AUX-	HDMI3_CTRLDATA
	DDI3_DDC_AUX_SEL	C38		

Table 4.19: Type 10 DDI

	Pin Name	Type 10 Pin Number	DP	HDMI/DVI (TMDS Signaling)
DDI 0	DDI0_PAIR0+	B71	DP0_LANE0+	TMDS0_DATA2+
	DDI0_PAIR0-	B72	DP0_LANE0-	TMDS0_DATA2-
	DDI0_PAIR1+	B73	DP0_LANE1+	TMDS0_DATA1+
	DDI0_PAIR1-	B74	DP0_LANE1-	TMDS0_DATA1-
	DDI0_PAIR2+	B75	DP0_LANE2+	TMDS0_DATA0+
	DDI0_PAIR2-	B76	DP0_LANE2-	TMDS0_DATA0-
	DDI0_PAIR3+	B81	DP0_LANE3+	TMDS0_CLK+
	DDI0_PAIR3-	B82	DP0_LANE3-	TMDS0_CLK-
	DDI0_PAIR4+	B77		
	DDI0_PAIR4-	B78		
	DDI0_PAIR5+	B91		
	DDI0_PAIR5-	B92		
	DDI0_PAIR6+	B93		
	DDI0_PAIR6-	B94		
	DDI0_HPD	B89	DP0_HPD	HDMI0_HPD
	DDI0_CTRLCLK_AUX+	B98	DP0_AUX+	HMDI0_CTRLCLK
	DDI0_CTRLDATA_AUX-	B99	DP0_AUX-	HMDI0_CTRLDATA
	DDI0_DDC_AUX_SEL	B95		

4.3.16 DDI Signals: DisplayPort

Table 4.20: DisplayPort Signals, Pin Types, and Descriptions

DisplayPort	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
DP[1:3]_LANE[0:3]+ DP[1:3]_LANE[0:3]-	O PCIE	AC coupled off Module	Uni-directional main link for the transport of isochronous streams and secondary-data packets	T6
DP[1:3]_AUX+ DP[1:3]_AUX-	I/O PCIE	AC coupled on Module	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	T6
DP[1:3]_HPD	I CMOS	3.3V / 3.3V	Detection of Hot Plug / Unplug and notification of the link layer	T6
DP[0]_LANE[0:3]+ DP[0]_LANE[0:3]-	O PCIE	AC coupled off Module	Uni-directional main link for the transport of isochronous streams and secondary-data packets	T10
DP[0]_AUX+ DP[0]_AUX-	I/O PCIE	AC coupled on Module	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	T10
DP[0]_HPD	I CMOS	3.3V / 3.3V	Detection of Hot Plug / Unplug and notification of the link layer	T10

4.3.17 DDI Signals: HDMI / DVI

Table 4.21: HDMI/DVI Signals, Pin Types, and Descriptions

HDMI	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
TMDS[1:3]_CLK+ TMDS[1:3]_CLK-	O PCIE	AC coupled off Module	HDMI/DVI TMDS Clock differential pair	T6
TMDS[1:3]_DATA[0:2]+ TMDS[1:3]_DATA[0:2]-	O PCIE	AC coupled off Module	HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs	T6
HDMI[1:3]_CTRL_CLK	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control clock	T6
HDMI[1:3]_CTRL_DAT	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control data	T6
HDMI[1:3]_HPD	I	3.3V / 3.3V	HDMI/DVI Hot-Plug Detect	T6
TMDS[0]_CLK+ TMDS[0]_CLK-	O PCIE	AC coupled off Module	HDMI/DVI TMDS Clock differential pair	T10
TMDS[0]_DATA[0:2]+ TMDS[0]_DATA[0:2]-	O PCIE	AC coupled off Module	HDMI/DVI TMDS lanes 0, 1 and 2 differential pairs	T10
HDMI[0]_CTRL_CLK	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control clock	T10
HDMI[0]_CTRL_DAT	I/O OD CMOS	3.3V / 3.3V	HDMI/DVI I2C control data	T10
HDMI[0]_HPD	I	3.3V / 3.3V	HDMI/DVI Hot-Plug Detect	T10

4.3.18 General Purpose Serial Interface

Two TTL compatible two wire asynchronous serial ports are available on Module Types 6, 7 and 10. This feature was introduced in COM.0 Revision 2 and uses pins on the A-B connector that have been re-claimed from the A-B VCC_12V pool. As such, it is possible that if a Type 6, 7, or 10 Module is deployed in an R1.0 Carrier Board designed for Module Types 1,2,3,4,5 then the Module TTL level serial pins may be exposed to the 12V supply, and Module designers must plan for this. Similarly, an R1.0 Module deployed on an R2.0 Carrier may bridge 12V to the serial pins and Carrier designers must plan for this. These pins are designated SER0_TX, SER0_RX, SER1_TX and SER1_RX. Data out of the Module is on the _TX pins. Hardware handshaking and hardware flow control are not supported.

Any of the Module asynchronous serial ports, if implemented on an Intel X86 architecture Module platform, ***should*** be I/O mapped serial ports that are register compatible with the National Semiconductor 16550 UARTs that were used in the PC AT architecture.

The Module asynchronous serial ports are intended for general purpose use and for use with debugging software that make use of the “console redirect” features available in many operating systems. The Module asynchronous serial ports ***should not*** be implemented as USB peripherals, as such implementations are generally not useful for low level debug purposes.

Table 4.22: Serial Interface Signals (Type 10), Pin Types, and Descriptions

Serial	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SER0_TX[4]	O CMOS-T	3.3V / 12V	General purpose serial port transmitter	All
SER0_RX[4]	I CMOS-T	3.3V / 12V	General purpose serial port receiver	All
SER1_TX[4]	O CMOS-T	3.3V / 12V	General purpose serial port transmitter This pin is shared with CAN_TX (refer to Section 4 3.30 'CAN Bus')	All
SER1_RX[4]	I CMOS-T	3.3V / 12V	General purpose serial port receiver This pin is shared with CAN_RX (refer to Section 4.3.30 'CAN Bus')	All

4 *These signals use reclaimed VCC_12V pins. Refer to Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations*

4.3.19 I2C Bus

The I2C port ***shall*** be available in addition to the SMBus. The I2C clock ***shall*** support 100kHz and ***should*** support 400kHz operation. The maximum capacitance on the Carrier Board ***shall*** not exceed 100pF. The I2C interface ***should*** support multi-master operation.[5] This capability will allow a Carrier to read an optional Module EEPROM before powering up the Module.

Revision 1.0 of the specification placed the I2C interface on the non-standby power domain. With this connection, the I2C interface can only be used when the Module is powered on. Since the I2C interface is used to connect to an optional Carrier EEPROM and since it is desirable to allow a Module based board controller access to the optional Carrier EEPROM before the Module is powered on, revision 2.0 of this specification changes the power domain of the I2C interface to standby-power allowing access during power down and suspend states. There is a possible leakage issue that can arise when using a R2.0 Module with a R1.0 Carrier that supports I2C devices. The R1.0 Carrier will power any I2C devices from the non-standby power rail. A R2.0 Module will pull-up the I2C clock and data lines to the standby-rail through a 2.2K resistor. The difference in the power domains on the Module and Carrier can provide a leakage path from the standby power rail to the non-standby power rail.

Table 4.23: I2C Signals, Pin Types, and Descriptions

I2C Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
I2C_CK	I/O OD CMOS	3.3V Suspend/ 3.3V	General purpose I2C port clock output	All
I2C_DAT	I/O OD CMOS	3.3V Suspend/ 3.3V	General purpose I2C port data I/O line	All

5 *I2C multi-master support starts with COM Express Rev. 2.0*

4.3.20 Miscellaneous

Table 4.24: Misc Signals, Pin Types, and Descriptions

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SPKR	O CMOS	3.3V / 3.3V	Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.	All
WDT	O CMOS	3.3V / 3.3V	Output indicating that a watchdog time-out event has occurred. Refer to Section 5.7 'Watchdog Timer' on page 115 for details.	All
FAN_PWMOUT[6]	O OD CMOS	3.3V / 12V	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	All
FAN_TACHIN[6]	I OD CMOS	3.3V / 12V	Fan tachometer input for a fan with a two pulse output.	All
TPM_PP[6]	I CMOS	3.3V / 3.3V	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	All

6 *These signals use reclaimed VCC_12V pins. Refer to Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations*

4.3.21 Power and System Management

Signals PWR_OK, SYS_RESET#, and CB_RESET# ***shall*** be supported for all Module pin-out types. Signal PCI_RESET# ***shall*** be supported for pin-out types 2 and 3. Signal IDE_RESET# ***shall*** be supported for pin-out types 2 and 4. Additionally, signal PWR_OK indicates that all the power supplies to the Module are stable within specified ranges and can be used to enable Module internal power supplies.
PWR_OK has been traditionally used to hold off a Module startup to allow devices on the Carrier such as FPGAs to initialize. The Module will typically not power up until the PWR_OK signal goes active. There is the potential for the Carrier to back drive voltages from the Carrier to the Module when the Carrier is powered but the Module is not. Designers of Modules and Carrier are encourage to follow the terminations as specified in Section 4.4 'Signals Requiring Carrier Board Termination'. The use of SYS_RESET# to hold off a Module startup may not produce the desired results since the behavior of SYS_RESET# is Module chipset dependent. In typical designs, the reset initiation happens on the falling edge of SYS_RESET# therefore holding the SYS_RESET# low will not result in preventing the Module for starting. PWR_OK ***should not*** be deactivated after the Module enters S0 unless there is a power fail condition.

Signals SUS_S3#, SUS_S4# and SUS_S5# define the signaling to indicate that the Module has entered the ACPI power-saving mode S3 (Suspend-To-RAM or STR), S4 (Suspend-To-Disk or STD), or S5 (Soft-Off).

Table 4.25: Power and System Management Signals, Pin Types, and Descriptions

Power and System Management	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PWRBTN#	I CMOS	3.3V Suspend/ 3 3V	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	All
SYS_RESET#	I CMOS	3.3V Suspend/ 3 3V	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle ***may*** be used.	All
CB_RESET#	O CMOS	3.3V Suspend/ 3 3V	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and ***may*** result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or ***may*** be initiated by the Module software.	All
PWR_OK	I CMOS	3.3V / 3.3V	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.	All
SUS_STAT#	O CMOS	3.3V Suspend/ 3 3V	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations.	All
SUS_S3#	O CMOS	3.3V Suspend/ 3 3V	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board ***may*** be used to enable the non-standby power on a typical ATX supply.	All
SUS_S4#	O CMOS	3.3V Suspend/ 3 3V	Indicates system is in Suspend to Disk state. Active low output.	All
SUS_S5#	O CMOS	3.3V Suspend/ 3 3V	Indicates system is in Soft Off state.	All
WAKE0#	I CMOS	3.3V Suspend/ 3 3V	PCI Express wake up signal.	All
WAKE1#	I CMOS	3.3V Suspend/ 3 3V	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	All
BATLOW#	I CMOS	3.3V Suspend/ 3 3V	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	T6,T10
			In a type 7 system, BATLOW# can be used as a power fail indication.	T7
LID#[7]	I OD CMOS	3.3V Suspend/ 12V	LID switch. Low active signal used by the ACPI operating system for a LID switch.	All
SLEEP#[7]	I OD CMOS	3.3V Suspend/ 12V	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	All

7 *These signals use reclaimed VCC_12V pins. Refer to Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations*

4.3.22 Rapid Shutdown

COM Express Modules ***may*** support rapid shutdown. On a Module equipped with rapid shutdown, the assertion of the RAPID_SHUTDOWN input will cause the internal power supply regulators on the Module to be disabled, and for all residual voltages on the internal power supply rails to be discharged through crowbar circuits.

Table 4.26: Rapid Shutdown Signal

Rapid Shutdown	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
RAPID_SHUTDOWN	I CMOS	5.0V Suspend/ 5.0V	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.	T6,T7

Modules supporting rapid shutdown ***shall*** specify the power rail discharge behavior, including discharge time constants and end-of-discharge voltages. An example of such a specification is “all internal power supply rails must decay to 37% of initial value within 300uS of RAPID_SHUTDOWN assertion, and to a voltage below 1.5V within 2mS of RAPID_SHUTDOWN assertion.”

A rapid shutdown implementation also requires supporting circuitry on the Carrier Board. Upon the assertion of RAPID_SHUTDOWN, the 12V (main) input power to the Module ***shall*** be removed by Carrier board circuitry and the input power pins ***shall*** be externally clamped to ground though a crowbar circuit located on the Carrier Board. This clamping circuit ***shall*** maintain a maximum resistance of 1 ohm and ***shall*** be active for a minimum of 2mS following the rise of RAPID_SHUTDOWN. The Module ***shall*** be designed with sufficiently low input capacitance to allow the input discharge specification to be met with a 1 ohm discharge resistance.

The Module design ***should*** prevent overheating or damage to any Module circuitry in the event that RAPID_SHUTDOWN is asserted without the removal of input power. This condition could occur due to malfunction of the Carrier Board support circuitry, or if the RAPID_SHUTDOWN signal is inadvertently asserted when the Module is installed on a Carrier Board that does not implement rapid shutdown support circuitry.

In some system implementations the power for both the Module and Carrier Board will fail shortly after the RAPID_SHUTDOWN signal is asserted. Therefore, the driving source for the RAPID_SHUTDOWN pin typically must charge an RC circuit on the Module that maintains crowbar assertion for several milliseconds following power failure. In order to charge this RC circuit rapidly, the RAPID_SHUTDOWN signal ***shall*** be sourced from a source impedance of 50 ohms or less. The RAPID_SHUTDOWN signal also ***shall*** have a rise time of <=1us and ***shall*** have a duration of >=20 uS. If the same RAPID_SHUTDOWN signal source is used to drive the Carrier Board input clamp circuitry, then any additional load from that Carrier Board circuitry needs to be considered in its design.

4.3.23 Thermal Protection

This port provides thermal signaling to protect critical components on the Module and the Carrier Board.

Table 4.27: Thermal Protection Signals, Pin Types, and Descriptions

Thermal Protection	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
THRM#	I CMOS	3.3V / 3.3V	Input from off-Module temp sensor indicating an over-temp situation.	All
THRMTRIP#	O CMOS	3.3V / 3.3V	Active low output indicating that the CPU has entered thermal shutdown.	All

4.3.24 SM Bus

The SMBus port is specified for system management functions. It is used on the Module to manage system functions such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. If the SMBus is used on the baseboard, then great care must be taken that no conflicts with the on-Module SMBus devices occur. It may be useful for implementation on the Carrier Board of standards such as Smart Battery. The maximum capacitance on the Carrier Board ***shall*** not exceed 100pF.

Table 4.28: SM Bus Signals, Pin Types, and Descriptions

SM Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SMB_CK	I/O OD CMOS	3.3V Suspend/ 3.3V	System Management Bus bidirectional clock line.	All
SMB_DAT	I/O OD CMOS	3.3V Suspend/ 3.3V	System Management Bus bidirectional data line.	All
SMB_ALERT#	I CMOS	3.3V Suspend/ 3.3V	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	All

4.3.25 General Purpose Input Output

GPI and GPO pins ***may*** be implemented as GPIO (Module specific). GPI and GPO pins ***may*** be implemented as SDIO (refer to Section 4.3.26 'SDIO'). If SDIO is supported the BIOS **may** be used to set the default state (SDIO or GPIO) of the GPIO.

Table 4.29: GPIO Signals, Pin Types, and Descriptions

General Purpose I/O	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
GPO[0:3]	O CMOS	3.3V / 3.3V	General purpose output pins. Upon a hardware reset, these outputs ***should*** be low.	All
GPI[0:3]	I CMOS	3.3V / 3.3V	General purpose input pins. Pulled high internally on the Module.	All

4.3.26 SDIO

Support for an SDIO interface is optional and added in R2.0. The SDIO signals are piggy-backed on the existing COM.0 General Purpose IO (GPIO) signals (refer to Section 4.3.25 'General Purpose Input Output'). An EEPROM bit is added so that the Carrier Board can define if the GPIO are used as GPIO or SDIO. The Module ***may*** use this information to allow boot from SDIO. Modules that support SDIO over GPIO ***shall*** implement the pin mapping based on the table below.

Table 4.30: SD Card Interface Signals

COM Express Signal	SD card interface signals	Comments
GPI0	SD_DATA0	Bidirectional signal
GPI1	SD_DATA1	Bidirectional signal
GPI2	SD_DATA2	Bidirectional signal
GPI3	SD_DATA3	Bidirectional signal
GPO0	SD_CLK	Output from COM Express, input to SD
GPO1	SD_CMD	Output from COM Express, input to SD
GPO2	SD_WP	Input to COM Express when used as SD_WP
GPO3	SD_CD#	Input to COM Express when used as SD_CD#

Table 4.31: SDIO Signals, Pin Types, and Descriptions

SDIO	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SDIO_CD#	I CMOS	3 3V / 3.3V	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support.	All
SDIO_CLK	O CMOS	3 3V / 3.3V	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.	All
SDIO_CMD	O CMOS	3 3V / 3.3V	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1.	All
SDIO_WP	I CMOS	3 3V / 3.3V	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support.	All
SDIO_DAT[0:3]	IO CMOS	3 3V / 3.3V	SDIO Data lines. These signals operate in push-pull mode. Maps to GPI[0:3].	All

4.3.27 Module Type Definition

Table 4.32: Module Type Signals, Pin Types, and Descriptions

<table>
<tr><th>Module Type Definition</th><th>Pin Type</th><th>Pwr Rail / Tolerance</th><th>Description</th><th>Pin Availability</th></tr>
<tr><td>TYPE[0:2]#</td><td>PDS</td><td></td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X).

<table>
<tr><td>TYPE2#</td><td>TYPE1#</td><td>TYPE0#</td><td></td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>Pin-out Type 10,
Pin-out Type 1 (deprecated)</td></tr>
<tr><td>NC</td><td>NC</td><td>NC</td><td>Pin-out Type 2 (deprecated)</td></tr>
<tr><td>NC</td><td>NC</td><td>GND</td><td>Pin-out Type 3 (deprecated)</td></tr>
<tr><td>NC</td><td>GND</td><td>NC</td><td>Pin-out Type 4 (deprecated)</td></tr>
<tr><td>NC</td><td>GND</td><td>GND</td><td>Pin-out Type 5 (deprecated)</td></tr>
<tr><td>GND</td><td>NC</td><td>NC</td><td>Pin-out Type 6</td></tr>
<tr><td>GND</td><td>NC</td><td>GND</td><td>Pin-out Type 7</td></tr>
</table>

The Carrier Board ***should*** implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin-out type is detected. The Carrier Board logic ***may*** also implement a fault indicator such as an LED.</td><td>T6,T7</td></tr>
<tr><td>TYPE10#</td><td>PDS</td><td></td><td>Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0 or a Rev 2.0/3.0 Module is installed.

<table>
<tr><td>TYPE10#</td><td></td></tr>
<tr><td>NC</td><td>Pin-out R2.0</td></tr>
<tr><td>PD</td><td>Pin-out Type 10 pull down to ground with 47K resistor</td></tr>
<tr><td>12V</td><td>Pin-out R1.0</td></tr>
</table>

This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2 0 this pin is defined as a no connect for types 1-6. In R3.0 this pin is defined as a no connect for types 6 and 7. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. R3 0 Module types 6 and 7 will no connect this pin. Type 10 Modules ***shall*** pull this pin to ground through a 47K resistor.</td><td>All</td></tr>
</table>

4.3.28 Power and Ground

Table 4.33: Power Signals, Pin Types, and Descriptions

Power and GND	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
VCC_12V	Power		Primary power input: +12V nominal. Refer to Section 7 "Electrical Specifications" for allowable input range. All available VCC_12V pins on the connector(s) ***shall*** be used.	All
VCC_5V_SBY	Power		Standby power input: +5.0V nominal. Refer to Section 7 "Electrical Specifications" for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) ***shall*** be used. Only used for standby and suspend functions. ***May*** be left unconnected if these functions are not used in the system design.	All
VCC_RTC	Power		Real-time clock circuit-power input. Nominally +3 0V. Refer to Sec ion 7 "Electrical Specifications" for details.	All
GND	Power		Ground - DC power and signal and AC signal return path. All available GND connector pins ***shall*** be used and tied to Carrier Board GND plane.	All

4.3.29 eDP - Embedded DisplayPort

Type 6 and Type 10 Modules allow the LVDS channel A signals (refer to Section 4.3.10 'LVDS Flat Panel') to be alternatively used for eDP. The manner in which LVDS or eDP operation is chosen is vendor dependent.

Table 4.34: Module and Carrier Combinations Type 6 and Type 10 Modules

Module	Carrier / Panel Adapter Requirements	Destination
eDP only	None - Straight through to eDP Header	eDP
	N/A – not a valid combination	LVDS
LVDS only	N/A – not a valid combination	eDP
	None - Straight through to LVDS receptacle	LVDS
Dual Mode	None - Straight through to eDP receptacle	eDP
	None – Straight through to LVDS receptacle	LVDS

Requirements

Module LVDS Channel A/eDP ***may*** support any combination of LVDS and eDP.
Module LVDS Channel A/eDP ***may*** support Dual Mode.
Module that support Dual-Mode ***shall*** implement the necessary muxing circuitry and control logic to ensure that the Module works properly with Carriers expecting either eDP or LVDS.

Table 4.35: eDP Signals

eDP	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
eDP_TX[0:3]+ eDP_TX[0:3]-	O PCIE	AC coupled off Module	eDP differential pairs	T6, T10
eDP _VDD_EN	O CMOS	3.3V / 3.3V	eDP power enable	T6,T10
eDP _BKLT_EN	O CMOS	3.3V / 3.3V	eDP backlight enable	T6,T10
eDP _BKLT_CTRL	O CMOS	3.3V / 3.3V	eDP backlight brightness control	T6,T10
eDP _AUX+	I/O PCIE	AC coupled off Module	eDP AUX+	T6,T10
eDP _AUX-	I/O PCIE	AC coupled off Module	eDP AUX-	T6,T10
eDP_HPD	I CMOS	3.3V / 3.3V	Detection of Hot Plug / Unplug and notification of the link layer	T6,T10

The off Module AC coupling of the eDP signals makes dual LVDS/eDP Module implementations easier.

Table 4.36: LVDS / eDP Pin Assignment

Pin Name	Type 6/10 Pin Number	eDP
LVDS_A0+	A71	eDP_TX2+
LVDS_A0-	A72	eDP_TX2-
LVDS_A1+	A73	eDP_TX1+
LVDS_A1-	A74	eDP_TX1-
LVDS_A2+	A75	eDP_TX0+
LVDS_A2-	A76	eDP_TX0-
LVDS_A_CK+	A81	eDP_TX3+
LVDS_A_CK-	A82	eDP_TX3-
LVDS_VDD_EN	A77	eDP_VDD_EN
LVDS_BKLT_EN	B79	eDP_BKLT_EN
LVDS_I2C_CK	A83	eDP_AUX+
LVDS_I2C_DAT	A84	eDP_AUX-
LVDS_BKLT_CTRL	B83	eDP_BKLT_CTRL
RSVD	A87	eDP_HPD

4.3.30 CAN Bus

CAN Bus Operation Over SER1 Lines

The SER1_TX and SER1_RX asynchronous serial port lines defined for COM.0 Types 6, 7 and 10 ***may*** be used alternatively to carry CMOS 3.3V logic level CAN (Controller Area Network) bus signals from a COM Express Module based CAN protocol controller. The CAN bus is an asynchronous, message based protocol widely used in the automotive and industrial control sectors. It is defined by ISO 11519, ISO 11898, and SAEJ2411. Data rates on a CAN bus ***may*** be as high as 1 MBit/s, although lower rates in the range from 10 kBit/s to 125 kBit/s are more common. The achievable data rates are dependent on the protection scheme used see Section 5.8 for further information.

Use of the CAN bus in a COM Express system requires a CAN bus transceiver on the Carrier Board to interface to the CAN physical layer. CAN bus transceivers are available from NXP, Texas Instruments, Linear Technology, and others.

Data from the COM Express Module based CAN controller to the Carrier Board CAN transceiver is carried on Module line SER1_TX. Data from the Carrier Board CAN transceiver to the COM Express Module based CAN controller is carried on Module line SER1_RX. The Carrier Board CAN transceiver converts the logic level CAN protocol TX and RX signals from the Module into a differential half duplex line per the CAN specification.

How the SER1 asynchronous lines are shared with CAN bus operation is Module vendor specific. A vendor ***may*** choose to use the SER1 TX and RX lines to support asynchronous serial port operation, or CAN bus operation, or both, or neither. Module build option(s) or software controlled muxing implementations ***may*** be used.

Table 4.37: CAN Bus Signals

CAN Bus	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
CAN_TX[8]	O CMOS	3.3V / 12V	CAN (Controller Area Network) TX output for CAN Bus channel 0. This pin is shared with SER1_TX (refer to Section 4.3.18 'General Purpose Serial Interface')	All
CAN_RX[8]	I CMOS	3.3V / 12V	RX input for CAN Bus channel 0. This pin is shared with SER1_RX (refer to Section 4 3.18 'General Purpose Serial Interface')	All

8 *These signals use reclaimed VCC_12V pins. Refer to Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations*

4.4 Signals Requiring Carrier Board Termination

Some signals, detailed below, require Carrier Board termination for proper operation. If the signals and the feature are not used, no Carrier Board termination is required, and the pins ***may*** be left open.

4.4.1 Ethernet

External Ethernet magnetics ***shall*** be implemented on the Carrier Board.

4.4.2 Analog VGA

If analog VGA is used, the VGA_RED, VGA_GRN, and VGA_BLU signals ***shall*** each be terminated on the Carrier Board through a 150Ω resistor to ground. These resistors ***should*** be placed close to the VGA connector on the Carrier Board. These lines ***may*** be left unterminated if the analog VGA function is not used.

4.4.3 LVDS

The LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) ***shall*** have 100Ω terminations across the pairs at the destination. These terminations ***may*** be on the Carrier Board if the Carrier Board implements a LVDS de-serializer on-board.
Unused LVDS lines ***may*** be left open.

4.4.4 USB

No termination is required on USB pairs. A common mode choke is advisable if USB pairs on the Carrier Board are routed to a connector for use with an external cable. Signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# are used to flag a USB over-current situation. Carrier Board USB current monitors ***may*** pull these lines to GND with open drain drivers to indicate that the monitor's current limit has been exceeded. Do not pull up these lines to 3.3V on the Carrier Board – this ***shall*** be done on the Module (Section 4.5.2).
If a USB 2.0 Debug port is present it ***should*** be routed to port 0.

4.4.5 Digital Display Interfaces (DDI)

The Carrier based termination requirements are dependent on the video interfaces supported by the Module's DDI implementation as well as the display type connected to the Carrier. A DDI can be used to support one or more of the following interfaces: DP, TMDS(DVI/HDMI), or Dual-Mode (DisplayPort and TMDS). Refer to the VESA DisplayPort Interoperability Guideline Version 1.1a dated February 5, 2009 available at the VESA website after registration http://www.vesa.org/vesa-standards/ for more information on supporting TMDS (DVI/HDMI) from a Dual-Mode Module.

Carriers that support TMDS (DVI/HDMI):

- DDI[n]_DDC_AUX_SEL ***shall*** be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel.
- Bi-directional level translators ***shall*** be placed on the Carrier DDI[n]_CTRLDATA_AUX- and DDI[n]_CTRLCLK_AUX+ to convert the 3.3V DDC channel on the Module to the 5V DDC channel for the TMDS display.
- Pull-up resistors ***shall*** be placed on the Carrier from 3.3V (Module side of level translator) and 5V (display side of level translator) and the [n]_CTRLDATA_AUX- and DDI[n]_CTRLCLK_AUX+ signals. The pull-up resistor ***should*** be 2k.
- Level translators ***may*** be placed on the DDI[n]_PAIR[0:3] signals if required by Module silicon. If such level translators are implemented, they ***shall*** be placed on the Carrier Board.
- Some Modules ***may*** require DC blocking capacitors on DDI[n]_PAIR[0:3]. If DC blocking capacitors are required by the DDI generating silicon, the DC blocking capacitors ***shall*** be placed on the Carrier.
- The Carrier ***shall*** include a blocking FET on DDI[n]_HPD to prevent back-drive current from damaging the Module.

Carriers that support DisplayPort (DisplayPort only or dual mode):

- Carrier DDI[n]_DDC_AUX_SEL ***should*** be connected to pin 13 of the DisplayPort connector to enable Modules that can support a Dual-Mode DisplayPort interface.
- DC blocking capacitors ***shall*** be placed on the Carrier for the DDI[n]_PAIR[0:3] signals.
- The Carrier ***shall*** include a blocking FET on DDI[n]_HPD to prevent back-drive current from damaging the Module.

4.4.6 VCC_RTC

To implement the RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series low-leakage diode and/or a series resistor. Revision 1.0 of this specification did not specify the location of this diode and the location was vendor implementation specific. For revision 2.0 Carrier Boards, a protection diode or a series resistor ***shall*** be placed on the Carrier Board. For backwards compatibility, a revision 2.0 Module ***may*** also implement the protection diode.

Note: If a Schottky diode is used, the leakage current must not exceed the UL requirement of the battery, especially at the temperature limits.

4.4.7 EMI and ESD Mitigation

Carrier board designers ***should*** take proper precautions to minimize EMI and maximize ESD protection on external connectors.

4.5 Signals Requiring Module Termination

The signals below require Module termination if used. They are mentioned to provide guidance to both the Module and Carrier designer. These terminations defined below ***may*** be omitted if the feature is not implemented on the Module.

4.5.1 AC coupled on the Module

The following signals ***shall*** be AC coupled on the Module.

- SATA[0:3]TX+/-
- SATA[0:3]RX+/-
- PCIE_TX[0:31]+/-
- PEG_TX[0:15]+/-
- USB_SSTX[0:3]+/-
- 10G_KR_RX[0:3]+/-

4.5.2 Misc

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 2.2kΩ resistor.

- LVDS_I2C_CK
- LVDS_I2C_DAT
- VGA_I2C_CK
- VGA_I2C_DAT

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 8.2kΩ resistor.

- LPC_SERIRQ

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V with a 10kΩ resistor.

- BIOS_DIS[0:1]#

The Module ***shall*** provide the termination for the signal below. The following signal ***should*** be pulled-up to 3.3V with a 47kΩ resistor.

- FAN_TACHIN

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V Standby with a 2.2kΩ resistor.

- I2C_CK
- I2C_DAT
- SMB_CK
- SMB_DAT
- 10G_PHY_MDIO_SDA[0:3]
- 10G_PHY_MDC_SCL[0:3]
- 10G_SFP_SDA[0:3]
- 10G_SFP_SCL[0:3]
- 10G_LED_SDA
- 10G_LED_SCL
- 10G_INT[0:3]

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V Standby with a 10kΩ resistor.

- USB_[0,2,4,6]_[1,3,5,7]_OC#
- SYS_RESET#
- BATLOW#
- WAKE0#
- WAKE1#
- PWRBTN#
- 10G_PHY_CAP_01
- 10G_PHY_CAP_23

- NCSI_ARB_IN

The Module ***shall*** provide the termination for the signals below. The following signals ***should*** be pulled-up to 3.3V Standby with a 47kΩ resistor.

- SLEEP#
- LID#

The Module ***shall*** provide termination for the signal below. The following signal ***should*** be pulled-up to 1.8V with a 1K resistor.

- ESPI_ALERT0#
- ESPI_ALERT1#

The Module ***shall*** provide termination for the signal below. The following signal ***should*** be pulled-down with a 10K resistor.

- NCSI_CLK_IN
- NCSI_TXD[0:1]
- NCSI_TX_EN

The Module ***shall*** provide termination for the signal below. The following signal ***should*** be pulled to a logic high with a 20K resistor.

- ESPI_EN#

When supporting Carrier Board based SPI devices, the SPI_MISO line ***shall*** have a series resistor of 33Ω on the Module.

Modules implementing a TPM ***shall*** pull down TPM_PP. The value of the pull down resistor will be Module specific. Carrier Boards that support TPM ***should*** drive this signal to 3.3V when TPM features that require physical presence detection are implemented.

The PWR_OK signal ***should*** be terminated by the Module. If the signal is driven low by the Carrier Board the Module power supplies do not start. If the signal is floated or driven to 3.3V logic high by the Carrier Board, and Module hardware determines that the incoming power is good then the Module power supplies proceed with their start up.

4.6 Pin-out Tables

Pin-out information for Module pin-out Types 6, 7 and 10 are provided in the tables on the following pages.

4.6.1 Type 10

Module Pin-out Type 10 implements a single 220-pin connector and a minimal feature set including up to 4 PCI Express lanes, up to 2 USB SuperSpeed, up to 8 USB, a USB client host detect, up to 2 SATA, LPC, eSPI, single LVDS, 1 DDI, SPI, power management and miscellaneous functions. Modules implementing Pin-out Type 10 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.3 for the order in which interfaces ***shall*** be implemented.

Table 4.38: Pin List for Pin-Out Type 10

Pin	Row A	Row B
1	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#/ESPI_CS0#
4	GBE0_LINK100#	LPC_AD0/ESPI_IO_0
5	GBE0_LINK1000#	LPC_AD1/ESPI_IO_1
6	GBE0_MDI2-	LPC_AD2/ESPI_IO_2
7	GBE0_MDI2+	LPC_AD3/ESPI_IO_3
8	GBE0_LINK#	LPC_DRQ0#/ESPI_ALERT0#
9	GBE0_MDI1-	LPC_DRQ1#/ESPI_ALERT1#
10	GBE0_MDI1+	LPC_CLK/ESPI_CK
11	GND(FIXED)	GND(FIXED)
12	GBE0_MD 0-	PWRBTN#
13	GBE0_MD 0+	SMB_CK
14	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#/ESPI_RESET#
19	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)
22	USB_SSRX0-	USB_SSTX0-
23	USB_SSRX0+	USB_SSTX0+
24	SUS_S5#	PWR_OK
25	USB_SSRX1-	USB_SSTX1-
26	USB_SSRX1+	USB_SSTX1+
27	BATLOW#	WDT
28	(S)ATA_ACT#	HDA_SDIN2
29	HDA_SYNC	HDA_SDIN1
30	HDA_RST#	HDA_SDIN0
31	GND(FIXED)	GND(FIXED)
32	HDA_BITCLK	SPKR
33	HDA_SDOUT	I2C_CK
34	BIOS_DIS0#/ESPI_SAFS	I2C_DAT
35	THRMTRIP#	THRM#
36	USB6-	USB7-

Pin	Row A	Row B
37	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-
40	USB4+	USB5+
41	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-
43	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-
46	USB0+	USB1+
47	VCC_RTC	ESPI_EN#
48	RSVD[9]	USB0_HOST_PRSNT
49	GBE0_SDP	SYS_RESET#
50	LPC_SERIRQ/ESPI_CS1#	CB_RESET#
51	GND(FIXED)	GND(FIXED)
52	RSVD[9]	RSVD[9]
53	RSVD[9]	RSVD[9]
54	GPI0	GPO1
55	RSVD[9]	RSVD[9]
56	RSVD[9]	RSVD[9]
57	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#
67	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	DD 0_PAIR0+
72	LVDS_A0-	DD 0_PAIR0-
73	LVDS_A1+	DD 0_PAIR1+
74	LVDS_A1-	DD 0_PAIR1-
75	LVDS_A2+	DD 0_PAIR2+
76	LVDS_A2-	DD 0_PAIR2-
77	LVDS_VDD_EN	DD 0_PAIR4+
78	LVDS_A3+	DD 0_PAIR4-
79	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	DD 0_PAIR3+
82	LVDS_A_CK-	DD 0_PAIR3-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY
86	RSVD	VCC_5V_SBY
87	eDP_HPD	VCC_5V_SBY
88	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	DDI0_HPD
90	GND(FIXED)	GND(FIXED)

9 RSVD pins are reserved for future use and ***should*** be no connect. Do not tie the RSVD pins together.

Pin	Row A	Row B
91	SPI_POWER	DD 0_PAIR5+
92	SPI_MISO	DD 0_PAIR5-
93	GPO0	DD 0_PAIR6+
94	SPI_CLK	DD 0_PAIR6-
95	SPI_MOSI	DD 0_DDC_AUX_SEL
96	TPM_PP	USB7_HOST_PRSNT
97	TYPE10#	SPI_CS#
98	SER0_TX	DD 0_CTRLCLK_AUX+
99	SER0_RX	DD 0_CTRLDATA_AUX-
100	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWMOUT
102	SER1_RX	FAN_TACHIN
103	LID#	SLEEP#
104	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)

4.6.2 Type 6

Modules implementing Pin-out Type 6 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.3 for the order in which interfaces ***shall*** be implemented.

Table 4.39: Pin List for Pin-Out Type 6

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GND	GND
3	GBE0_MDI3+	LPC_FRAME#/ESPI_CS0#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0/ESPI_IO_0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1/ESPI_IO_1	GND	GND
6	GBE0_MDI2-	LPC_AD2/ESPI_IO_2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3/ESPI_IO_3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	LPC_DRQ0#/ESPI_ALERT0#	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#/ESPI_ALERT1#	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK/ESPI_CK	USB_SSRX2+	USB_SSTX2+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	USB_SSRX3-	USB_SSTX3-
13	GBE0_MDI0+	SMB_CK	USB_SSRX3+	USB_SSTX3+
14	GBE0_CTREF	SMB_DAT	GND	GND
15	SUS_S3#	SMB_ALERT#	DDI1_PAIR6+	DDI1_CTRLCLK_AUX+
16	SATA0_TX+	SATA1_TX+	DDI1_PAIR6-	DDI1_CTRLDATA_AUX-
17	SATA0_TX-	SATA1_TX-	RSVD[10]	RSVD[10]
18	SUS_S4#	SUS_STAT#/ESPI_RESET#	RSVD[10]	RSVD[10]
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-	SATA3_TX-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	DDI1_HPD	RSVD[10]
25	SATA2_RX+	SATA3_RX+	DDI1_PAIR4 +	RSVD[10]
26	SATA2_RX-	SATA3_RX-	DDI1_PAIR4-	DDI1_PAIR0+
27	BATLOW#	WDT	RSVD[10]	DDI1_PAIR0-
28	(S)ATA_ACT#	HDA_SDIN2	RSVD[10]	RSVD[10]
29	HDA_SYNC	HDA_SDIN1	DDI1_PAIR5+	DDI1_PAIR1+
30	HDA_RST#	HDA_SDIN0	DDI1_PAIR5-	DDI1_PAIR1-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	HDA_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	BIOS_DIS0#/ESPI_SAFS	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
35	THRMTRIP#	THRM#	RSVD[10]	RSVD[10]
36	USB6-	USB7-	DDI3_CTRLCLK_AUX+	DDI1_PAIR3+
37	USB6+	USB7+	DDI3_CTRLDATA_AUX-	DDI1_PAIR3-
38	USB_6_7_OC#	USB_4_5_OC#	DDI3_DDC_AUX_SEL	RSVD[10]
39	USB4-	USB5-	DDI3_PAIR0+	DDI2_PAIR0+
40	USB4+	USB5+	DDI3_PAIR0-	DDI2_PAIR0-
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	DDI3_PAIR1+	DDI2_PAIR1+
43	USB2+	USB3+	DDI3_PAIR1-	DDI2_PAIR1-
44	USB_2_3_OC#	USB_0_1_OC#	DDI3_HPD	DDI2_HPD

10 *RSVD pins are reserved for future use and* ***should*** *be no connect. Do not tie the RSVD pins together.*

Pin	Row A	Row B	Row C	Row D
45	USB0-	USB1-	RSVD[10]	RSVD[10]
46	USB0+	USB1+	DDI3_PAIR2+	DDI2_PAIR2+
47	VCC_RTC	ESPI_EN#	DDI3_PAIR2-	DDI2_PAIR2-
48	RSVD[10]	USB0_HOST_PRSNT	RSVD[10]	RSVD[10]
49	GBE0_SDP	SYS_RESET#	DDI3_PAIR3+	DDI2_PAIR3+
50	LPC_SERIRQ/ESPI_CS1#	CB_RESET#	DDI3_PAIR3-	DDI2_PAIR3-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_RX1-	PEG_TX1-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_RX3-	PEG_TX3-
63	GPI1	GPO3	RSVD[10]	RSVD[10]
64	PCIE_TX1+	PCIE_RX1+	RSVD[10]	RSVD[10]
65	PCIE_TX1-	PCIE_RX1-	PEG_RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_RX4-	PEG_TX4-
67	GPI2	WAKE1#	RAPID_SHUTDOWN	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_RX5+	PEG_TX5+
69	PCIE_TX0-	PCIE_RX0-	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+	PEG_RX6+	PEG_TX6+
72	LVDS_A0-	LVDS_B0-	PEG_RX6-	PEG_TX6-
73	LVDS_A1+	LVDS_B1+	GND	GND
74	LVDS_A1-	LVDS_B1-	PEG_RX7+	PEG_TX7+
75	LVDS_A2+	LVDS_B2+	PEG_RX7-	PEG_TX7-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD[10]	RSVD[10]
78	LVDS_A3+	LVDS_B3-	PEG_RX8+	PEG_TX8+
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+	PEG_TX9+
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-	PEG_TX9-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD[10]	RSVD[10]
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	RSVD	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	eDP_HPD	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PEG_RX11+	PEG_TX11+
89	PCIE_CLK_REF-	VGA_RED	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-	PEG_TX13-
96	TPM_PP	VGA_I2C_DAT	GND	GND
97	TYPE10#	SPI_CS#	RSVD[10]	RSVD[10]
98	SER0_TX	RSVD[10]	PEG_RX14+	PEG_TX14+
99	SER0_RX	RSVD[10]	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

Pin	Row A	Row B	Row C	Row D
101	SER1_TX	FAN_PWMOUT	PEG_RX15+	PEG_TX15+
102	SER1_RX	FAN_TACHIN	PEG_RX15-	PEG_TX15-
103	LID#	SLEEP#	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

4.6.3 Type 7

Modules implementing Pin-out Type 7 ***shall*** use the pin-out shown in this table. Refer to Table 3.2 for minimum requirements and Table 3.3 for the order in which interfaces ***shall*** be implemented.

Table 4.40: Pin List for Pin-Out Type 7

Pin	Row A	Row B	Row C	Row D
1	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#	GND	GND
3	GBE0_MDI3+	LPC_FRAME#/ESPI_CS0#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0/ESPI_IO_0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1/ESPI_IO_1	GND	GND
6	GBE0_MDI2-	LPC_AD2/ESPI_IO_2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3/ESPI_IO_3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	LPC_DRQ0#/ESPI_ALERT0#	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#/ESPI_ALERT1#	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK/ESPI_CK	USB_SSRX2+	USB_SSTX2+
11	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#	USB_SSRX3-	USB_SSTX3-
13	GBE0_MDI0+	SMB_CK	USB_SSRX3+	USB_SSTX3+
14	GBE0_CTREF	SMB_DAT	GND	GND
15	SUS_S3#	SMB_ALERT#	10G_PHY_MDC_SCL3	10G_PHY_MDIO_SDA3
16	SATA0_TX+	SATA1_TX+	10G_PHY_MDC_SCL2	10G_PHY_MDIO_SDA2
17	SATA0_TX-	SATA1_TX-	10G_SDP2	10G_SDP3
18	SUS_S4#	SUS_STAT#/ESPI_RESET#	GND	GND
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
22	PCIE_TX15+	PCIE_RX15+	PCIE_RX7+	PCIE_TX7+
23	PCIE_TX15-	PCIE_RX15-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	10G_INT2	10G_INT3
25	PCIE_TX14+	PCIE_RX14+	GND	GND
26	PCIE_TX14-	PCIE_RX14-	10G_KR_RX3+	10G_KR_TX3+
27	BATLOW#	WDT	10G_KR_RX3-	10G_KR_TX3-
28	(S)ATA_ACT#	RSVD	GND	GND
29	RSVD	RSVD	10G_KR_RX2+	10G_KR_TX2+
30	RSVD	RSVD	10G_KR_RX2-	10G_KR_TX2-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	RSVD	SPKR	10G_SFP_SDA3	10G_SFP_SCL3
33	RSVD	I2C_CK	10G_SFP_SDA2	10G_SFP_SCL2
34	BIOS_DIS0#/ESPI_SAFS	I2C_DAT	10G_PHY_RST_23	10G_PHY_CAP_23
35	THRMTRIP#	THRM#	10G_PHY_RST_01	10G_PHY_CAP_01
36	PCIE_TX13+	PCIE_RX13+	10G_LED_SDA	RSVD
37	PCIE_TX13-	PCIE_RX13-	10G_LED_SCL	RSVD
38	GND	GND	10G_SFP_SDA1	10G_SFP_SCL1
39	PCIE_TX12+	PCIE_RX12+	10G_SFP_SDA0	10G_SFP_SCL0
40	PCIE_TX12-	PCIE_RX12-	10G_SDP0	10G_SDP1
41	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-	10G_KR_RX1+	10G_KR_TX1+
43	USB2+	USB3+	10G_KR_RX1-	10G_KR_TX1-
44	USB_2_3_OC#	USB_0_1_OC#	GND	GND
45	USB0-	USB1-	10G_PHY_MDC_SCL1	10G_PHY_MDIO_SDA1

Pin	Row A	Row B	Row C	Row D
46	USB0+	USB1+	10G_PHY_MDC_SCL0	10G_PHY_MDIO_SDA0
47	VCC_RTC	ESPI_EN#	10G_INT0	10G_INT1
48	RSVD	USB0_HOST_PRSNT	GND	GND
49	GBE0_SDP	SYS_RESET#	10G_KR_RX0+	10G_KR_TX0+
50	LPC_SERIRQ/ESPI_CS1#	CB_RESET#	10G_KR_RX0-	10G_KR_TX0-
51	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+	PCIE_RX16+	PCIE_TX16+
53	PCIE_TX5-	PCIE_RX5-	PCIE_RX16-	PCIE_TX16-
54	GPI0	GPO1	TYPE0#	RSVD
55	PCIE_TX4+	PCIE_RX4+	PCIE_RX17+	PCIE_TX17+
56	PCIE_TX4-	PCIE_RX4-	PCIE_RX17-	PCIE_TX17-
57	GND	GPO2	TYPE1#	TYPE2#
58	PCIE_TX3+	PCIE_RX3+	PCIE_RX18+	PCIE_TX18+
59	PCIE_TX3-	PCIE_RX3-	PCIE_RX18-	PCIE_TX18-
60	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+	PCIE_RX19+	PCIE_TX19+
62	PCIE_TX2-	PCIE_RX2-	PCIE_RX19-	PCIE_TX19-
63	GPI1	GPO3	RSVD	RSVD
64	PCIE_TX1+	PCIE_RX1+	RSVD	RSVD
65	PCIE_TX1-	PCIE_RX1-	PCIE_RX20+	PCIE_TX20+
66	GND	WAKE0#	PCIE_RX20-	PCIE_TX20-
67	GPI2	WAKE1#	RAPID_SHUTDOWN	GND
68	PCIE_TX0+	PCIE_RX0+	PCIE_RX21+	PCIE_TX21+
69	PCIE_TX0-	PCIE_RX0-	PCIE_RX21-	PCIE_TX21-
70	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
71	PCIE_TX8+	PCIE_RX8+	PCIE_RX22+	PCIE_TX22+
72	PCIE_TX8-	PCIE_RX8-	PCIE_RX22-	PCIE_TX22-
73	GND	GND	GND	GND
74	PCIE_TX9+	PCIE_RX9+	PCIE_RX23+	PCIE_TX23+
75	PCIE_TX9-	PCIE_RX9-	PCIE_RX23-	PCIE_TX23-
76	GND	GND	GND	GND
77	PCIE_TX10+	PCIE_RX10+	RSVD	RSVD
78	PCIE_TX10-	PCIE_RX10-	PCIE_RX24+	PCIE_TX24+
79	GND	GND	PCIE_RX24-	PCIE_TX24-
80	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
81	PCIE_TX11+	PCIE_RX11+	PCIE_RX25+	PCIE_TX25+
82	PCIE_TX11-	PCIE_RX11-	PCIE_RX25-	PCIE_TX25-
83	GND	GND	RSVD	RSVD
84	NCSI_TX_EN	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PCIE_RX26+	PCIE_TX26+
86	RSVD	VCC_5V_SBY	PCIE_RX26-	PCIE_TX26-
87	RSVD	VCC_5V_SBY	GND	GND
88	PCIE_CK_REF+	BIOS_DIS1#	PCIE_RX27+	PCIE_TX27+
89	PCIE_CK_REF-	NCSI_RX_ER	PCIE_RX27-	PCIE_TX27-
90	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
91	SPI_POWER	NCSI_CLK_IN	PCIE_RX28+	PCIE_TX28+
92	SPI_MISO	NCSI_RXD1	PCIE_RX28-	PCIE_TX28-
93	GPO0	NCSI_RXD0	GND	GND
94	SPI_CLK	NCSI_CRS_DV	PCIE_RX29+	PCIE_TX29+
95	SPI_MOSI	NCSI_TXD1	PCIE_RX29-	PCIE_TX29-
96	TPM_PP	NCSI_TXD0	GND	GND
97	TYPE10#	SPI_CS#	RSVD	RSVD
98	SER0_TX	NCSI_ARB_IN	PCIE_RX30+	PCIE_TX30+
99	SER0_RX	NCSI_ARB_OUT	PCIE_RX30-	PCIE_TX30-
100	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
101	SER1_TX	FAN_PWMOUT	PCIE_RX31+	PCIE_TX31+

Pin	Row A	Row B	Row C	Row D
102	SER1_RX	FAN_TACHIN	PCIE_RX31-	PCIE_TX31-
103	LID#	SLEEP#	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)

5 Module and Carrier Board Implementation Specifications

5.1 PCI Express Link Configuration Definitions

Lane:

A "lane" or "PCI Express lane" is a set of 4 pins on the COM Express connector that can be used for a single PCI Express transmit pair and a single receive pair. Clocking information is embedded into the data stream.

Link:

A "link" or "PCI Express link" is a group of PCI Express lanes between two PCI Express agents. Allowable link widths are x1, x2, x4, x8, x16 and x32. A x1 link utilizes 1 lane; a x2 link 2 lanes, etc. The link bandwidth scales up proportionally with the link width.

Link Configuration:

The COM Express connector allows up to 32 PCI Express lanes to be used. The count varies with the Module Pin-out Type. Chipsets used on COM Express Modules have a variety of PCI Express lane and link capabilities. On some chipsets, the PCI Express lanes can be grouped into various links under software control; on other chipsets, the PCI Express links are of a fixed width. The mapping of the chipset PCI Express lanes to the COM Express lanes and the grouping of the lanes into links is referred to as "link configuration."

Bucket:

A "bucket" is a group of 8 PCI Express lanes on the COM Express connector. The 32 PCI Express lanes on the COM Express connector are conceptually divided into 4 buckets to facilitate a description of how the available PCI Express lanes ***should*** be assigned to COM Express connector pins. The "bucket" terminology is only a vehicle to facilitate the description of an orderly mapping of chipset PCI Express lanes to COM Express connector PCI Express lanes. A bucket is not a link.

5.2 PCI Express Link Configuration Guidelines

The COM Express connector PCI Express lanes are conceptually divided into four "buckets," labeled B1, B2, B3, and B4. The buckets ***shall*** be filled according to the following rules. If a conflict in rules occurs, the lower number rule takes precedence.

1. The fill ***shall*** start from the lowest lane number in a bucket and proceeds upwards.
2. The largest links ***shall*** go into the lower lane numbers in a bucket.
3. Links that are 16 lanes wide ***shall*** span buckets B3 and B4 or buckets B1 and B2.
4. PCI Express Graphics (PEG) link(s) ***shall*** use B3 and B4 for the first link and ***shall*** use B1 and B2 for a 2nd link.
5. Links that span more than one bucket ***shall*** start in the bucket with the lowest lane number.
6. Bucket fill order ***shall*** be B1, B3, B4, then B2.
   (e.g. B1 filled, B2 empty, B3 filled, B4 empty)
7. Lower speed links (earlier generation) fill order ***shall*** be B1, B2, B3, then B4.
   (e.g. B1 gen2, B2 gen2, B3 gen3, B4 gen3)

Table 5.1: PCI Express Lane Numbers and Bucket Groupings

COM Express Pin Label	Lane Number	Availability By Module Pin-out Type	Bucket Reference
PEG15	PCIE31	Module Pin-out Types 6,7 (PCI Express Graphics)	Bucket B4
PEG14	PCIE30		
PEG13	PCIE29		
PEG12	PCIE28		
PEG11	PCIE27		
PEG10	PCIE26		
PEG9	PCIE25		
PEG8	PCIE24		
PEG7	PCIE23	Module Pin-out Types 6,7 (PCI Express, general I/O)	Bucket B3
PEG6	PCIE22		
PEG5	PCIE21		
PEG4	PCIE20		
PEG3	PCIE19		
PEG2	PCIE18		
PEG1	PCIE17		
PEG0	PCIE16		
PCIE15	PCIE15	Module Pin-out Type 7	Bucket B2
PCIE14	PCIE14		
PCIE13	PCIE13		
PCIE12	PCIE12		
PCIE11	PCIE11		
PCIE10	PCIE10		
PCIE9	PCIE9		
PCIE8	PCIE8		
PCIE7	PCIE7	Module Pin-out Types 6,7	Bucket B1
PCIE6	PCIE6		
PCIE5	PCIE5	Module Pin-out Types 6,7	
PCIE4	PCIE4		
PCIE3	PCIE3	Module Pin-out Types 6,7,10	
PCIE2	PCIE2		
PCIE1	PCIE1		
PCIE0	PCIE0		

Table 5.2: Module Pin-Out Type 6 - Preferred Lane Groupings: Bucket B1

<table>
<tr><th>COM Express Pin Label</th><th>Lane</th><th>Bucket Reference</th><th colspan="12">Preferred Link Configurations</th></tr>
<tr><td>PEG15</td><td>PCIE31</td><td rowspan="8">B4</td><td colspan="12" rowspan="16">X16
(PEG)</td></tr>
<tr><td>PEG14</td><td>PCIE30</td></tr>
<tr><td>PEG13</td><td>PCIE29</td></tr>
<tr><td>PEG12</td><td>PCIE28</td></tr>
<tr><td>PEG11</td><td>PCIE27</td></tr>
<tr><td>PEG10</td><td>PCIE26</td></tr>
<tr><td>PEG9</td><td>PCIE25</td></tr>
<tr><td>PEG8</td><td>PCIE24</td></tr>
<tr><td>PEG7</td><td>PCIE23</td><td rowspan="8">B3</td></tr>
<tr><td>PEG6</td><td>PCIE22</td></tr>
<tr><td>PEG5</td><td>PCIE21</td></tr>
<tr><td>PEG4</td><td>PCIE20</td></tr>
<tr><td>PEG3</td><td>PCIE19</td></tr>
<tr><td>PEG2</td><td>PCIE18</td></tr>
<tr><td>PEG1</td><td>PCIE17</td></tr>
<tr><td>PEG0</td><td>PCIE16</td></tr>
<tr><td>PCIE15</td><td>PCIE15</td><td rowspan="8">B2</td><td colspan="12" rowspan="8"></td></tr>
<tr><td>PCIE14</td><td>PCIE14</td></tr>
<tr><td>PCIE13</td><td>PCIE13</td></tr>
<tr><td>PCIE12</td><td>PCIE12</td></tr>
<tr><td>PCIE11</td><td>PCIE11</td></tr>
<tr><td>PCIE10</td><td>PCIE10</td></tr>
<tr><td>PCIE9</td><td>PCIE9</td></tr>
<tr><td>PCIE8</td><td>PCIE8</td></tr>
<tr><td>PCIE7</td><td>PCIE7</td><td rowspan="8">B1</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X1</td><td>X1</td><td rowspan="4">X4</td><td rowspan="8">X8</td></tr>
<tr><td>PCIE6</td><td>PCIE6</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X1</td><td>X1</td><td>X1</td></tr>
<tr><td>PCIE5</td><td>PCIE5</td><td></td><td></td><td></td><td></td><td></td><td></td><td>X1</td><td>X1</td><td>X1</td><td>X1</td></tr>
<tr><td>PCIE4</td><td>PCIE4</td><td></td><td></td><td></td><td></td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td></tr>
<tr><td>PCIE3</td><td>PCIE3</td><td></td><td></td><td>X1</td><td rowspan="3">X4</td><td>X1</td><td rowspan="3">X4</td><td>X1</td><td>X1</td><td>X1</td><td rowspan="3">X4</td><td rowspan="3">X4</td></tr>
<tr><td>PCIE2</td><td>PCIE2</td><td></td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td></tr>
<tr><td>PCIE1</td><td>PCIE1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td></tr>
<tr><td>PCIE0</td><td>PCIE0</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td><td>X1</td></tr>
</table>

Notes:

1. Lanes 6 and 7 are only available on Types 6 and 7.
2. If upper lanes (buckets B3 and B4) are not used for PCI Express Graphics (PEG), then lanes mapped into buckets B3 and B4 ***should*** be grouped per Table 5.3 'Module Pin-Out Type 6 - Preferred Lane Groupings: Buckets B3 and B4' on page 92.

Table 5.3: Module Pin-Out Type 6 - Preferred Lane Groupings: Buckets B3 and B4

<table>
<tr><th>COM Express Pin Label</th><th>PCI Express Lane</th><th>Bucket Reference</th><th colspan="4">Preferred Link Configurations</th></tr>
<tr><td>PEG15</td><td>PCIE31</td><td rowspan="8">B4</td><td rowspan="4">X4</td><td rowspan="4">X4</td><td rowspan="8">X8</td><td rowspan="16">X16
(PEG)</td></tr>
<tr><td>PEG14</td><td>PCIE30</td></tr>
<tr><td>PEG13</td><td>PCIE29</td></tr>
<tr><td>PEG12</td><td>PCIE28</td></tr>
<tr><td>PEG11</td><td>PCIE27</td><td rowspan="4">X4</td><td rowspan="4">X4</td></tr>
<tr><td>PEG10</td><td>PCIE26</td></tr>
<tr><td>PEG9</td><td>PCIE25</td></tr>
<tr><td>PEG8</td><td>PCIE24</td></tr>
<tr><td>PEG7</td><td>PCIE23</td><td rowspan="8">B3</td><td rowspan="4">X4</td><td rowspan="8">X8</td><td rowspan="8">X8</td></tr>
<tr><td>PEG6</td><td>PCIE22</td></tr>
<tr><td>PEG5</td><td>PCIE21</td></tr>
<tr><td>PEG4</td><td>PCIE20</td></tr>
<tr><td>PEG3</td><td>PCIE19</td><td rowspan="4">X4</td></tr>
<tr><td>PEG2</td><td>PCIE18</td></tr>
<tr><td>PEG1</td><td>PCIE17</td></tr>
<tr><td>PEG0</td><td>PCIE16</td></tr>
<tr><td>PCIE15</td><td>PCIE15</td><td rowspan="8">B2</td><td colspan="4" rowspan="8"></td></tr>
<tr><td>PCIE14</td><td>PCIE14</td></tr>
<tr><td>PCIE13</td><td>PCIE13</td></tr>
<tr><td>PCIE12</td><td>PCIE12</td></tr>
<tr><td>PCIE11</td><td>PCIE11</td></tr>
<tr><td>PCIE10</td><td>PCIE10</td></tr>
<tr><td>PCIE9</td><td>PCIE9</td></tr>
<tr><td>PCIE8</td><td>PCIE8</td></tr>
<tr><td>PCIE7</td><td>PCIE7</td><td rowspan="8">B1</td><td colspan="4" rowspan="8">Refer to bucket B1 in Table 5.2</td></tr>
<tr><td>PCIE6</td><td>PCIE6</td></tr>
<tr><td>PCIE5</td><td>PCIE5</td></tr>
<tr><td>PCIE4</td><td>PCIE4</td></tr>
<tr><td>PCIE3</td><td>PCIE3</td></tr>
<tr><td>PCIE2</td><td>PCIE2</td></tr>
<tr><td>PCIE1</td><td>PCIE1</td></tr>
<tr><td>PCIE0</td><td>PCIE0</td></tr>
</table>

Notes:

- X16 link ***may*** be used for PCI Express Graphics (PEG) or for general purpose I/O.

5.2.1 Type 7 Limitations

Type 7 Modules ***may*** support eight x1 root hubs in bucket one (B1). It is expected that future generation products may limit the number of available root hubs on first bucket (B1) to 2.

Table 5.4: Module Pin-Out Type 7 - Preferred Lane Groupings, X4 Root Hubs

<table>
<tr><th>COM Express Pin Label</th><th>PCI Express Lane</th><th>Bucket Reference</th><th colspan="5">Preferred Link Configurations</th></tr>
<tr><td>PEG15</td><td>PCIE31</td><td rowspan="8">B4</td><td rowspan="3"></td><td rowspan="2"></td><td rowspan="3">X4</td><td rowspan="8">X8</td><td rowspan="16">X16 (PEG)</td></tr>
<tr><td>PEG14</td><td>PCIE30</td></tr>
<tr><td>PEG13</td><td>PCIE29</td><td rowspan="2">X2</td></tr>
<tr><td>PEG12</td><td>PCIE28</td><td>X1</td></tr>
<tr><td>PEG11</td><td>PCIE27</td><td rowspan="3"></td><td></td><td rowspan="3">X4</td></tr>
<tr><td>PEG10</td><td>PCIE26</td></tr>
<tr><td>PEG9</td><td>PCIE25</td><td rowspan="2">X2</td></tr>
<tr><td>PEG8</td><td>PCIE24</td><td>X1</td></tr>
<tr><td>PEG7</td><td>PCIE23</td><td rowspan="8">B3</td><td rowspan="3"></td><td rowspan="2"></td><td rowspan="3">X4</td><td rowspan="8">X8</td></tr>
<tr><td>PEG6</td><td>PCIE22</td></tr>
<tr><td>PEG5</td><td>PCIE21</td><td rowspan="2">X2</td></tr>
<tr><td>PEG4</td><td>PCIE20</td><td>X1</td></tr>
<tr><td>PEG3</td><td>PCIE19</td><td rowspan="3"></td><td></td><td rowspan="3">X4</td></tr>
<tr><td>PEG2</td><td>PCIE18</td></tr>
<tr><td>PEG1</td><td>PCIE17</td><td rowspan="2">X2</td></tr>
<tr><td>PEG0</td><td>PCIE16</td><td>X1</td></tr>
<tr><td>PCIE15</td><td>PCIE15</td><td rowspan="8">B2</td><td rowspan="3"></td><td rowspan="2"></td><td rowspan="3">X4</td><td rowspan="8">X8</td><td rowspan="8"></td></tr>
<tr><td>PCIE14</td><td>PCIE14</td></tr>
<tr><td>PCIE13</td><td>PCIE13</td><td rowspan="2">X2</td></tr>
<tr><td>PCIE12</td><td>PCIE12</td><td>X1</td></tr>
<tr><td>PCIE11</td><td>PCIE11</td><td rowspan="3"></td><td></td><td rowspan="3">X4</td></tr>
<tr><td>PCIE10</td><td>PCIE10</td></tr>
<tr><td>PCIE9</td><td>PCIE9</td><td rowspan="2">X2</td></tr>
<tr><td>PCIE8</td><td>PCIE8</td><td>X1</td></tr>
<tr><td>PCIE7</td><td>PCIE7</td><td rowspan="8">B1</td><td>X1[11]</td><td></td><td rowspan="3">X4</td><td rowspan="8">X8</td><td rowspan="8"></td></tr>
<tr><td>PCIE6</td><td>PCIE6</td><td>X1[11]</td></tr>
<tr><td>PCIE5</td><td>PCIE5</td><td>X1[11]</td><td rowspan="2">X2</td></tr>
<tr><td>PCIE4</td><td>PCIE4</td><td>X1</td></tr>
<tr><td>PCIE3</td><td>PCIE3</td><td>X1[11]</td><td rowspan="3"></td><td rowspan="3">X4</td></tr>
<tr><td>PCIE2</td><td>PCIE2</td><td>X1[11]</td></tr>
<tr><td>PCIE1</td><td>PCIE1</td><td>X1[11]</td><td rowspan="2">X2</td></tr>
<tr><td>PCIE0</td><td>PCIE0</td><td>X1</td></tr>
</table>

11 The gray shaded X1 lanes may not be supported for future generation processors/chipsets.

Footnote: Type 7 Modules ***may*** support eight x1 root hubs in bucket one (B1). It is expected that future generation products may limit the number of available root hubs on bucket one to 2.

Caution: Type 7 does not support X1 root hubs. Therefore, there is a maximum of two X1 lanes per bucket and eight X1 lanes per system. This is to guarantee forward compatibility. Early implementation of type 7 hardware may provide additional X1 lanes, but forward compatibility is not guaranteed.

Type 7 Lane Reversal

Lane reversal is supported per root hub. Table Table 5.5 depicts a typical X4 root hub. The X2 is an aggregation of PCIe0 plus PCIe1 (PCIe2-3 are not available). The X1 is PCIe0 (PCIe1-3 are not available).

Table 5.5: Type 7 X4 Root Hub Without Lane Reversal

COM Express Pin Label	PCI Express Lane		Preferred Link Configuration		
PCIE3	PCIE3				X4
PCIE2	PCIE2				
PCIE1	PCIE1			X2	
PCIE0	PCIE0		X1		

Table Table 5.6 depicts a X4 root hub with lane reversal enabled. The X2 is an aggregation of PCIe2 plus PCIe3 (PCIE0-1 are not available). The X1 is PCIe3 (PCIE0-2 are not available).

Table 5.6: Type 7 X4 Root Hub With Lane Reversal

COM Express Pin Label	PCI Express Lane		Preferred Link Configuration		
PCIE3	PCIE3		X1	X2	X4
PCIE2	PCIE2				
PCIE1	PCIE1				
PCIE0	PCIE0				

Lane reversal is available on all root hubs.

5.3 COM Express EEPROMs

The COM Express EEPROM content is defined in the PICMG COM Express companion document EeeP(Embedded EEPROM) Specification. The COM Express R1.0 Carrier Board configuration EEPROM content and layout is superseded by the EeeP Specification. All new designs implementing either the Module or Carrier EEPROM ***shall*** exclusively use the new EeeP styled layout.

Note: As of the time of this writing, the EeeP specification does not contain Type 7 information. It will need to be updated at a later time.

5.3.1 EEPROM Device Information

If the Module and or Carrier EEPROMs are implemented, a two-wire serial interface device operating at a supply voltage of 3.3V ***shall*** be used. The two-wire interface ***shall*** be I2C compatible. The device ***shall*** have a capacity of at least 2 kbits, and ***shall*** have three address inputs. Suitable devices include the Atmel AT24C32C, the ST M24C32 and other compatible devices.

5.3.2 COM Express Module EEPROM

The Module Board ***should*** implement a serial EEPROM that Identifies the Module using the Unique Device Id.

The Module EEPROM allows the COM Express Carrier Board to set up any software configurable Carrier Board features in a way that is appropriate for the Module board. The Module EEPROM device, if implemented, ***shall*** interface to the Carrier Board over the general purpose I2C interface (COM Express pin names I2C_DAT and I2C_CK). The device address lines, A2, A1 and A0 ***shall*** be pulled to a logic low, placing the device at address 0x50(0xA0) (A6-A3 = 1010b for I2C EEPROM devices).

5.3.3 COM Express Carrier Board EEPROM

The Carrier Board ***should*** implement a serial EEPROM that identifies the Carrier using the Unique Device Id and describe the expected PCI Express link configuration. In addition this EEPROM ***may*** describe the expected link presence for SATA, USB, DDI, VGA, LAN, audio, and the expected presence of miscellaneous I/O signals.

The Carrier EEPROM allows the COM Express Module BIOS to set up any software configurable Module features in a way that is appropriate for the Carrier Board. If there is an incompatibility between the expected Carrier Board configuration and the Module capabilities, an error message ***may*** be generated. The error messaging is Module vendor specific and is not defined by this standard.

The Carrier EEPROM device, if implemented, ***shall*** interface to the Module over the general purpose I2C interface (COM Express pin names I2C_DAT and I2C_CK). The device address lines, A2, A1 and A0 ***shall*** be pulled to a logic high, placing the device at address 0x57(0xAE) (A6-A3 = 1010b for I2C EEPROM devices).

5.4 Loss Budgets for High Speed Differential Interfaces

COM Express Module and Carrier Board insertion loss budgets for the PCI Express, SATA, USB and GbE interfaces are presented in the following Sections.
The COM Express Module and Carrier Board insertion loss budgets were formulated to be compatible with the relevant source specifications. The source specifications vary in their treatment of insertion loss parameters. For example, the PCI Express Card Electromechanical Specification factors cross talk losses into the insertion loss budgets, but the SATA, USB and GbE source specifications do not.
For frequency dependent material losses, a rule-of-thumb insertion loss value of 0.28 dB per inch per GHz is used in all cases, representative of commonly used FR4 PCB laminates. This value is consistent with the PCI Express Card Electromechanical Specification usage (which calls out a 1.4 dB material loss for 4 inches of trace at 1.25 GHz). It is also consistent with other PICMG specifications that use values slightly above and below this value.
Module and Carrier Board vendors ***may*** elect to use PCB laminates with better characteristics than common FR4. If this is done, then the trace lengths referenced in the following Sections may be extended as long as the net insertion loss budgets are met.

There is no explicit COM Express jitter budget for the high speed differential interfaces. Designers are referred to the relevant source specifications (PCIE, SATA, USB and GbE) for system jitter budgets.

To develop guidelines for PCI Express Gen 2 (5 GT/s) operation, a series of simulations that modeled PCIe Gen2 operations in the COM Express environment was conducted per the recommendations given in the PCI-SIG PCI Express ® Base Specification, Rev 2.1, Section 4.3.6, “Channel Specifications”. The following two paragraphs excerpted from the PCI-SIG document, Section 4.3.6.2, “Channel Characteristics at 5.0 GT/s” may serve as an overview of the PCI-SIG recommendations:

> At 5.0 GT/s a more accurate method of comprehending the effects of channel loss is required in order to avoid excessive guardbanding. The method described here imports the channel’s s-parameters into a simulation environment that includes worst case models for transmitters and data patterns. The resulting time domain simulation yields eye diagrams from which voltage and timing margins may be obtained and compared against those defined for the receiver.
> Note: The methodology described in Sections 4.3.6.2 through 4.3.6.2.7 must be applied to 5.0 GT/s designs, and may be applied to 2.5 GT/s designs.
> A channel's characteristics are completely defined by its s-parameters, in particular: insertion loss, return loss, and aggressor-victim coupling. It can been demonstrated that these parameters are sufficient to completely quantize all channel-induced phenomena affecting eye margins including I/O-channel impedance mismatch, insertion loss, jitter amplification, impedance discontinuities, and crosstalk. Long channels tend to be dominated by insertion loss and crosstalk, while short channels tend to dominated by impedance discontinuities. Since both types of channels are possible in PCI Express implementations, it is necessary provide a means of

characterizing the channel that comprehends all possible channel characteristics.

All relevant elements of the COM Express environment were included in the simulations: a PCIe Gen 2 source, package breakout, coupling capacitors, Module trace, COM Express connector, Carrier Board trace, and Carrier Board target device, for the "Device Down" case. The "Device Up" case was also simulated, adding in the effects of a Slot Card connector and trace. Cross-talk, jitter and inter-symbol interference effects were included in the simulations, and both the common clocked and data clocked PCIe operations were considered. The simulations were carried out assuming that the Module, Carrier, and Slot PCBs care constructed with standard FR4 dielectrics. Full details of these simulations may be found in the document titled '***PCIe Gen2 COM Express® Hardware Simulation Report***', available from the PICMG.

The conclusions drawn from the simulations are that the eye margins are dominated by the trace length in the various sections and the jitter components, and that connector losses and crosstalk play minor roles. For Gen 2 operation, the maximum allowed PCIe trace lengths need to be shorter than those that were allowed for Gen 1 operation.

Note: Revision 3 of this document includes PCI Express Gen 3 routing guidelines that were pulled from the COM Express Carrier Design Guide.

5.4.1 PCI Express Insertion Loss Budget with Slot Card

Figure 5-1: PCI Express Insertion Loss Budget with Slot Card

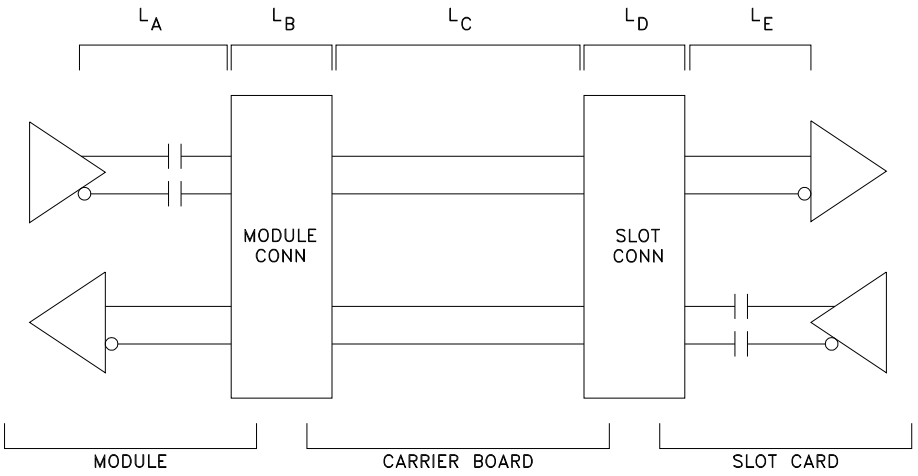


Table 5.7: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board Slot Card

Segment	max. Length [mm/inches]	Notes
L_A	130/5.15	Allowance for 3.45 dB loss @ 0 28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps		1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B		COM Express connector at 1.25 GHz measured value: 0.25 dB loss.
L_C	228/9.0	Allowance for 4.40 db loss @ 0.28 dB / GHz / inch and a 1.25 dB crosstalk allowance.
L_D		1.25 dB loss. PCI Express Card Electromechanical Spec Rev 1.1 “guard band” allowance for slot connector – includes 1.0 dB connector loss.
L_E		2.65 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1 (without coupling caps; L_{AR}). Implied crosstalk allowance is 1.25 dB.
Total		13.20 dB loss.

The Module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Module transmit path. The Module transmit path insertion loss budget ***shall*** be 4.65 dB (3.46 dB + 1.19 dB). The Module receive path insertion loss budget ***shall*** be 3.46 dB. COM Express connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are the same in this case. The Carrier Board insertion loss budget ***shall*** be 4.40 dB. COM Express connector and slot card connector losses are accounted for separately.

The slot card transmit and receive insertion loss budgets are different due to the

presence of the coupling caps in the slot card's transmit path. The slot card's transmit path insertion loss budget is 3.84 dB (2.65 dB + 1.19 dB) per the PCI Express Card Electromechanical Specification Revision 1.1. The slot card's receive path insertion loss budget is 2.65 dB per the same specification. Slot card connector loss is accounted for separately.

Table 5.8: PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board Slot Card

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for Module trace. Coupling cap effects included within simulation.
L_B		COM Express connector simulated at 2.5 GHz.
L_C	113/4.45	Allowance for Carrier Board.
L_D		PCI Express Card slot connector simulated at 2.5 GHz.
L_E	80/3.15	Slot Card trace length from PCI Express Card Electromagnetical Spec., Rev. 1.1
Total	320/12.6	PCIe GEN2 Data clocked architecture

For "device up" PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 4.45 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics. Other dielectrics with lower losses could be considered, but were not simulated.

It can be noted that a use case exists that might result in reduced PCI Express bandwidth. This use case is tied to Carrier boards with a PCI Express slot (device up). PCI Express Gen 1 and Gen 2 signaling rates use the same PCI Express connector – there is no mechanical keying mechanism to identify the capabilities of the PCI Express slot or the PCI Express board plugged into the slot. This can lead to the situation where the Module and PCI Express board attempt a PCI Express Gen2 signaling rate connection over a Carrier that does not meet the routing guidelines for Gen 2 signaling rates. In a worst case scenario the devices might connect at Gen2 signaling rate with a high number of errors impacting the actual data throughput. It should be noted that there is a Carrier EEPROM which would allow the Module to determine the Carrier Board capabilities but this is not a requirement in COM.0.

5.4.2 PCI Express Insertion Loss Budget with Carrier Board PCIe Device

The insertion losses previously allowed for the slot card and slot card connector are re-allocated for use on the Carrier Board, allowing longer Carrier Board trace lengths and more Carrier Board design flexibility. The Module and COM Express connector loss budgets remain the same.

Figure 5-2: PCI Express Insertion Loss Budget with Carrier Board PCIe Device

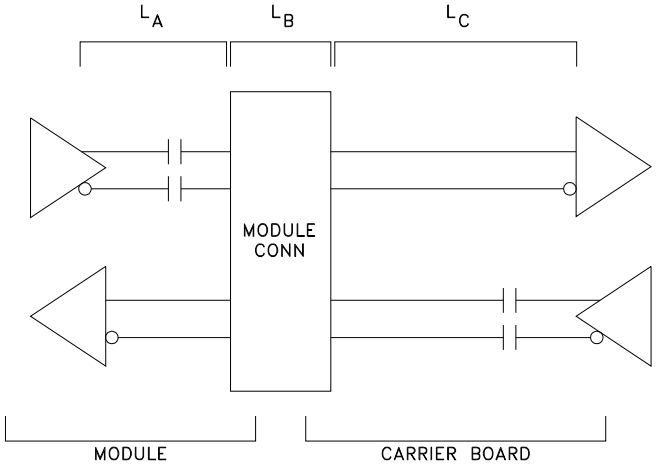


Table 5.9: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board PCIe Device

Segment	max. Length [mm/inches]	Notes
L_A	131/5.15	Allowance for 3.46 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps		1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B		COM Express connector at 1.25 GHz measured value: 0 25 dB loss
L_C	402/15.85	Allowance for 8.30 dB loss @ 0.28 dB / GHz / inch and a 2.75 dB crosstalk allowance.
Total		13.20 dB loss

The Module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Module transmit path. The Module transmit path insertion loss budget ***shall*** be 4.65 dB (3.46 dB + 1.19 dB). The Module receive path insertion loss budget ***shall*** be 3.46 dB. COM Express connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Carrier Board transmit path. The Carrier Board transmit path insertion loss budget ***shall*** be 9.49 dB (8.30 dB + 1.19 dB). The Carrier Board receive path insertion loss ***shall*** be 8.30 dB. COM Express connector loss is accounted for separately.

Table 5.10: PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board PCIe Device

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for Module trace. Coupling cap effects included within simulation.
L_B		COM Express connector simulated at 2.5 GHz.
L_C	203/8.0	Allowance for Carrier Board trace.
Total	330/13 0	PCIe GEN2 Data clocked architecture

For “device down” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 8.0 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics. Other dielectrics with lower losses could be considered, but were not simulated.

Table 5.11: PCI Express Trace Routing Guidelines

Parameter	PCIe Gen2	PCIe Gen3
Symbol Rate / PCIe Lane	5.0 G Symbols/s	8.0 G Symbols/s
Maximum signal line length (coupled traces) TX and RX	21.0 inches	14.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe device	15.85 inches	10.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe slot	9.00 inches	4.0 inches
PCI-SIG: Differential impedance recommendation	85 Ω +/-15%	85 Ω +/-15%
COMCDG Rev. 2.0: Differential impedance recommendation for new Carrier designs	85 Ω +/-15%	
Single-ended Impedance	50 Ω +/-15%	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.	No strict electrical requirements. Keep difference within a 3 0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.	No electrical requirements.
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 40mils	Min. 40mils
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace	Max. 2 vias / TX Max. 4 vias / RX (to device) Max. 2 vias / RX (to slot)
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 200nF +/-10%, 16V, shape 0402.

5.4.3 SATA Insertion Loss Budget

The Serial ATA source specification provides insertion loss figures only for the SATA cable. There are several cable types defined with insertion losses ranging from 6 dB up to 16 dB. Cross talk losses are separate from material losses in the SATA specification. The COM Express SATA Insertion loss budgets presented below represent the material losses and do not include cross talk losses. The COM Express SATA Insertion loss budgets are a guideline: Module and Carrier Board vendors ***should not*** exceed the values shown in the tables below.

Figure 5-3: SATA Insertion Loss Budget

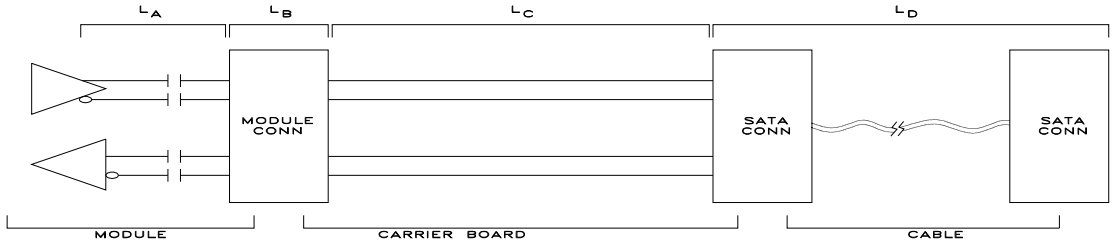


Table 5.12: SATA Gen 1 Insertion Loss Budget, 1.5 GHz

Segment	Loss (dB)	Notes
L_A	1.26	Up to 3.0 inches of Module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.25	COM Express connector at 1.5 GHz measured value
L_C	3.07	Up to 7.2 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

Table 5.13: SATA Gen 2 Insertion Loss Budget, 3.0 GHz

Segment	Loss (dB)	Notes
L_A	1.68	Up to 2.0 inches of Module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.38	COM Express connector at 3.0 GHz measured value
L_C	2.52	Up to 3.0 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

Table 5.14: Serial ATA Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	Up to 6 0 GBit/s
Maximum signal line length (coupled traces)	5.0 inches on PCB (COM Express Module and Carrier Board. The length of the SATA cable is specified between 0 and 40 inches)
Signal length used on COM Express Module (including the COM Express Carrier Board connector)	2 inches
Signal length available for the COM Express Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates
Differential Impedance	85 Ω +/-20%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict length-matching requirements. Route the signals as directly as possible.
Spacing from edge of plane	Min. 40mils
Via Usage	A maximum of 2 vias is recommended.
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the COM Express Module.

5.4.4 USB 2.0 Insertion Loss Budget

Figure 5-4: USB 2.0 Insertion Loss Budget

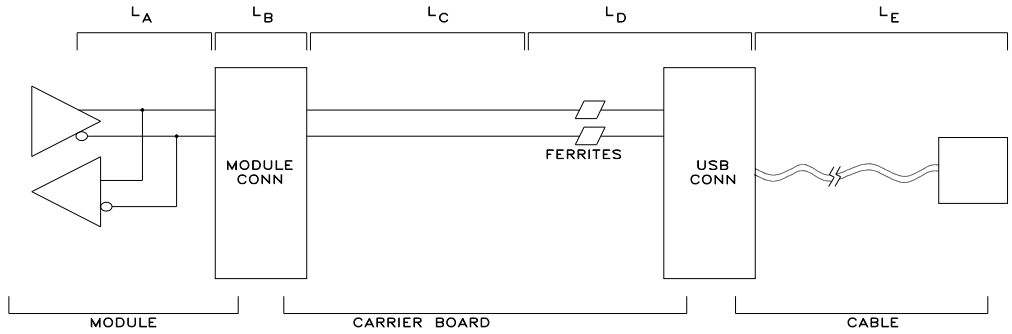


Table 5.15: USB Insertion Loss Budget, 400 MHz

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of Module trace @ 0.28 dB / GHz / inch
L_B	0.05	COM Express connector at 400 MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

COM Express USB implementations ***should*** conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the Carrier Board, ***may*** add the ferrite and USB connector insertion loss values to the Carrier Board budget. The Carrier Board insertion loss budget then becomes $L_C + L_D$, or 2.68 dB.

5.4.5 SuperSpeed USB Insertion Loss Budget

Figure 5-5: SuperSpeed USB Insertion Loss Budget

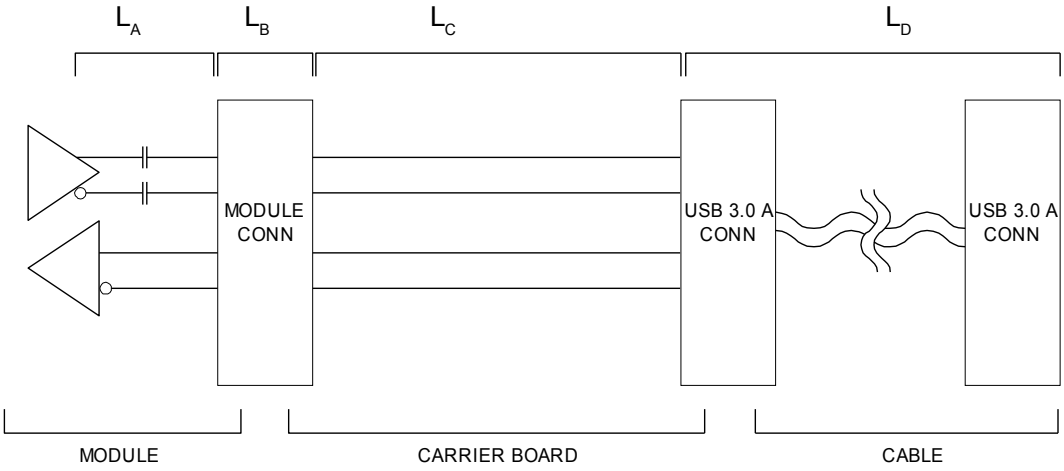


Table 5.16: SuperSpeed USB Insertion Loss Budget

Segment	Loss (dB)	Notes
L_A	1.94	Up to 3 inches of Module trace @ 2.5 GHz
L_B	1.20	COM Express connector at 2.5 GHz
L_C	3.64	Up to 5 inches of Carrier Board trace @ 2 5 GHz with Common-Mode Component
Total	6.78	

5.4.6 10/100/1000 Ethernet Insertion Loss Budget

Figure 5-6: 10/100/1000 Ethernet Insertion Loss Budget

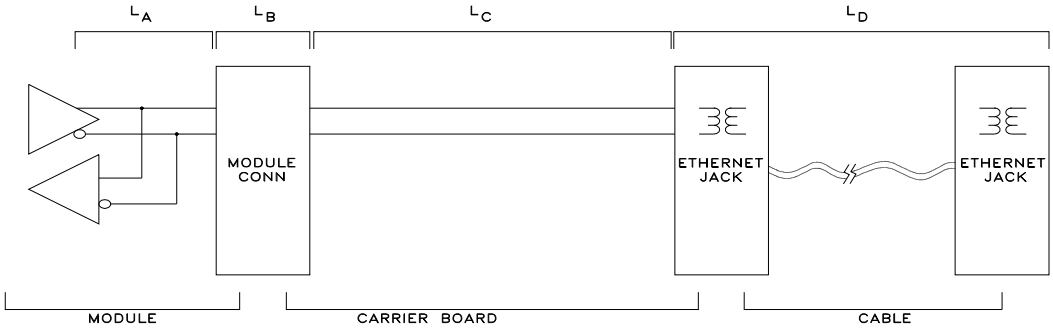


Table 5.17: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Loss (dB)	Notes
L_A	0.08	Up to 3 inches of Module trace @ 0.28 dB / GHz / inch
L_B	0.02	COM Express connector at 100 MHz measured value
L_C	0.15	Up to 5 inches of Carrier Board trace @ 0 28 dB / GHz / inch
L_D	24.00	Cable and cable connectors, integrated magnetics, per source spec.
Total	24.25	

COM Express Ethernet implementations ***should*** conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gb Ethernet specification.

"Device Down" implementations, in which the Ethernet target device is implemented on the Carrier Board (for instance, an Ethernet switch), ***may*** add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the Carrier Board budget. This insertion loss value is typically 1 dB. The Carrier Board insertion loss budget then becomes L_C + 1 dB, or 1.15 dB.

5.4.7 10Gb Ethernet Insertion Loss Performance

The 10Gb Ethernet interface to the COM Express connector is the KR interface as specified in the IEEE 802.3-KR Clause 72 and Annex 69B specification. This is the MAC to PHY interface as opposed to the PHY to connector (magnetic) interface of the 1Gb Ethernet connections.

Typically, the MAC KR interface is connected directly to the PHY. In the case of COM Express, the KR interface is connected through the COM Express connector to the PHY. The insertion loss performance must be maintained within the normative channel specification as stated in IEEE 802.3 Annex 69B.

Simulations have shown that the trace length allocations in Table 5.18 meet the required channel specifications. Proper high speed design techniques must be used. Consult the silicon design guide for trace clearance and other design rules. High speed guidance for the routing of 10GHz differential pairs is outside the scope of this document.

All differential pairs are routed at 100 Ohms +/-10% differential impedance

Match signals within a pair +/- 5 mils

Figure 5-7: 10GBASE-KR Trace Length Budget

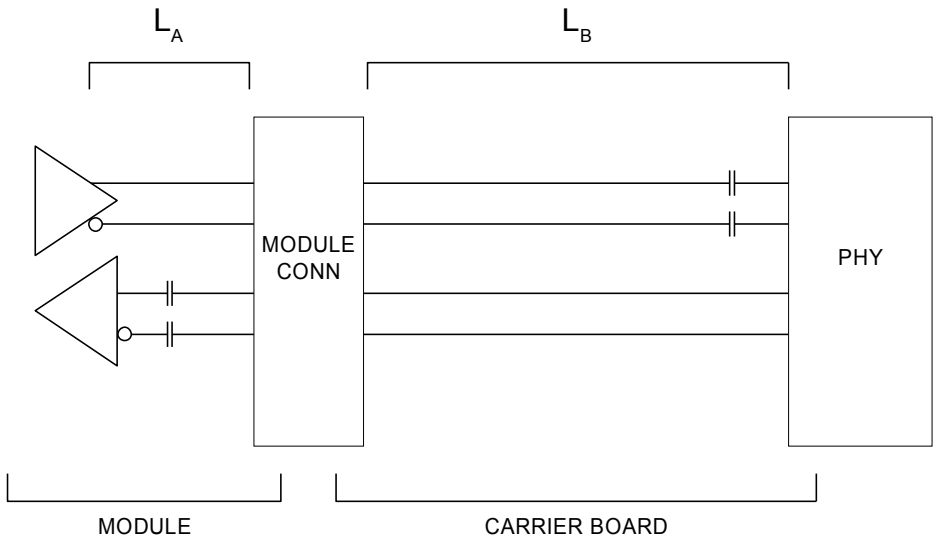


Table 5.18: 10GBASE-KR Trace Length Budget

Segment	Length (Mils)	Notes
L_A	2500	Up to 2.5 inches of Module trace (within Normal FR4)
L_C	5000	Up to 5 inches of Carrier Board trace (within Normal FR4)
Total	7500	

5.4.8 DDI Trace Length Recommendation

The DDI signals can be used to support a variety of video interfaces. The circuits required to realize the different video interfaces can be found at the PICMG Carrier Design Guide. Trace length recommendations for the DDI signals are specified below.

Figure 5-8: DDI Trace Length

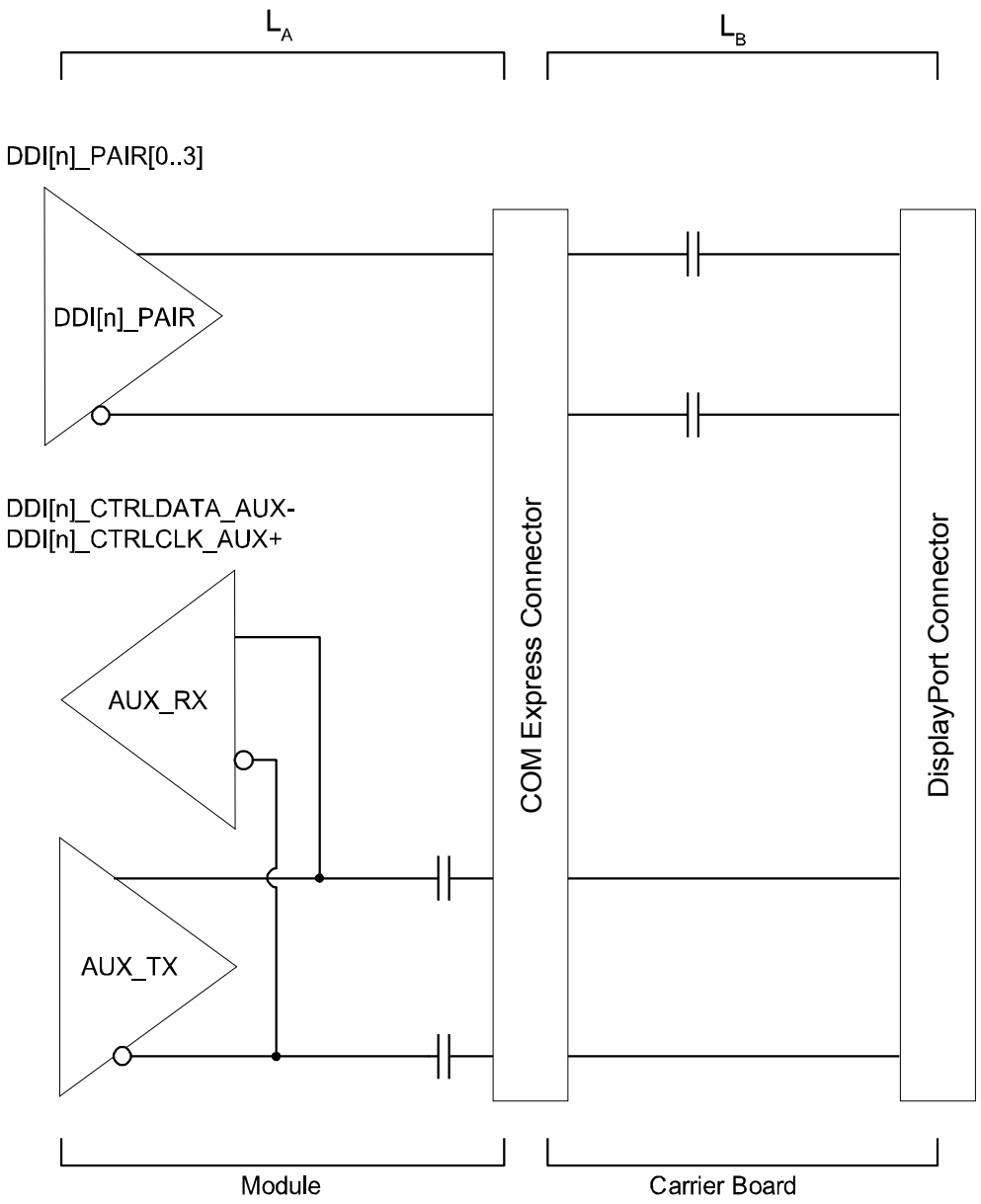


Figure 5-8 above shows a DisplayPort implementation. The DDI can also support TMDS. Depending on the type of video interface desired, there ***may*** be level shifters on the Carrier.

Requirements:

- DDI[n]_PAIR[0..3] L_A ***should*** be less than 4.0". L_A is defined as the total Module trace length from the silicon to the COM Express connector including any blocking capacitors that might be required.
- DDI[n]_PAIR[0..3] L_B ***should*** be less than 5.0". L_B is defined as the total trace length on the Carrier from the COM Express connector to the display connector or level shifter including any blocking capacitors that might be required.
- DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+ L_A ***should*** be less than 7.0".
  L_A is defined as the total Module trace length from the silicon to the COM Express connector including any blocking capacitors that might be required.
- DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+ L_B ***should*** be less than 5.0".
  L_B is defined as the total trace length on the Carrier from the COM Express connector to the display connector or level shifter including any blocking capacitors that might be required.

Table 5.19: DDI Trace Length

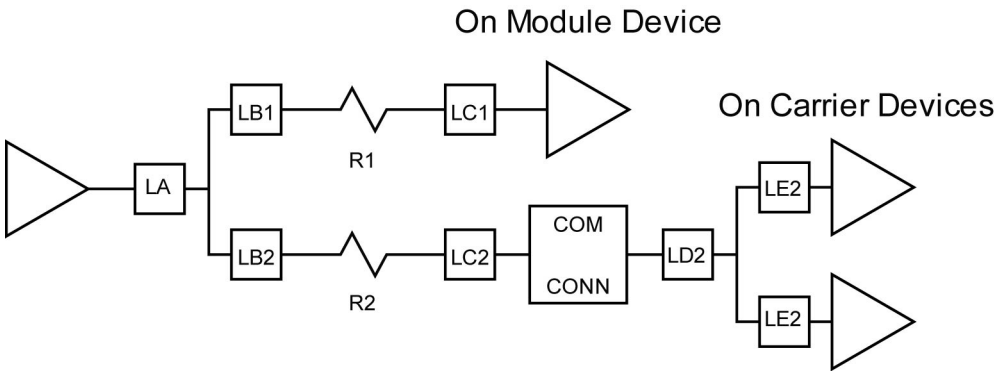
Segment	Trace Length (inch)	Notes
L_A	< 4.0	DDI[n]_PAIR[0..3]
L_B	< 5.0	DDI[n]_PAIR[0..3]
L_A	< 7.0	DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+
L_B	< 5.0	DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+
Total	< 9.0	DDI[n]_PAIR[0..3]
Total	< 12.0	DDI[n]_CTRLDATA_AUX- / DDI[n]_CTRLCLK_AUX+

5.4.9 Carrier Board LPC Devices

Carrier Board LPC devices ***should*** be clocked with the LPC clock provided by the Module interface. If the Carrier Board has two loads on the LPC clock these loads ***should*** be connected to the common clock without a buffer. The Carrier Board ***should*** not have more than two loads on the LPC clock.
Carrier Board LPC devices ***should*** be reset with signal CB_RESET#.

A typical routing topology for a Module LPC device and two Carrier Board LPC devices clock is shown below. This topology is used by Modules that start and stop the LPC clock on the fly. In this case, a buffer cannot be used and all LPC devices must share a common clock.

Figure 5-9: Typical Routing Topology for a Module LPC Device

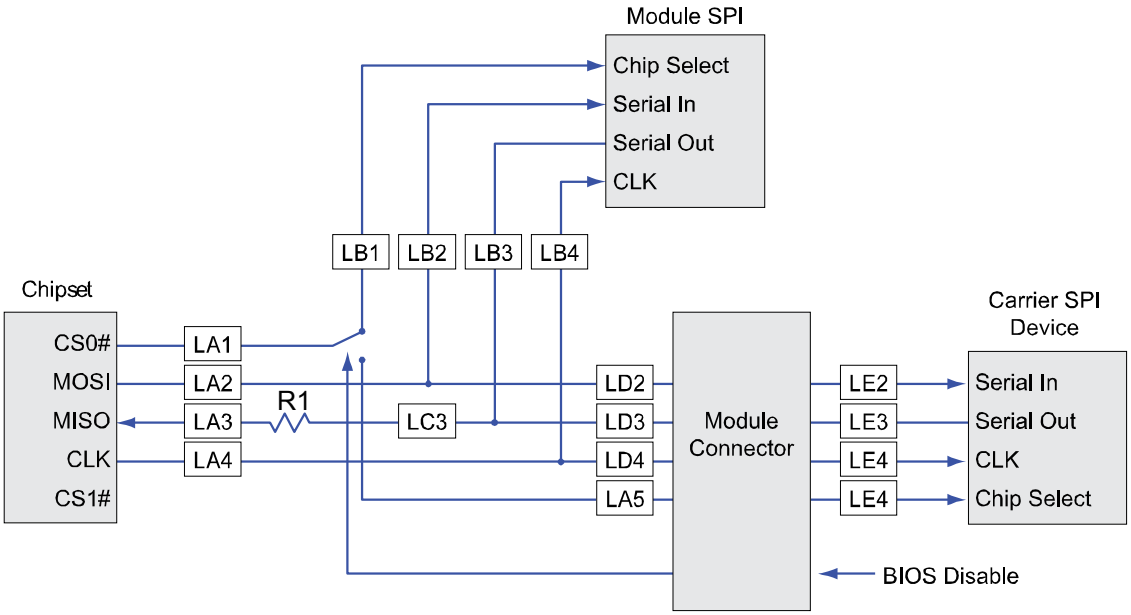


LA 500 mils max
LB1 = LB2 = 150 mils max
LC1 = 8.88”+LC2
LC2 = .25” max
LE2 = 1” max
LD2 + LE2 (note 2 instances of LE2) = 8.88”
R1 = R2 = 22Ω

5.5 SPI Devices

All Module types ***may*** implement a SPI bus. The SPI bus is replacing the LPC bus for BIOS EEPROM devices. If a Module supports an external BIOS it ***shall*** support an external SPI BIOS and ***may*** support an external LPC BIOS. The diagram below depicts a typical SPI topology. Note that other SPI configurations are possible including Module or Carrier based CS1# SPI device. Refer to Section 4.3.12 'SPI Interface' for other implementation options.

Figure 5-10: Typical SPI topology



(LA1 + LB1), (LA2 + LB2), (LA3 + LC3 + LB3), (LA4 + LB4) max length 2” match all within .1”
LD2, LD3, LD4, LD5 max length .25” (maximum stub length to COM.0 connector)
LE2, LE3, LE4, LE5 max length 4.5” match within .1”
(LA4 + LB4), (LA2 + LB2) match within .5” (match CLK & MOSI within .5” Module)
(LA4 + LD4), (LA2 + LD2) match within .4” (match CLK & MOSI within .5” Carrier Board)
(LA4 + LB4), (LA1 + LB1) match within .5” (match CLK & CS within .5” Module)
(LA4 + LD4), (LA1 + LA5) match within .4” (match CLK & CS within .5” Carrier Board)
R1 = 33Ω

5.6 eSPI Devices

At the time of this writing, the use case and design rules for eSPI are still being developed. Designers of Modules and Carriers are provided with the following guidance:

The maximum trace length for Carrier routed eSPI traces ***shall not*** exceed 4.5”.
Carrier routed ESPI traces ***shall*** be routed at 50 Ohms.
Carrier routed SPI traces ***shall*** have 5 mil via to via clearance, 4 mil trace to via clearance, and 10 mil clearance to any other traces.
The Carrier ***shall*** have a 33 Ohm series termination between 0.5” and 1” of the target device on the ESPI_CK signal.
The Carrier ***shall*** have a 33 Ohm series termination between 0.5” and 1” of the target device on the ESPI_IO_[0..3] signals.
The Carrier ***shall*** length match ESPI_CK and ESPI_IO_[0..3] within 250mils.
The Carrier ***shall*** length match eSPI_CK and ESPI_CS within 100mils.

5.7 Watchdog Timer

COM Express Modules ***may*** implement a watchdog timer output to the Carrier Board.

5.7.1 Output Modes and Characteristics

The support of a watch dog timer on the Module is optional. If a Module supports a watchdog timer it ***shall*** minimally support output mode 1 and ***may*** also support output modes 2 or 3 as defined below. The selection of the output modes ***may*** be realized by software configurable hardware or by Module build options.

Table 5.20: Watchdog Timer Output Modes

Output Mode	Description
1	The Module generates an internal reset. Module pins PCI_RST# and CB_RESET# that are supported are pulsed low. WDT pin is driven high until the unit resets.
2	The Module only drives WDT pin high until cleared by Module software.
3	The Module generates an NMI. WDT pin is driven high until cleared by Module software.

The watchdog output ***shall*** come up as a logic low and ***shall*** be disabled upon power-on-reset (VCC_12V power cycle) or external system reset (when SYS_RST# pin is toggled low by external hardware). The watchdog ***may*** be enabled by BIOS or system software.

5.7.2 Watchdog Enable and Strobe

Typically, the watchdog parameters (output options, enabling, enable delay, timeout delay) are managed by the Module BIOS, often via a BIOS setup screen. The regular watchdog strobes to prevent a watchdog timeout are typically handled by the Module's application software. There ***may*** be BIOS abstractions to isolate the application software from the watchdog hardware.

The software programmable Watchdog Enable Delay is the time between when the watchdog is enabled by firmware and when the first watchdog strobe is needed to prevent a watchdog time out. The enable delay allows time for the operating system to boot and the application to load and initialize.

After the initial Enable Delay, the enabled watchdog must be periodically strobed by software to prevent a watchdog timeout. The Strobe Interval ***shall*** be software programmable.

Recommended ranges in enable delay and max strobe periods are given in the following table.

Table 5.21: Watchdog Enable and Strobe Parameter Range

	Min Value	Max Value
Enable Delay	1 second	10 minutes
Strobe Interval	0.1 second	10 minutes

5.8 Protecting COM.0 Pins Reclaimed from the VCC_12V Pool

The COM.0 Rev. 2 Type 6 and Type 10 pin-out types introduce eight signals that are mapped to pins that are re-claimed from pins that are VCC_12V supply pins on Type 1,2,3,4 and 5 Modules. These signals include

- SER0_TX, SER1_TX — TTL level outputs from the Module
- SER0_RX, SER1_RX — TTL level inputs to the Module
- LID#, SLEEP# — 3.3V logic level inputs to the Module, in the suspend domain
- FAN_TACHIN — 3.3V logic level input to the Module
- FAN_PWMOUT — 3.3V logic level output from the Module

A new type strap pin is also introduced in COM.0 Rev 2, for all Module Types. It also falls on a pin that was used exclusively for VCC_12V in COM.0 Rev. 1:

- TYPE10# — VCC_12V on COM.0 Rev. 1 Module Types 1,2,3,4,5
  No connect on COM.0 Rev. 2 Module Types 1,2,3,4,5,6
  47K Module pull-down to GND on Module Type 10

All nine of the signals referenced above on COM.0 Rev. 2 compliant Module and Carrier designs ***shall*** be able to withstand continuous direct connections to low impedance 12V sources (i.e. a short to a 12V power supply).

One line of defense against such unintended connections is for Carrier designs to decode the Module TYPE pins (3 pins on the C-D connector, and the new TYPE10# pin on the A-B connector) and to not power the system up if an improper Module Type is detected. Examples of this may be found in the PICMG Carrier Design Guide. However, there are some situations in which this can not be relied upon. One such situation is if a user plugs a Type 10 Module into a Rev. 1 Type 1 Carrier. Since the TYPE10# strap was not anticipated in the Rev. 1 Carrier, the Carrier will apply power to the Type 10 Module. Thus it is very important that Type 10 and 6 Modules be able to withstand 12V exposure to the pins reclaimed from the VCC_12V pool.

5.8.1 Logic Level Signals on Pins Reclaimed from VCC_12V

Module logic level inputs and outputs that are implemented on pins reclaimed from the VCC_12V pool ***should*** implement the series Schottky diode protection shown in the right side of the Figure 5-11 or FET based protection as shown Figure 5-12.
Diode Based Method: The Schottky diode ***should*** be a BAT54 device. For inputs in this group, a 47K pull-up to the local 3.3V S0 or S5 rail (as appropriate) ***shall*** be used.
Carrier board logic level inputs and outputs that are implemented on pins reclaimed from the VCC_12V pool ***shall*** be protected against protracted accidental exposure to 12V. The protection scheme shown in the left side of the Figure 5-11 below ***may*** be used. Any scheme that is used ***shall*** be able to pull the reclaimed Module input low enough such that Module CMOS input logic sees a maximum voltage of 0.5V for a logic low, as indicated in the figure.

Figure 5-11: Protecting Logic Level Signals on Pins Reclaimed from VCC_12V, Diode Based Method

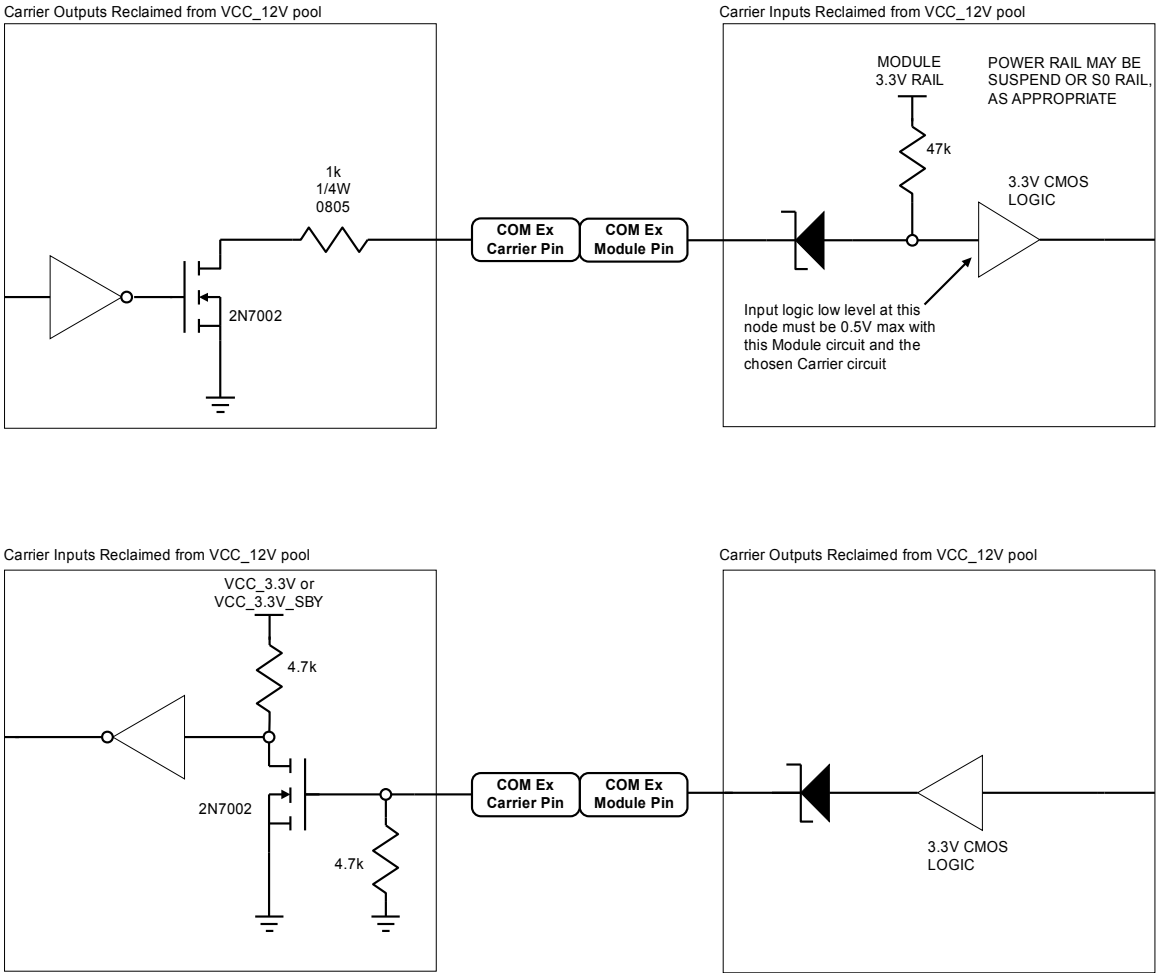
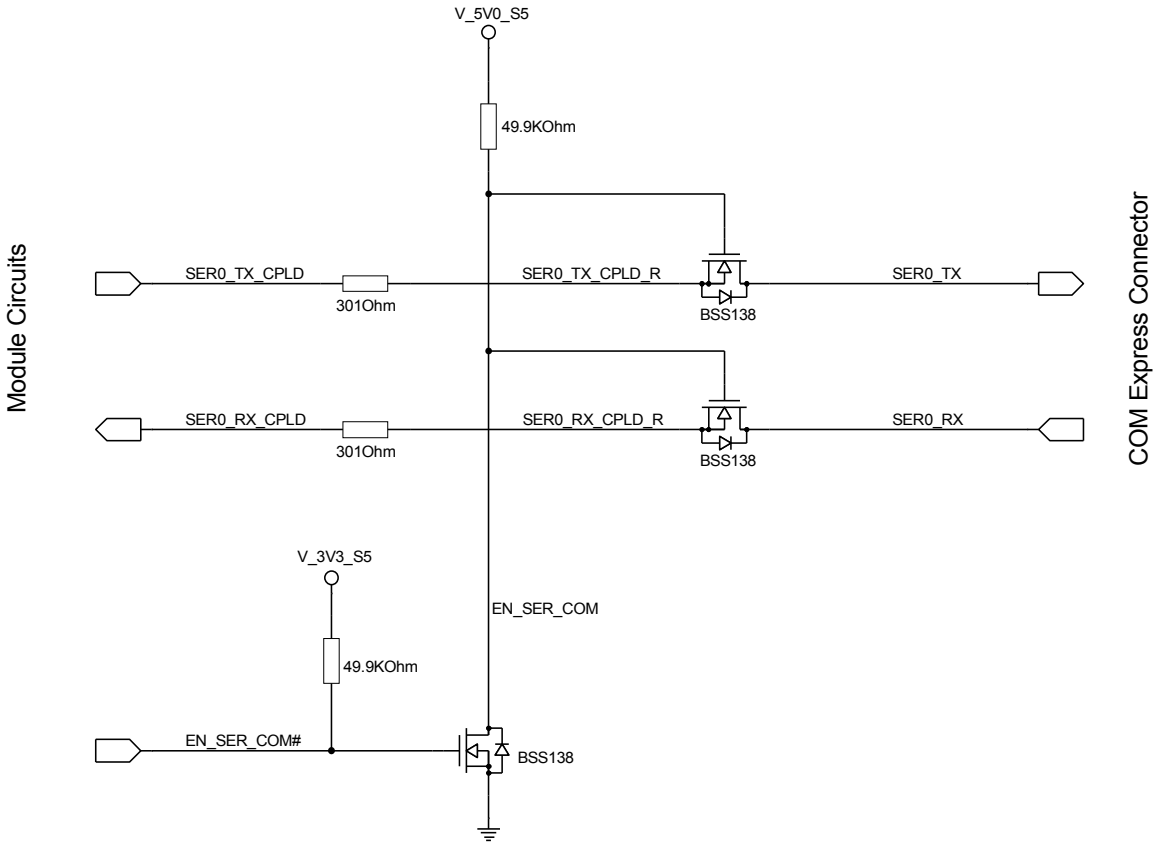


Figure 5-12: Protecting Logic Level Signals on Pins Reclaimed from VCC_12V, FET Based Method



Note: SER_RX_UART must have pull-up if operational compatibility with carrier boards with output circuit described in Figure 5-11, above, is required.

FET Based Method: The gate of the FET is connected to 5V. When the voltage on the drain goes above 5V the voltage on the source will be limited to 5V (the voltage on the gate) minus the turn-on threshold of the FET (around a volt for a BSS138). This requires that the serial port I/O (coming from a CPLD in this example) need to be 5V tolerant, as the voltage will rise above 3.3V but remain a Vth below the gate voltage. The series resistor is to limit the current into the serial port I/O when the FET source voltage is above the serial port's clamping voltage (this would be device dependent). If the serial port is not 5V tolerant then a clamping diode would be required to limit the voltage on the I/O.

Assuming a totem-pole driver on the device driving the drain of the FET on a receive port, the signal will drive the input hard up to 5V minus the Vth. This will allow a 3.3V signal to be driven hard, both high and low, providing much faster slew rates than using the diode and resistive pull-up that the COM Express currently recommends. If an open-drain driver is used on the receive lines, pull-up resistors will be required at the receiver.

Note that open-drain driver will not support higher slew rates.

The transmitter lines operate in the same manner, in as much as they will drive hard until the source of the FET reaches 5V minus Vth.

This circuit could also work with 3.3V connected to the FET gate. In this case the TX ports would drive hard high until 3.3V minus Vth and then would continue to drive high through the FET body diode. The RX ports would be driven hard high until 3.3V minus Vth and then be pulled the rest of the way to 3.3V by the pull-up resistor. This would not be a significant issue if the receiver inputs had high logic level maximums of around 2V. TTL logic levels would probably be ok.

The enable circuit, on the bottom of the sheet, is there to allow the FETs to be held off during power up so that no voltage can be fed through from the connected device, driving port I/O before its supply is up.

5.8.2 TYPE10# Strap - Reclaimed from VCC_12V

No additional protection is needed for the TYPE10# strap on the Module side:

- On Type 10 Modules, this pin is tied through a 47K resistor to GND. Exposure of this Module pin to 12V is harmless.
- On Rev. 1 Type 1,2,3,4,5 Modules, this pin is tied to VCC_12V already.
- On Rev. 2 Type 1,2,3,4,5 Modules, this pin is a no connect.
- On Type 6 Modules, this pin is a no connect.

On the Carrier side, protection against accidental 12V exposure is required. Carrier Board designs ***shall*** be tolerant of protracted VCC_12V exposure on the TYPE10# pin. A Rev. 1 Type 1 Module, for example, would expose the TYPE10# pin on a Rev. 2 Type 1,2,3,4,5 Carrier to 12V (unless the Carrier design does not allow the system to power up for an incorrect Module type).

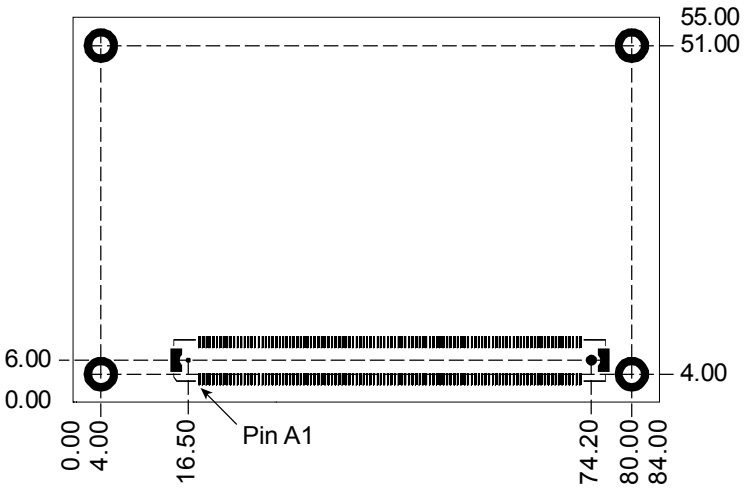
The TYPE10# Module pin is, in effect, a tri-level pin: it is tied, depending on Module Type and COM.0 Revision level, to either VCC_12V, to nothing, or to GND through 47K. Carrier Board circuits can be created that distinguish between the 3 levels. If implemented, this would allow the Carrier Board to determine whether a Type 1,2,3,4,5 Module is a built to COM.0 Rev. 1 or Rev. 2. This may be illustrated in a future edition of the PCIMG Carrier Design Guide.

6 Mechanical Specifications

6.1 Module Size – Mini Module

The PCB size for the Mini Module ***shall*** be 84mm x 55mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader (refer to Section 6.10 "Heat-Spreader").
The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***may***be used to attach the heat-spreader to the Module.

Figure 6-1: Mini Module Form Factor

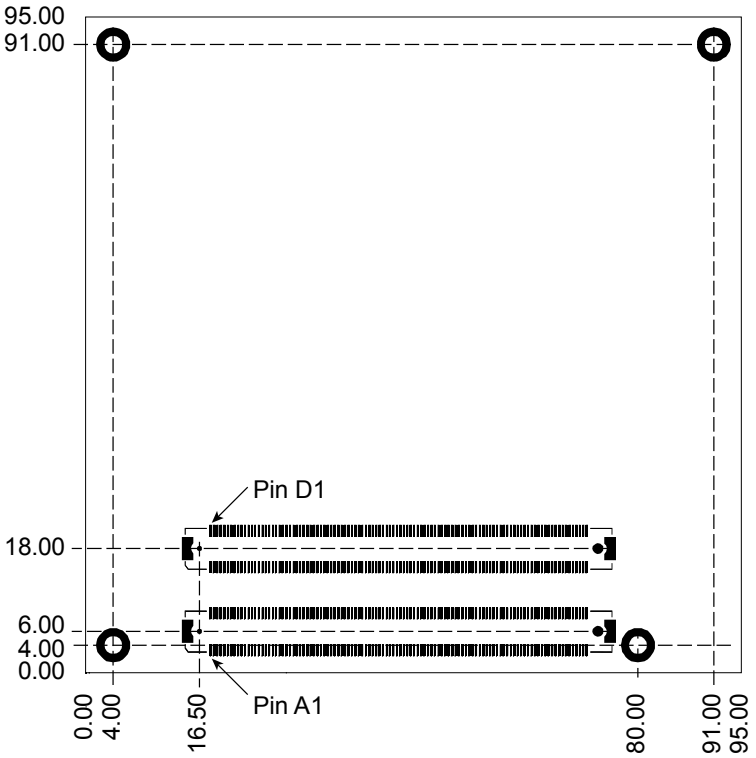


All dimensions are shown in millimeters.
Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.
The 220-pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.
The four mounting holes shown ***shall*** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads ***shall*** be tied to the PCB ground plane.
Modules ***shall*** include the 4 mounting holes as shown in Figure 6-1 above. These holes are primarily used to attach the Module to the Carrier.

6.2 Module Size - Compact Module

The PCB size for the Compact Module ***shall*** be 95mm x 95mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader (refer to Section 6.10 "Heat-Spreader").
The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-2: Compact Module Form Factor



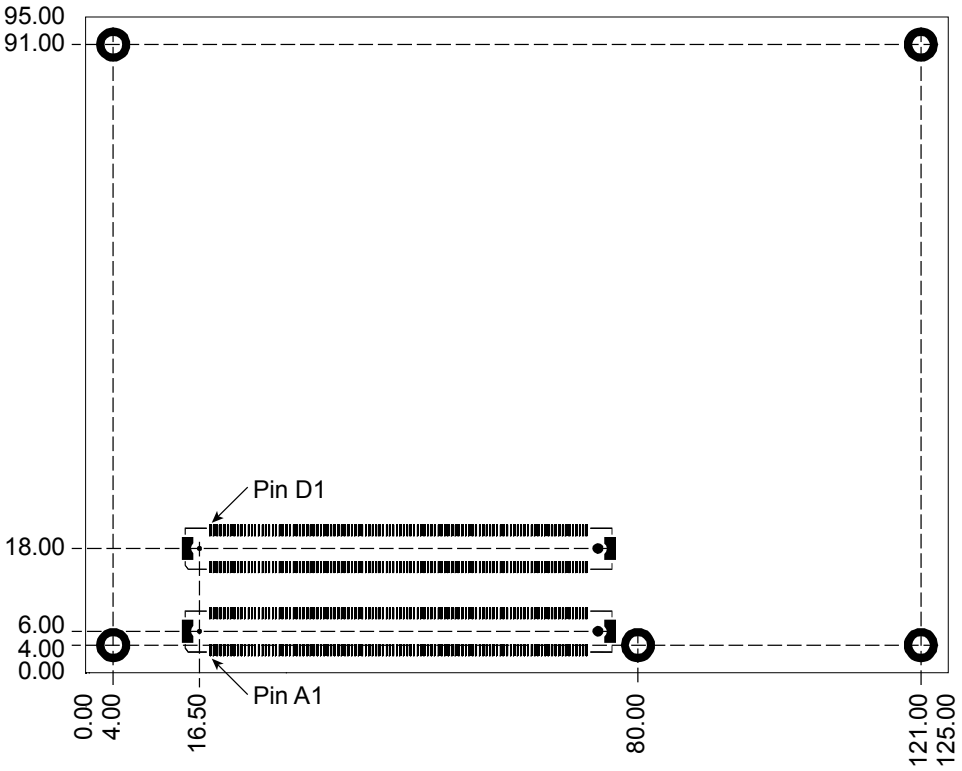
All dimensions are shown in millimeters.
Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.
The 440 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.
The four mounting holes shown ***shall*** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads ***shall*** be tied to the PCB ground plane.
Modules ***shall*** include the 4 mounting holes as shown in Figure 6-2 above. These holes are primarily used to attach the Module to the Carrier.

6.3 Module Size - Basic Module

The PCB size for the Basic Module ***shall*** be 125mm x 95mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader. (refer to Section 6.10 "Heat-Spreader").

The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-3: Basic Module Form Factor



All dimensions are shown in millimeters.

Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.

The 440 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.

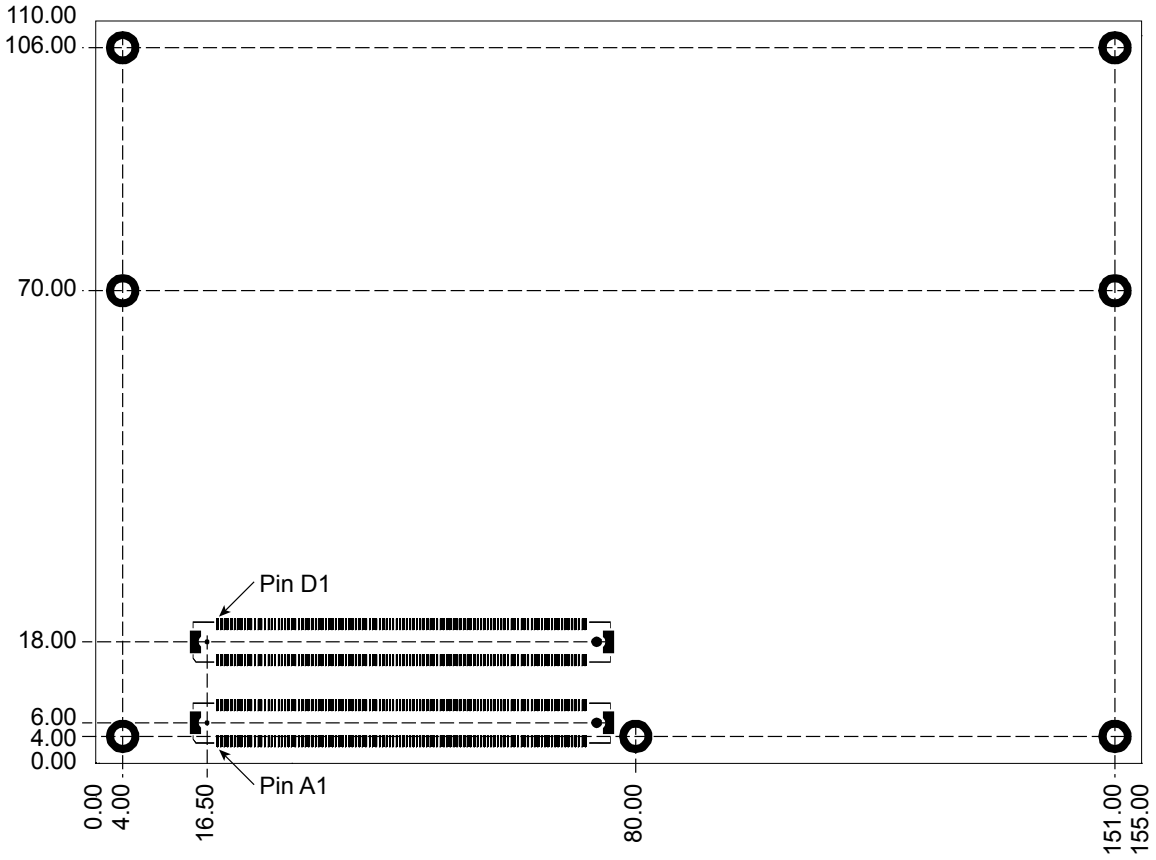
The five mounting holes shown ***shall*** use 6mm diameter pads and ***shall*** have 2.7mm plated holes, for use with 2.5mm hardware. The pads ***shall*** be tied to the PCB ground plane.

Modules ***shall*** include the 5 mounting holes as shown in Figure 6-3 above. These holes are primarily used to attach the Module to the Carrier.

6.4 Module Size - Extended Module

The PCB size for the Extended Module ***shall*** be 155mm x 110mm. The PCB thickness ***should*** be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader. (refer to Section 6.10 "Heat-Spreader").
The holes shown in this drawing are intended for mounting the Module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers ***shall*** be used to attach the heat-spreader to the Module.

Figure 6-4: Extended Module Form Factor



All dimensions are shown in millimeters.
Tolerances ***shall*** be ± 0.25mm [±0.010"], unless noted otherwise.
The 440 pin connector pair ***shall*** be mounted on the backside of the PCB and is seen "through" the board in this view.
The seven mounting holes shown ***shall*** use 6 mm diameter pads and have 2.7 mm plated holes, for use with 2.5 mm hardware. The pads ***shall*** be tied to the PCB ground plane.
Modules ***shall*** include the 7 mounting holes as shown in Figure 6-4 above. These holes are primarily used to attach the Module to the Carrier.

6.5 Module Connector

The Module connector for Pin-out Types 6 and 7 ***shall*** be a 440-pin receptacle that is composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle. The pair of connectors ***may*** be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Module Pin-out Type 10 ***shall*** use a single 220-pin, 0.5 mm pitch receptacle. The connectors ***shall*** be qualified for LVDS operation up to 6.25GHz and support for PCI Express Generation 3 signaling speeds.

Sources for the individual 220-pin receptacle are

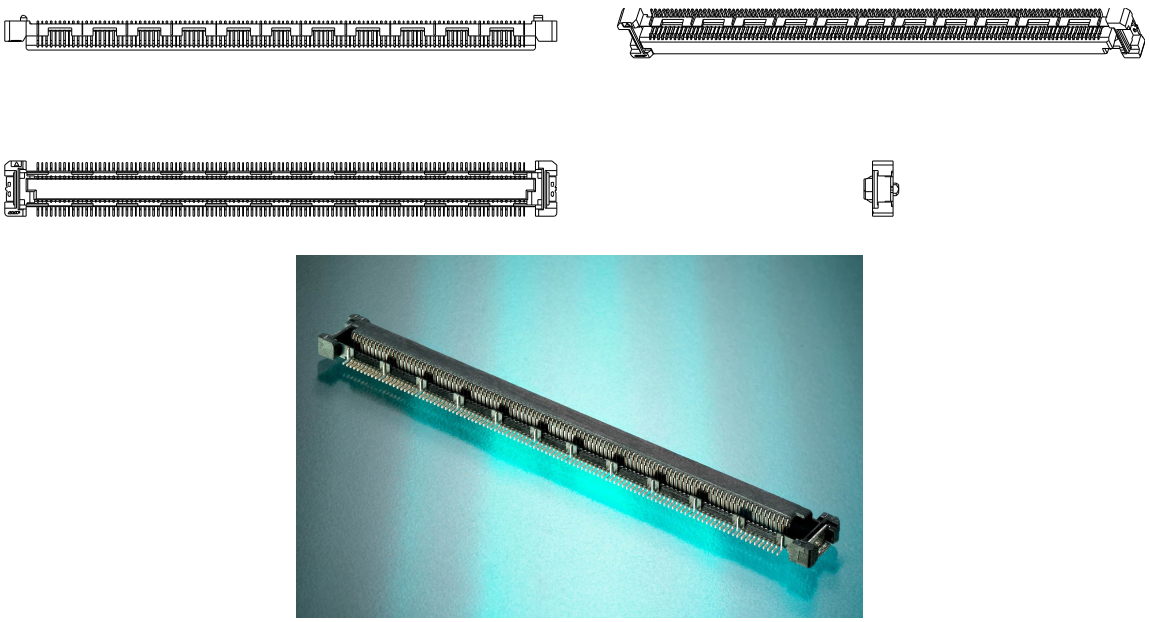
Tyco Electronics	3-6318490-6
Foxconn	QT012206-1031-2H
ept	402-51101-51
or equivalent	0.5 mm pitch Free Height 220-pin 4H Receptacle

Sources for the combined 440-pin receptacle (composed of 2 pieces of the 220-pin receptacle held by a carrier) are:

Tyco Electronics	3-1827231-6
Foxconn	QT012206-1041-3H
ept	402-51501-51
or equivalent	0.5mm pitch Free Height 440 pin 4H Receptacle

The Module connector is a receptacle by virtue of the vendor's technical definition of a receptacle, and to some users it looks like a plug.

Figure 6-5: Module Receptacle



6.6 Carrier Board Connector

The Carrier Board connector for Module Pin-out Types 6 and 7 ***shall*** be a 440-pin plug that is composed of 2 pieces of a 220-pin, 0.5 mm pitch plug. The pair of connectors ***may*** be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Carrier Boards intended only for use with Pin-out Type 10 Modules ***may*** use a single 220-pin, 0.5 mm pitch plug. The connectors ***shall*** be qualified for LVDS operation up to 6.25GHz and support for PCI Express Generation 3 signaling speeds. The Carrier Board plugs are available in a variety of heights. The Carrier Board ***shall*** use either the 5mm or 8mm heights.

Sources for the individual 5 mm stack height 220-pin plug are:

Tyco Electronics	3-1827253-6
Foxconn	QT002206-2131-3H
ept	401-51101-51
or equivalent	0.5 mm pitch Free Height 220-pin 5H Plug

Sources for the combined 5mm stack height 440-pin plug (composed of 2 pieces of the 220-pin plug held by a carrier) are:

Tyco Electronics	3-1827233-6
Foxconn	QT002206-2141-3H
ept	401-51501-51
or equivalent	0.5 mm pitch Free Height 440 pin 5H Plug

Sources for the individual 8 mm stack height 220-pin plug are:

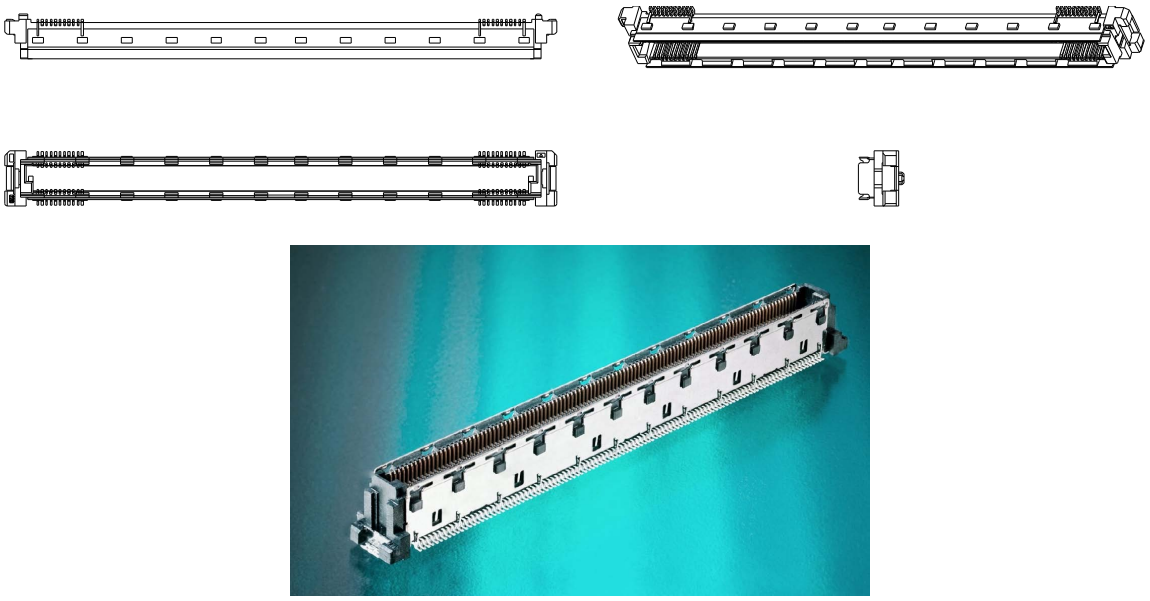
Tyco Electronics	3-6318491-6
Foxconn	QT002206-4131-3H
ept	401-55101-51
or equivalent	0.5 mm pitch Free Height 220-pin 8H Plug

Sources for the combined 8 mm stack height 440 pin plug (composed of 2 pieces of the 220-pin plug held by a carrier) are:

Tyco Electronics	3-5353652-6
Foxconn	QT002206-4141-3H
ept	401-55501-51
or equivalent	0.5 mm Free Height 440 pin 8H Plug or equivalent.

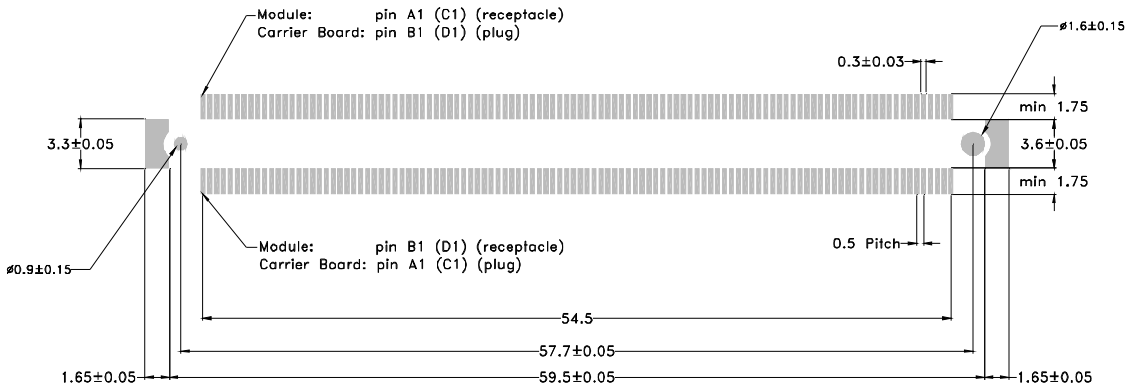
The Carrier Board connector is a plug by virtue of the vendor's technical definition of a plug, and to some users it looks like a receptacle.

Figure 6-6: Carrier Board Plug



6.7 Connector PCB Pattern

Figure 6-7: Connector PCB Pattern

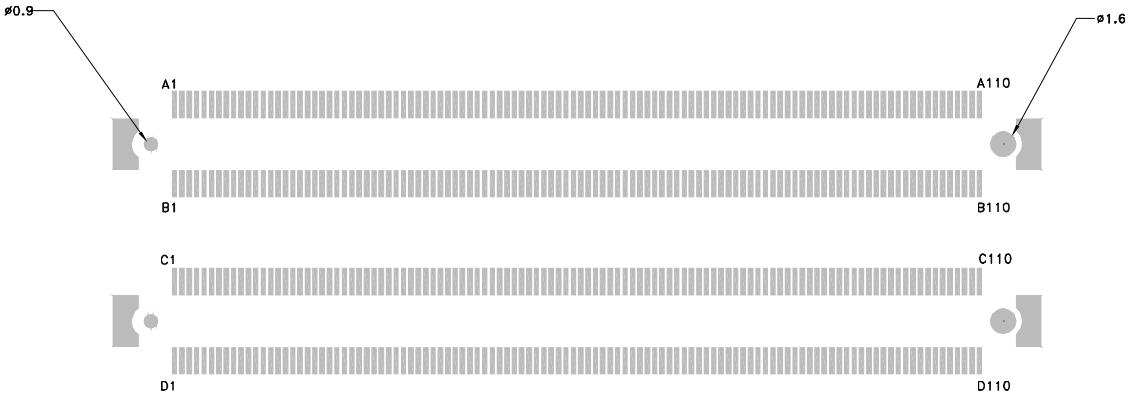


All dimensions in mm.

6.8 Module Connector Pin Numbering

Pin numbering for 440-pin Module receptacle. This is a top view of the receptacle, looking into the receptacle, as mounted on the backside of the Module.

Figure 6-8: Module Connector Pin Numbering

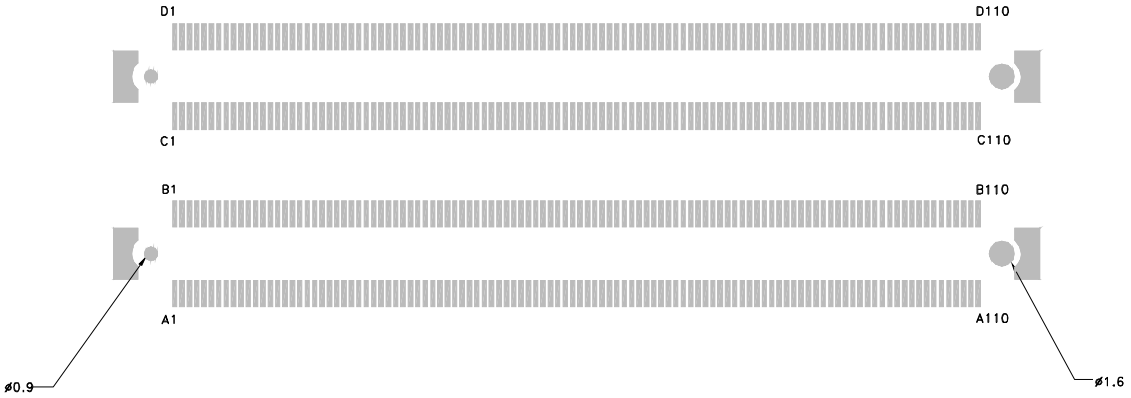


All dimensions in mm.

6.9 Carrier Board Connector Pin Numbering

Pin numbering for 440-pin Carrier Board plug. This is a top view, looking into the plug as mounted on the Carrier Board.

Figure 6-9: Carrier Board Connector Pin Numbering

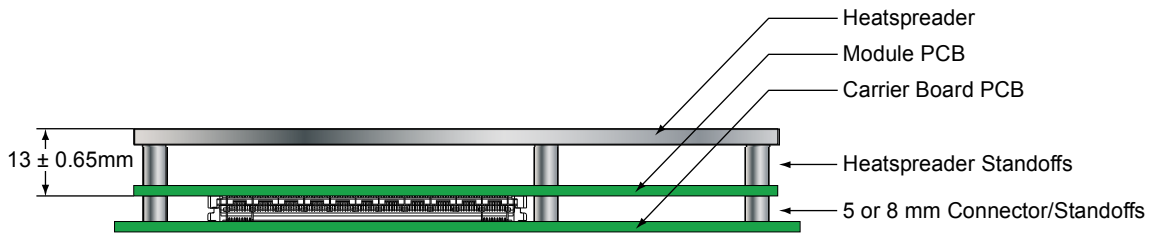


All dimensions in mm.

6.10 Heat-Spreader

Modules ***should*** be equipped with a heat-spreader. This heat-spreader by it self does not constitute the complete thermal solution for a Module but provides a common interface between Modules and implementation-specific thermal solutions.
If implemented, a heat-spreader for the Compact, Basic and Extended form factor ***shall*** use and the Mini form factor ***may*** use an implementation specific set of holes and spacers to attach the heat-spreader to the Module. These implementation specific holes are in addition to the Module mounting holes specified in Sections 6.2, 6.3 or 6.4.
For the Compact, Basic and Extended form factor a heat-spreader ***should not*** use the Module mounting holes as the only attachment points to a Module. The intent is to be able to provide a Module and heat-spreader as an assembly that can then be mounted to a Carrier without having to break the thermal interface between the Module components and the heat-spreader.
The standoffs shown in Figure 6-10 ***should*** be mounted on the Carrier Board. The height of the standoff is dependent on the stack height of the Carrier Board connector (5 mm or 8 mm).
The overall Module height from the bottom surface of the Module board to the heat-spreader top surface ***shall*** be 13 mm for the Mini, the Compact, the Basic and the Extended Modules. The Module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2 mm PCB with a 3 mm heat-spreader ***may*** be used which allows use of readily available standoffs.

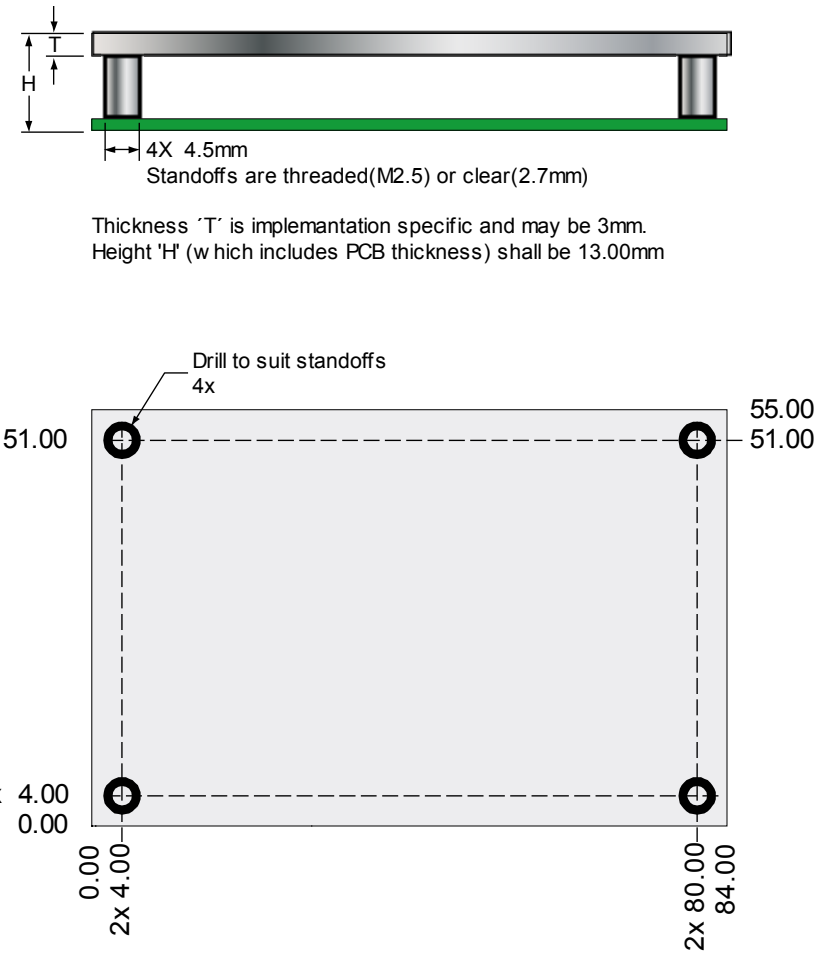
Figure 6-10: Overall Height for Heat-Spreader in Mini, Compact, Basic and Extended Modules



All dimensions in mm.

Tolerances (unless otherwise specified):
Z (height) dimensions ***should*** be ± 0.8mm [±0.031”] from top of Carrier Board to top of heat- spreader.
Heat-spreader surface ***should*** be flat within 0.2mm [.008"] after assembly.
Interface surface finish ***should*** have a maximum roughness average (R_a) of 1.6µm [63µin].
The critical dimension in Figure 6-10 is the Module PCB bottom side to heat-spreader top side. This dimension ***shall*** be 13.00mm ± 0.65mm [±0.026”].
Figure 6-10 shows a cross section of a Module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.

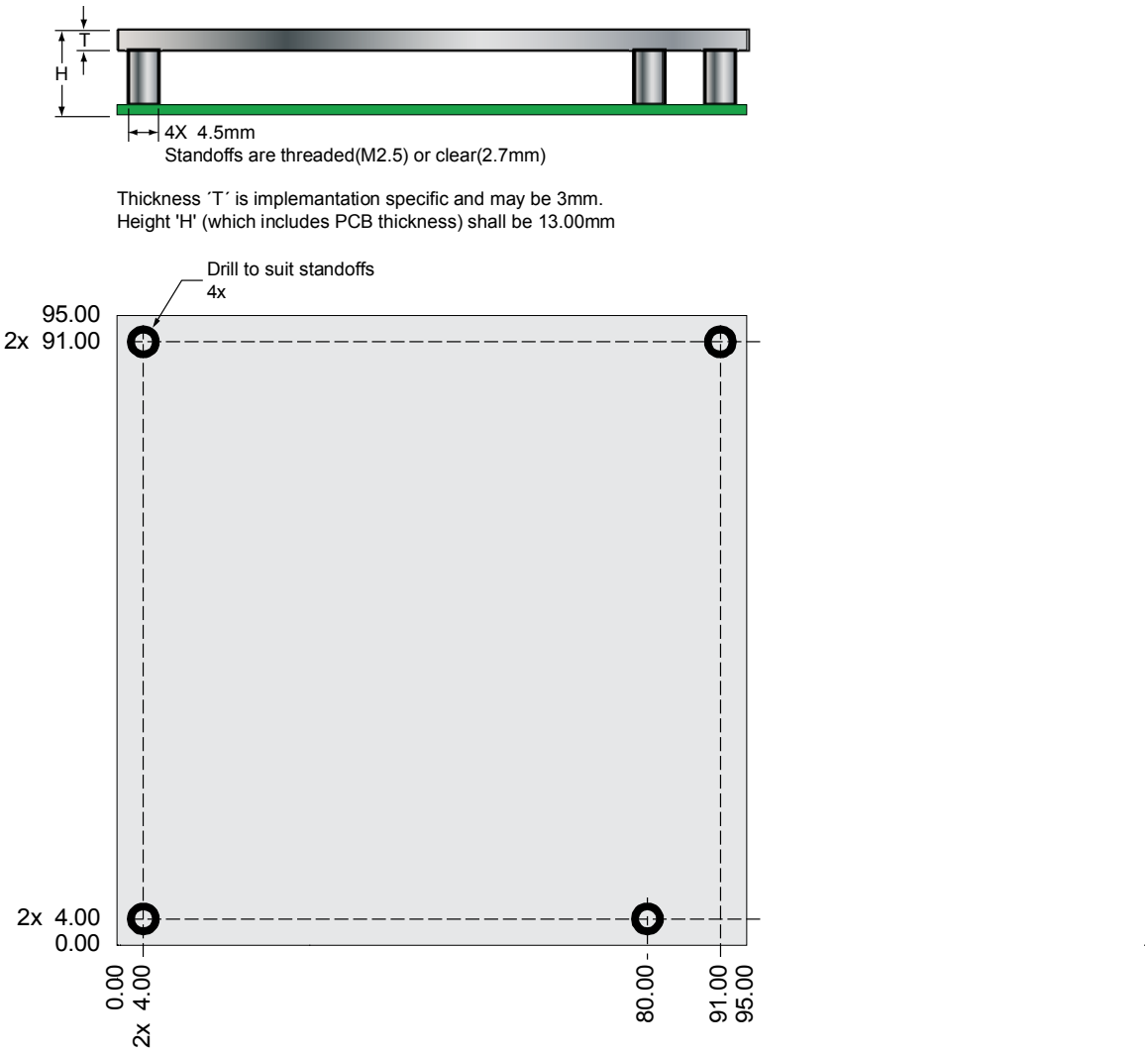
Figure 6-11: Mini Module Heat-Spreader



All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].
If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-11.

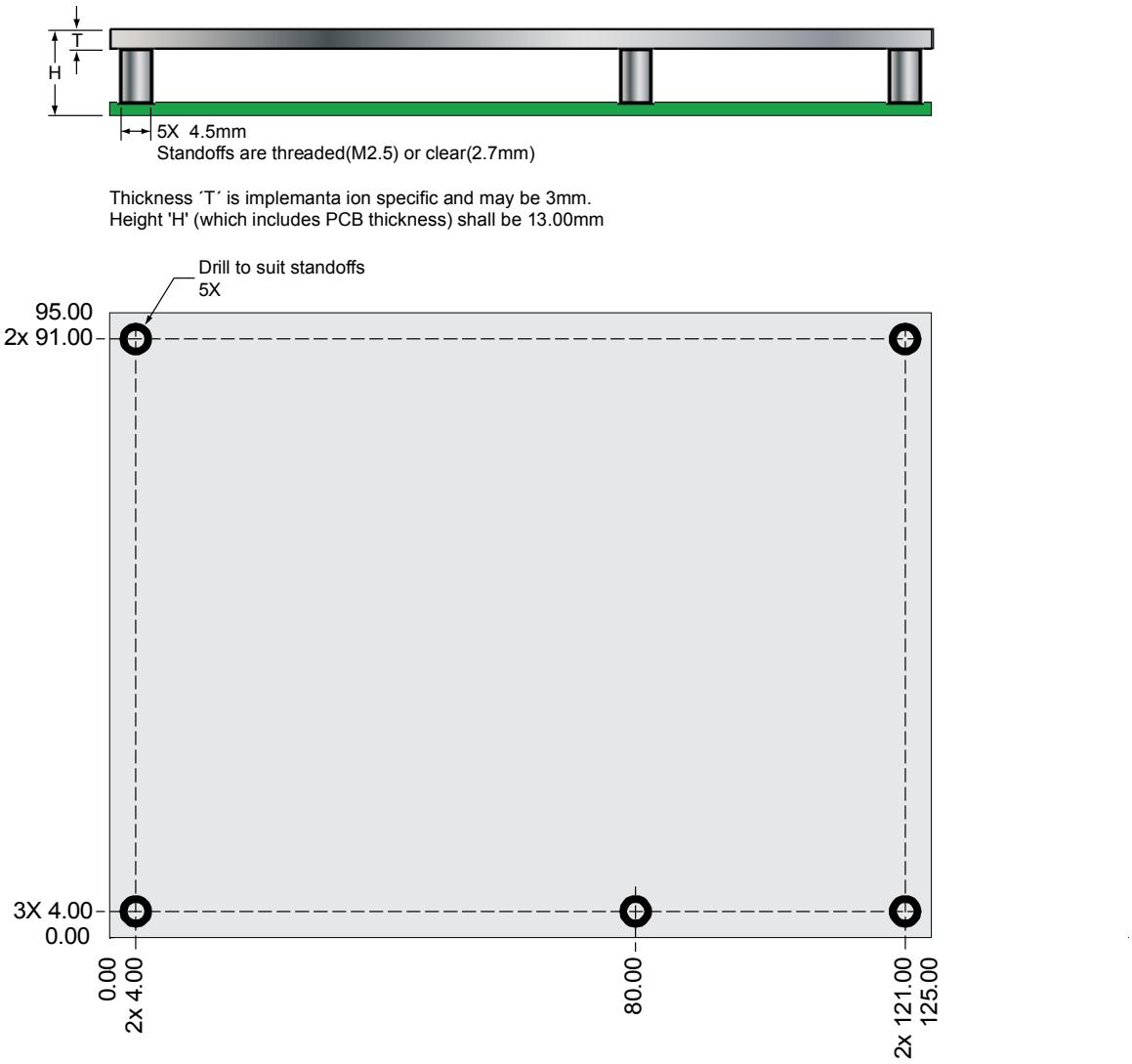
Figure 6-12: Compact Module Heat-Spreader



All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].
If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-12.

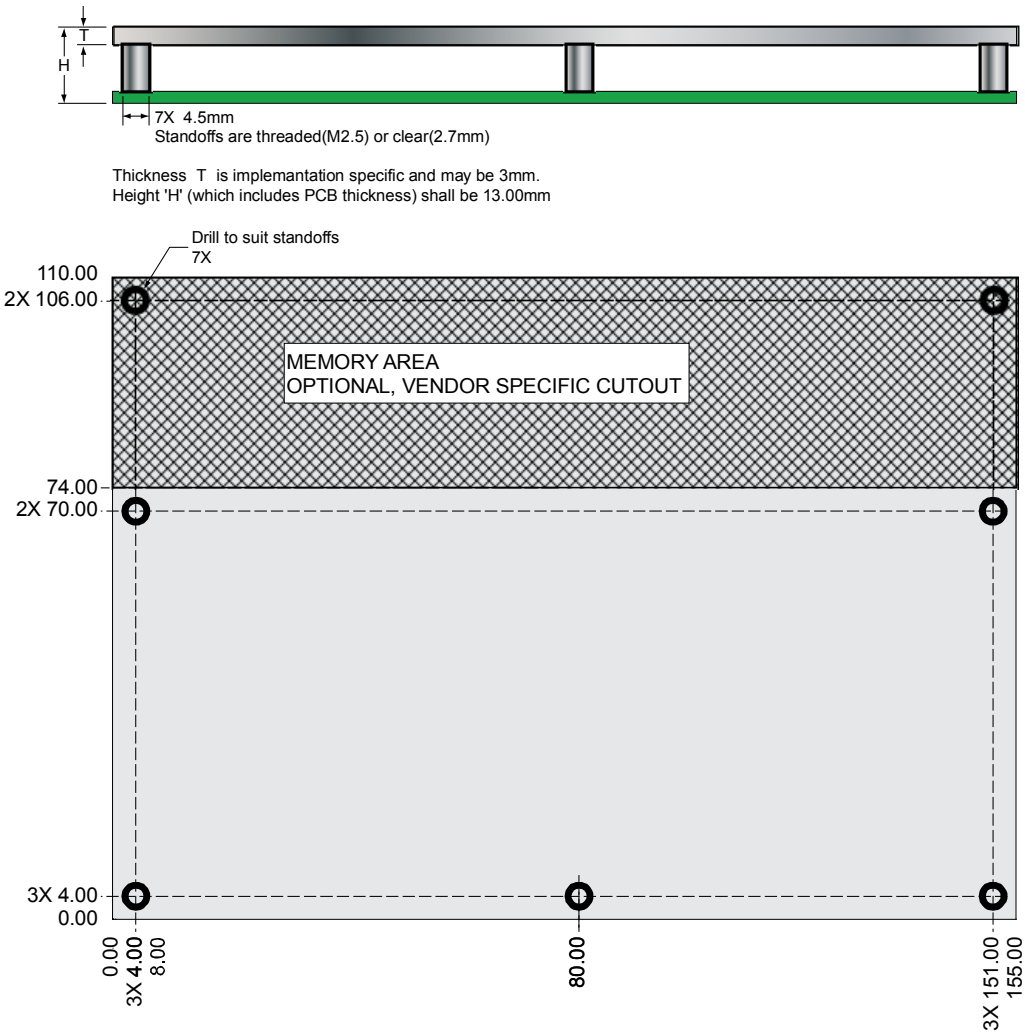
Figure 6-13: Basic Module Heat-Spreader



All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].
If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-13.

Figure 6-14: Heat-Spreader Specification for Extended Module



All dimensions are in mm.

X-Y tolerances ***shall*** be ± 0.3mm [±0.012"].
The Extended Module heat-spreader ***shall*** have minimum X-Y dimensions of 155 mm x 74 mm, as per the clear area in the figure above. The hatched area indicates the PCB area that ***may*** be used for memory Modules. The Extended Module heat-spreader ***may*** extend into the memory area. This extension is vendor specific. The maximum X-Y extent of the Extended Module heat-spreader ***shall*** be 155mm x 110mm.
If a heat-spreader is supported, it ***shall*** provide the mounting hole attachment points dimensioned in Figure 6-14.

6.11 Component Height - Module Back and Carrier Board Top

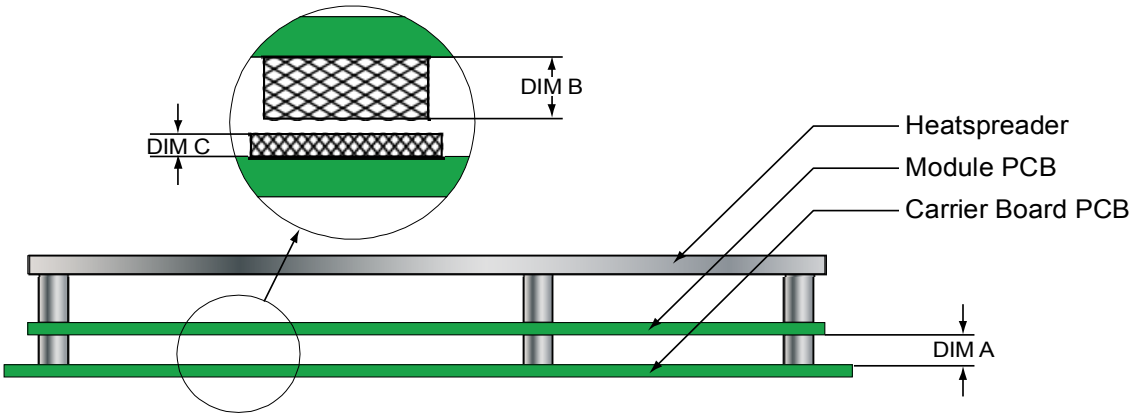
Parts mounted on the backside of the Module (in the space between the bottom surface of the Module PCB and the Carrier Board) ***shall*** have a maximum height of 3.8 mm (dimension 'B' in Figure 6-15).

It is likely that Mini size Modules will be used in space constrained applications such as hand held devices. In these applications the Module is commonly mounted directly to an enclosure without a heat-spreader. These applications would benefit from a reduced height that is possible with the lower power processors used on Mini Modules. The Mini size Modules allow for reduced component height on both the top and bottom of the Module. The Mini Module maximum top side and back side component height ***should*** be 3.0 mm.

With the 5 mm stack option, the clearance between the Carrier Board and the bottom surface of the Module's PCB is 5 mm (dimension 'A' in Figure 6-15). Using the 5 mm stack option, components placed on the Carrier Board topside under the Module envelope ***shall*** be limited to a maximum height of 1 mm (dimension 'C' in Figure 6-15), with the exception of the mating connectors. Using Carrier Board topside components up to 1mm allows a gap of 0.2 mm between Carrier Board Module bottom side components. This may not be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height ***should*** be restricted to a value less than 1mm that yields a clearance that is sufficient for the application.

If the Carrier Board uses the 8 mm stack option (dimension 'A' in Figure 6-15), then the Carrier Board topside components within the Module envelope ***shall*** be limited to a height of 4 mm (dimension 'C' in Figure 6-15), with the exception of the mating connectors. Using Carrier Board topside components up to 4mm allows a gap of 0.2 mm between Carrier Board topside components and Module bottom side components. This may not be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height ***should*** be restricted to a value less than 4 mm that yields a clearance that is sufficient for the application.

Figure 6-15: Component Clearances Underneath Module


DIM B
DIM C
Heatspreader
Module PCB
Carrier Board PCB
DIM A

7 Electrical Specifications

7.1 Input Power - General Considerations

The Compact, Basic and Extended Module Modules ***shall*** use a single main power rail with a nominal value of +12V.
The Mini Module shall support a wide range power supply of 4.75V to 20.0V.
In addition, the Mini Module ***shall*** be optimized for 5V operation and Module vendors ***should*** report Module power figures at 5V, 12V and 18V input voltages.
Two additional rails are specified: a +5V standby power rail and a +3V battery input to power the Module Real-time Clock (RTC) circuit in the absence of other power sources. The +5V standby rail ***may*** be left unconnected on the Carrier Board if the standby functions are not required by the application. Likewise, the +3V battery input ***may*** be left open if the application does not require the RTC to keep time in the absence of the main and standby sources. There ***may*** be Module specific concerns regarding storage of system setup parameters that ***may*** be affected by the absence of the +5V standby and / or the +3V battery.

The rationale for this power-delivery scheme is:

- Module pins are scarce. It is more pin-efficient to bring power in on a higher voltage rail.
- Single supply operation is attractive to many users.
- Lithium ion battery packs for mobile systems are most prevalent with a +14.4V output. This is well suited for the +12V main power rail.
- Contemporary chipsets have no power requirements for +5V other than to provide a reference voltage for +5V tolerant inputs. No COM Express Module pins are allocated to accept +5V except for the +5V standby pins. In the case of an ATX supply, the switched (non standby) +5V line would not be used for the COM Express Module, but it might be used elsewhere on the Carrier Board.

7.2 Input Power - Current Load

The Module connector pins limit the amount of power that can be brought into the COM Express Module. The limits are different for Module Pin-out Type 10 vs. Pin-out Types 6 and 7, based on the number of 12V power pins as Pin-out Type 10 has fewer pins available.

Table 7.1: Input Power - Pin-Out Type 10 Modules (Single Connector, 220 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	6	12	11.4 - 12.6	11.4	+/-100	68	85%	58
Wide input (Mini)	6		4.75 – 20.0	4.75	+/-100	28		
VCC_5V_SBY	2	5	4.75 - 5.25	4.75	+/-50	9		
VCC_RTC	0.5	3	2 0 - 3.3		+/-20			

Table 7.2: Input Power - Pin-Out Type 6/7 Modules (Dual Connector, 440 pins)

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max Input Ripple (mV)	Max Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max Load Power (Watts)
VCC_12V	12	12	11.4 - 12.6	11.4	+/-100	137	85%	116
VCC_5V_SBY	2	5	4.75 - 5.25	4.75	+/-50	9		
VCC_RTC	0.5	3	2 0 - 3.3		+/-20			

The ripple voltage, if present, must not cause the input voltage range to be exceeded.

7.3 Input Power - Sequencing

COM Express input power sequencing requirements are as follows:

VCC_RTC	***shall*** come up at the same time or before VCC_5V_SBY comes up[12]
VCC_5V_SBY	***shall*** come up at the same time or before VCC_12V comes up[12]
PWR_OK	***shall*** be active at the same time or after VCC_12V comes up[12]
PWR_OK	***shall*** be inactive at the same time or before VCC_12V goes down[12]
VCC_12V	***shall*** go down at the same time or before VCC_5V_SBY goes down
VCC_5V_SBY	***shall*** go down at the same time or before VCC_RTC goes down[12]
Wide input (Mini)	***shall*** follow the power sequencing of the VCC_12V

Figure 7-1: Power Sequencing

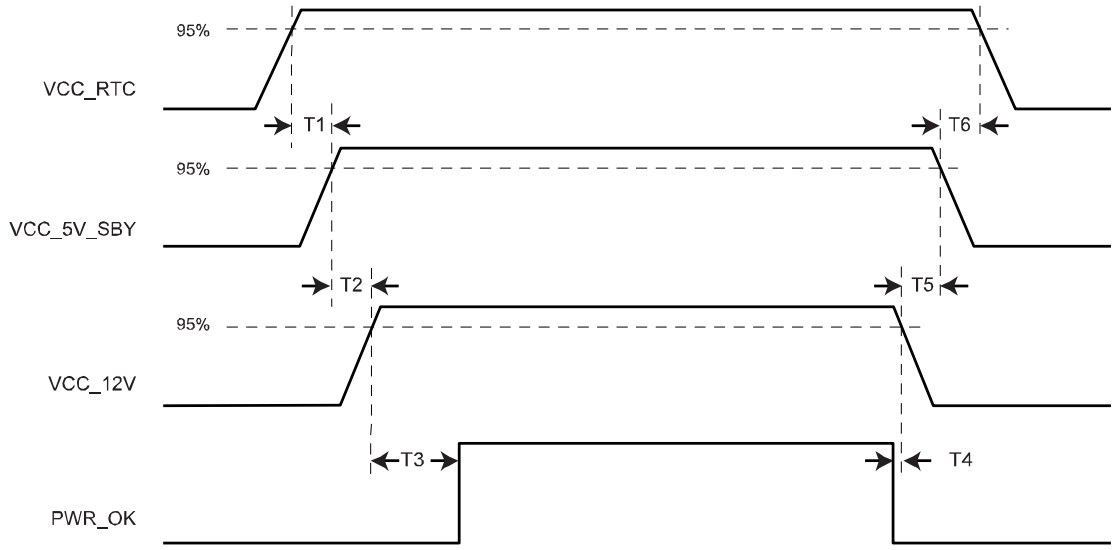


Table 7.3: Power Sequencing

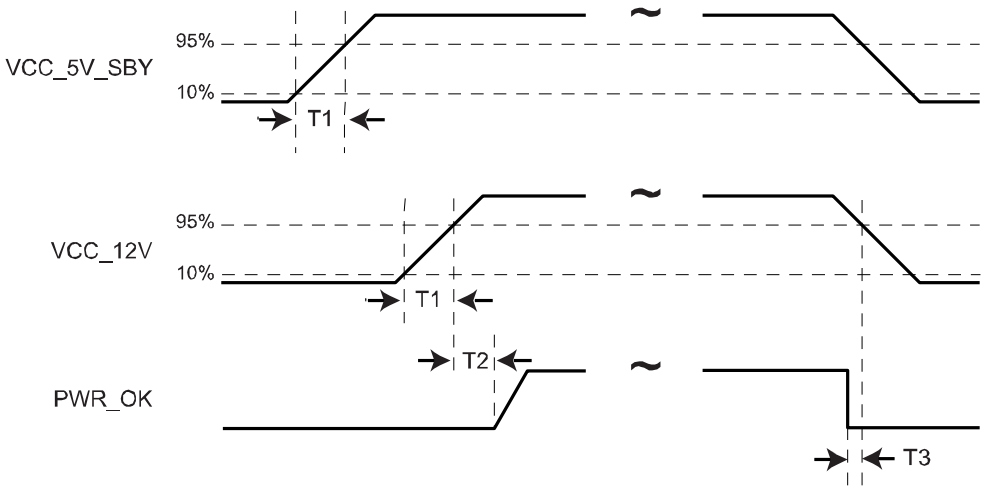
T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_12V rise	≥ 0 ms
T3	VCC_12V rise to PWROK rise	≥ 0 ms
T4	PWR_OK fall to VCC_12V fall	≥ 0 ms
T5	VCC_12V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

12 *If used*

7.4 Input Power - Rise Time

The input voltages to the COM Express Module VCC_12V, wide input (Mini) and VCC_5V_SBY if used ***shall*** rise from ≤10% of nominal to within the regulation ranges within 0.1 ms to 20 ms (0.1 ms ≤ T2 ≤ 20 ms). There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of its final set point within the regulation band. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive and have a value of between 0 V/ms and [Vout, nominal / 0.1] V/ms. Also, for any 5ms segment of the 10% to 90% rise time waveform, a straight line drawn between the end points of the waveform segment must have a slope ≥ [Vout, nominal / 20] V/ms.

Figure 7-2: Input Power Rise Time



- T1,min = 0,1ms
- T1,max = 20ms
- T2 ≥ 0ms
- T3 ≥ 0ms

The values chosen were selected to be compatible and enable use of ATX specification R2.2

7.5 Signal Integrity Requirements

The signal groups listed in the following table have signal-integrity concerns that ***should*** be accounted for in Module and Carrier Board designs. A general description is shown in the table for reference only. The designer ***should*** consult the relevant interface specification documents for complete information.

Table 7.4: Signal Integrity Requirements

Signal Group	General Description	Source Spec Reference
Gigabit Ethernet	Differential pairs	IEEE 802.3 Specification
LVDS	100Ω edge coupled differential pairs	National Semiconductor LVDS web site
PCI and LPC clocks	50Ω single ended ground-referenced	
PCI Express	Differential pairs	PCI SIG - PCI Express Specification
PCI Express clocks	100Ω edge couple differential pair, ground-referenced	
Serial ATA	Differential pairs	SATA Specification
USB	Differential pairs	USB 2.0 Specification
10GBASE-KR	Differential pairs	IEEE 802.3 Specification
USB SS	Differential pairs	USB 3.0 Specification
SPI	50Ω single ended ground-referenced	
eSPI	50Ω single ended ground-referenced	

8 Environmental Specifications

8.1 Thermal Specification

8.1.1 Objectives

Thermal specification requirements set forth here serve two objectives:

1. To provide a method through which any COM Express Module's thermal performance can be specified and verified against a common reference.
2. To provide a method of thermal specification that is independent of the particular components used on the Module.

These objectives are limited to the Modules' heat-spreader interface, and primary heat sources are limited to the Module itself and ambient air.

8.1.2 Definitions

Tcase. This is the temperature of the outside surface of the Module heat-spreader plate.

Tcase_max. The maxiumum temperature allowed for the heat-spreader of the Module at point M (defined below).

Tcase_min. This is defined as the minimum temperature allowed for the heat-spreader of the Module. This temperature is directly tied to minimum allowed junction temperatures of the chips that are in contact with the heat-spreader.

M. The point on the heat-spreader where the maximum case temperature must be measured.

Tambient_max. This is defined as the maximum temperature of the air directly surrounding the Module, allowed for the operation of the Module.

Tambient_min. This is defined as the minimum temperature of the air directly surrounding the Module, allowed for the operation of the Module.

TDPmax. This is defined as the maximum power dissipation of the Module for design of a thermal solution to guarantee that the Module operates within the manufacturer's specifications. TDP stands for thermal design power.

Tcpu_junction. The junction temperature of the processor. Tcpu_junction can be measured in many processors by accessing an on-die thermal diode. Refer to the manufacturer datasheet for information on how to access the thermal diode. In some instances, software provided by the processor manufacturer or a third party may be used in conjunction with hardware on the Module / Carrier Board assembly to monitor the temperature of the processor. Verification of an internal thermal diode accuracy should be done and certified by the OEM. With verified accuracy of the diode, validation with software can then be done by end users.

Tcpu_junction_max. The maximum junction temperature for the processor as specified in the silicon manufacturer's datasheet. The Module thermal solution (i.e. heat-spreader and heatsink) shall keep the processor junction temperature at or below the Tcpu_junction_max. Note that some manufacturers do not specify maximum junction temperatures but specify maximum case temperatures instead.

Tcpu_case. The CPU package case temperature, as specified in the silicon vendor's data sheet. Note that Tcpu_case and T_case may refer to different locations in the COM Express Module system.

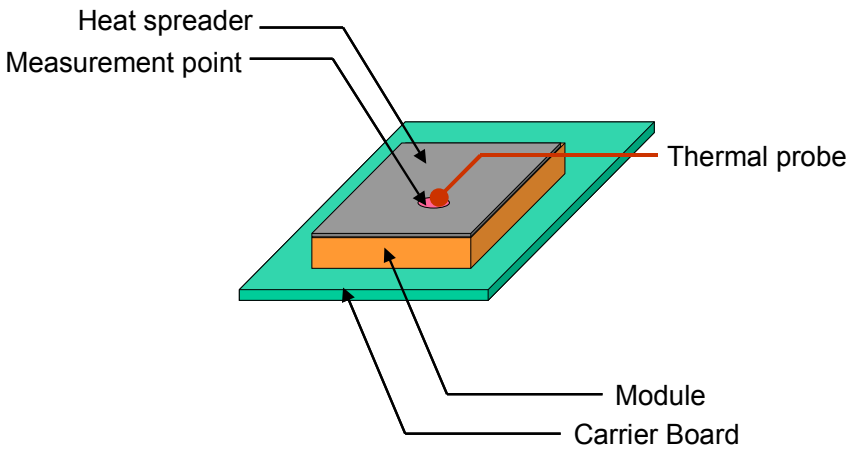
Tcpu_case_max. The maximum CPU package case temperature for the processor as specified in the silicon manufacturer's datasheet. The Module's thermal solution (i.e. heat-spreader and heatsink) shall keep the processor case temperature at or below the Tcpu_case_max. Note that some manufacturers do not specify maximum case temperatures but specify maximum junction temperatures instead.

The ultimate goal of the system thermal solution is to ensure that Tcpu_junction or Tcpu_case, whichever applies to the CPU at hand, remain below the maximum levels specified by the CPU vendor. Similar concerns apply to other high dissipation components in the Module system.

8.1.3 Tcase_max Measurement Setup

Measurements for Tcase_max ***should*** be performed according to a standardized method and under TDPmax conditions. The following figure depicts the standardized measurement setup for Tcase_max measurements.

Figure 8-1: Tcase_Max Measurement Point



Standardized setup for Tcase_max measurements.

This schematic illustration shows the Module heat-spreader, the Module, and the Carrier Board. Not shown is the user-specific cooling solution that is used to attach to the heat-spreader. Modules are not normally operated without a cooling solution attached.
The measurement point (M) ***should*** be specified, either through a permanent marker on the Module's heat-spreader, or through a mechanical drawing in the product's support documentation.

8.1.4 Module Thermal Specification Requirements

A Module manufacturer ***should*** specify Tcase_max, Tcase_min, Tambient_max, Tambient_min, TDPmax and M (the Tcase_max measurement point).
A Module manufacturer ***may*** specify Tcpu_junction_max and maximum junction temperatures of other critical chips on the Module. In this case, the Module vendor ***should*** provide software to read the junction temperature of the CPU and ***may*** do the same for the other critical chips. In that case, the Module vendor ***shall*** ensure that the software is properly calibrated and that the junction temperature readings are accurate.
The efficiency of the Module thermal characteristics has an impact on the Module's MTBF (Mean Time Between Failure). Higher junction temperatures result in a shorter silicon life. Module vendors ***should*** provide MTBF information.

8.1.5 Shock and Vibration

The shock and vibration characteristics of a system built with a COM Express Module will vary depending on system-implementation details. These details include size, rigidity, and mounting configuration of the Carrier Board and the thermal solution. There is no explicit shock and vibration specification that COM Express Modules are required to meet.

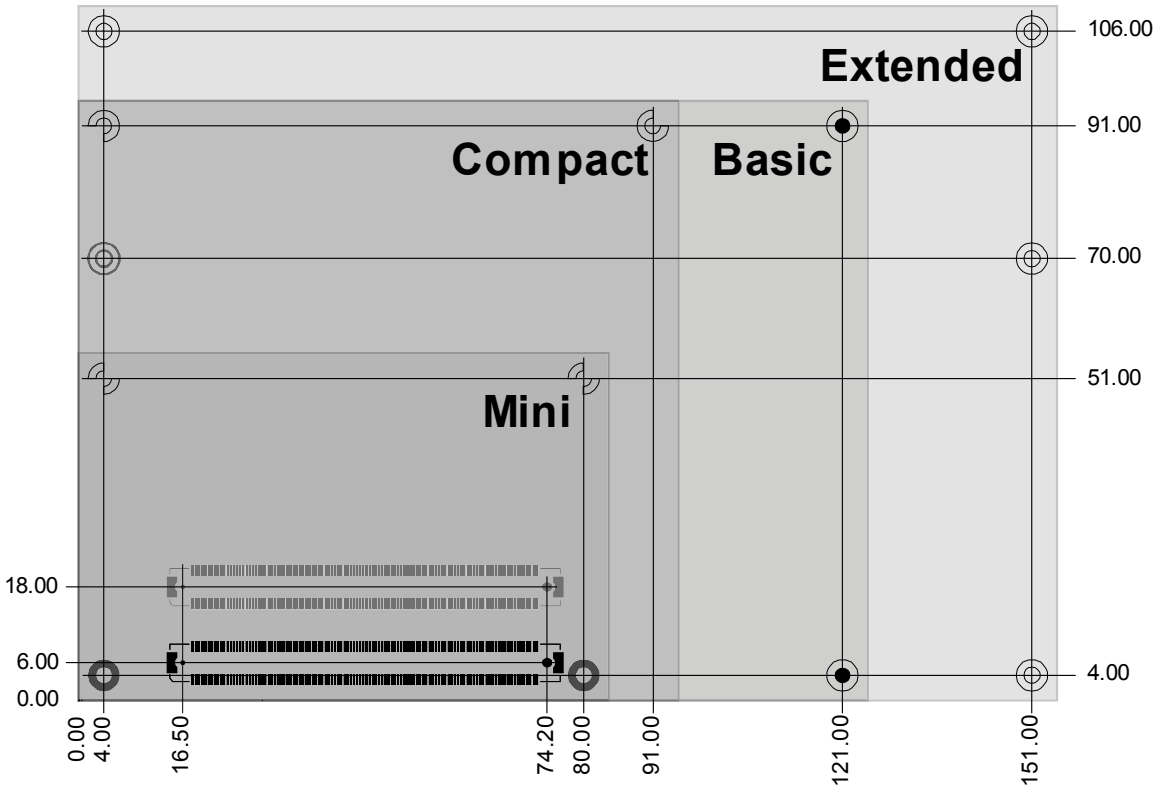
If all available COM Express Module and heat-spreader attachment points are used, then a COM Express based system should be capable of excellent shock and vibration performance.

9 Appendix

9.1 Mounting Positions and Connector Location for Carrier Boards

Figure 9-1: Carrier Board Mounting Positions

Common for all Form Factors
Extended only
Basic only
Compact only
Compact and Basic only
Mini only



All dimensions are shown in millimeters.

9.2 Changes in Type 6 from Revision 2.1 to Revision 3.0

Table 9.1: Comparison Type 6 Rev. 2.1 with Type 6 Rev 3.0

Type 6, Rev. 2.1				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
3	GBE0_MDI3+	LPC_FRAME#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1	GND	GND
6	GBE0_MDI2-	LPC_AD2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	LPC_DRQ0#	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK	USB_SSRX2+	USB_SSTX2+
18	SUS_S4#	SUS_STAT#	RSVD	RSVD
28	(S)ATA_ACT#	AC/HDA_SDIN2	RSVD	RSVD
29	AC/HDA_SYNC	AC/HDA_SDIN1	DDI1_PA R5+	DDI1_PAIR1+
30	AC/HDA_RST#	AC/HDA_SDIN0	DDI1_PA R5-	DDI1_PAIR1-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	AC/HDA_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	BIOS_DIS0#	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
47	VCC_RTC	EXCD1_PERST#	DDI3_PA R2-	DDI2_PAIR2-
48	EXCD0_PERST#	EXCD1_CPPE#	RSVD	RSVD
49	EXCD0_CPPE#	SYS_RESET#	DDI3_PA R3+	DDI2_PAIR3+
50	LPC_SERIRQ	CB_RESET#	DDI3_PA R3-	DDI2_PAIR3-
67	GPI2	WAKE1#	RSVD	GND

Type 6, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
3	GBE0_MDI3+	LPC_FRAME#/ **ESPI_CS0#**	USB_SSRX0-	USB_SSTX0-
4	GBE0_L NK100#	LPC_AD0/**ESPI_IO_0**	USB_SSRX0+	USB_SSTX0+
5	GBE0_L NK1000#	LPC_AD1/**ESPI_IO_1**	GND	GND
6	GBE0_MDI2-	LPC_AD2/**ESPI_IO_2**	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3/**ESPI_IO_3**	USB_SSRX1+	USB_SSTX1+
8	GBE0_L NK#	LPC_DRQ0#/ **ESPI_ALERT0#**	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#/ **ESPI_ALERT1#**	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK/**ESPI_CK**	USB_SSRX2+	USB_SSTX2+
18	SUS_S4#	SUS_STAT#/ **ESPI_RESET#**	RSVD	RSVD
28	(S)ATA_ACT#	HDA_SDIN2	RSVD	RSVD
29	HDA_SYNC	HDA_SDIN1	DDI1_PAIR5+	DDI1_PA R1+
30	HDA_RST#	HDA_SDIN0	DDI1_PAIR5-	DDI1_PA R1-
31	GND(FIXED)	GND(FIXED)	GND(FIXED)	GND(FIXED)
32	HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PA R2+
33	HDA_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PA R2-
34	BIOS_DIS0#/ **ESPI_SAFS**	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
47	VCC_RTC	**ESPI_EN#**	DDI3_PAIR2-	DDI2_PA R2-
48	**RSVD**	**USB0_HOST_PRSNT**	RSVD	RSVD
49	**GBE0_SDP**	SYS_RESET#	DDI3_PAIR3+	DDI2_PA R3+
50	LPC_SER RQ/ **ESPI_CS1#**	CB_RESET#	DDI3_PAIR3-	DDI2_PA R3-
67	GPI2	WAKE1#	**RAPID_SHUTDOWN**	GND

9.3 Comparison of Type 6 Revision 3.0 to Type 7

Table 9.2: Comparison Type 6 Rev. 2.1 with Type 7 Rev 3.0

Type 6, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
15	SUS_S3#	SMB_ALERT#	DDI1_PA R6+	DDI1_CTRLCLK_AUX+
16	SATA0_TX+	SATA1_TX+	DDI1_PA R6-	DDI1_CTRLDATA_AUX-
17	SATA0_TX-	SATA1_TX-	RSVD	RSVD
18	SUS_S4#	SUS_STAT#/ ESPI_RESET#	RSVD	RSVD
22	SATA2_TX+	SATA3_TX+	PCIE_RX7+	PCIE_TX7+
23	SATA2_TX-	SATA3_TX-	PCIE_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	DDI1_HPD	RSVD
25	SATA2_RX+	SATA3_RX+	DDI1_PA R4+	RSVD
26	SATA2_RX-	SATA3_RX-	DDI1_PA R4-	DDI1_PAIR0+
27	BATLOW#	WDT	RSVD	DDI1_PAIR0-
28	(S)ATA_ACT#	HDA_SD N2	RSVD	RSVD
29	HDA_SYNC	HDA_SD N1	DDI1_PA R5+	DDI1_PAIR1+
30	HDA_RST#	HDA_SD N0	DDI1_PA R5-	DDI1_PAIR1-
32	HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	HDA_SDOUT	I2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	BIOS_DIS0#/ ESPI_SAFS	I2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
35	THRMTRIP#	THRM#	RSVD	RSVD
36	USB6-	USB7-	DDI3_CTRLCLK_AUX+	DDI1_PAIR3+
37	USB6+	USB7+	DDI3_CTRLDATA_AUX-	DDI1_PAIR3-
38	USB_6_7_OC#	USB_4_5_OC#	DDI3_DDC_AUX_SEL	RSVD
39	USB4-	USB5-	DDI3_PA R0+	DDI2_PAIR0+
40	USB4+	USB5+	DDI3_PA R0-	DDI2_PAIR0-
42	USB2-	USB3-	DDI3_PA R1+	DDI2_PAIR1+
43	USB2+	USB3+	DDI3_PA R1-	DDI2_PAIR1-
44	USB_2_3_OC#	USB_0_1_OC#	DDI3_HPD	DDI2_HPD

Type 7, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
15	SUS_S3#	SMB_ALERT#	**10G_PHY_MDC_SCL3**	**10G_PHY_MDIO_SDA3**
16	SATA0_TX+	SATA1_TX+	**10G_PHY_MDC_SCL2**	**10G_PHY_MDIO_SDA2**
17	SATA0_TX-	SATA1_TX-	**10G_SDP2**	**10G_SDP3**
18	SUS_S4#	SUS_STAT#/ ESPI_RESET#	**GND**	**GND**
22	**PCIE_TX15+**	**PCIE_RX15+**	PC E_RX7+	PCIE_TX7+
23	**PCIE_TX15-**	**PCIE_RX15-**	PC E_RX7-	PCIE_TX7-
24	SUS_S5#	PWR_OK	**10G_INT2**	**10G_INT3**
25	**PCIE_TX14+**	**PCIE_RX14+**	**GND**	**GND**
26	**PCIE_TX14-**	**PCIE_RX14-**	**10G_KR_RX3+**	**10G_KR_TX3+**
27	BATLOW#	WDT	**10G_KR_RX3-**	**10G_KR_TX3-**
28	(S)ATA_ACT#	**RSVD**	**GND**	**GND**
29	**RSVD**	**RSVD**	**10G_KR_RX2+**	**10G_KR_TX2+**
30	**RSVD**	**RSVD**	**10G_KR_RX2-**	**10G_KR_TX2-**
32	**RSVD**	SPKR	**10G_SFP_SDA3**	**10G_SFP_SCL3**
33	**RSVD**	I2C_CK	**10G_SFP_SDA2**	**10G_SFP_SCL2**
34	BIOS_DIS0#/ ESPI_SAFS	I2C_DAT	**10G_PHY_RST_23**	**10G_PHY_CAP_23**
35	THRMTRIP#	THRM#	**10G_PHY_RST_01**	**10G_PHY_CAP_01**
36	**PCIE_TX13+**	**PCIE_RX13+**	**10G_LED_SDA**	**RSVD**
37	**PCIE_TX13-**	**PCIE_RX13-**	**10G_LED_SCL**	**RSVD**
38	**GND**	**GND**	**10G_SFP_SDA1**	**10G_SFP_SCL1**
39	**PCIE_TX12+**	**PCIE_RX12+**	**10G_SFP_SDA0**	**10G_SFP_SCL0**
40	**PCIE_TX12-**	**PCIE_RX12-**	**10G_SDP0**	**10G_SDP1**
42	USB2-	USB3-	**10G_KR_RX1+**	**10G_KR_TX1+**
43	USB2+	USB3+	**10G_KR_RX1-**	**10G_KR_TX1-**
44	USB_2_3_OC#	USB_0_1_OC#	**GND**	**GND**

Type 6, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
45	USB0-	USB1-	RSVD	RSVD
46	USB0+	USB1+	DDI3_PA R2+	DDI2_PAIR2+
47	VCC_RTC	ESPI_EN#	DDI3_PA R2-	DDI2_PAIR2-
48	RSVD	USB0_HOST_PRSNT	RSVD	RSVD
49	GBE0_SDP	SYS_RESET#	DDI3_PA R3+	DDI2_PAIR3+
50	LPC_SERIRQ/ ESPI_CS1#	CB_RESET#	DDI3_PA R3-	DDI2_PAIR3-
52	PCIE_TX5+	PC E_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PC E_RX5-	PEG_RX0-	PEG_TX0-
54	GPI0	GPO1	TYPE0#	PEG_LANE_RV#
55	PCIE_TX4+	PC E_RX4+	PEG_RX1+	PEG_TX1+
56	PCIE_TX4-	PC E_RX4-	PEG_RX1-	PEG_TX1-
58	PCIE_TX3+	PC E_RX3+	PEG_RX2+	PEG_TX2+
59	PCIE_TX3-	PC E_RX3-	PEG_RX2-	PEG_TX2-
61	PCIE_TX2+	PC E_RX2+	PEG_RX3+	PEG_TX3+
62	PCIE_TX2-	PC E_RX2-	PEG_RX3-	PEG_TX3-
65	PCIE_TX1-	PC E_RX1-	PEG_RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_RX4-	PEG_TX4-
68	PCIE_TX0+	PC E_RX0+	PEG_RX5+	PEG_TX5+
69	PCIE_TX0-	PC E_RX0-	PEG_RX5-	PEG_TX5-
71	LVDS_A0+	LVDS_B0+	PEG_RX6+	PEG_TX6+
72	LVDS_A0-	LVDS_B0-	PEG_RX6-	PEG_TX6-
73	LVDS_A1+	LVDS_B1+	GND	GND
74	LVDS_A1-	LVDS_B1-	PEG_RX7+	PEG_TX7+
75	LVDS_A2+	LVDS_B2+	PEG_RX7-	PEG_TX7-
76	LVDS_A2-	LVDS_B2-	GND	GND
77	LVDS_VDD_EN	LVDS_B3+	RSVD	RSVD
78	LVDS_A3+	LVDS_B3-	PEG_RX8+	PEG_TX8+
79	LVDS_A3-	LVDS_BKLT_EN	PEG_RX8-	PEG_TX8-
81	LVDS_A_CK+	LVDS_B_CK+	PEG_RX9+	PEG_TX9+
82	LVDS_A_CK-	LVDS_B_CK-	PEG_RX9-	PEG_TX9-

Type 7, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
45	USB0-	USB1-	**10G_PHY_MDC_SCL1**	**10G_PHY_MDIO_SDA1**
46	USB0+	USB1+	**10G_PHY_MDC_SCL0**	**10G_PHY_MDIO_SDA0**
47	VCC_RTC	ESPI_EN#	10G_ NT0	10G_INT1
48	RSVD	USB0_HOST_PRSNT	**GND**	**GND**
49	GBE0_SDP	SYS_RESET#	**10G_KR_RX0+**	**10G_KR_TX0+**
50	LPC_SER RQ/ ESPI_CS1#	CB_RESET#	**10G_KR_RX0-**	**10G_KR_TX0-**
52	PC E_TX5+	PCIE_RX5+	**PCIE_RX16+**	**PCIE_TX16+**
53	PC E_TX5-	PCIE_RX5-	**PCIE_RX16-**	**PCIE_TX16-**
54	GPI0	GPO1	TYPE0#	**RSVD**
55	PC E_TX4+	PCIE_RX4+	**PCIE_RX17+**	**PCIE_TX17+**
56	PC E_TX4-	PCIE_RX4-	**PCIE_RX17-**	**PCIE_TX17-**
58	PC E_TX3+	PCIE_RX3+	**PCIE_RX18+**	**PCIE_TX18+**
59	PC E_TX3-	PCIE_RX3-	**PCIE_RX18-**	**PCIE_TX18-**
61	PC E_TX2+	PCIE_RX2+	**PCIE_RX19+**	**PCIE_TX19+**
62	PC E_TX2-	PCIE_RX2-	**PCIE_RX19-**	**PCIE_TX19-**
65	PC E_TX1-	PCIE_RX1-	**PCIE_RX20+**	**PCIE_TX20+**
66	GND	WAKE0#	**PCIE_RX20-**	**PCIE_TX20-**
68	PC E_TX0+	PCIE_RX0+	**PCIE_RX21+**	**PCIE_TX21+**
69	PC E_TX0-	PCIE_RX0-	**PCIE_RX21-**	**PCIE_TX21-**
71	**PCIE_TX8+**	**PCIE_RX8+**	**PCIE_RX22+**	**PCIE_TX22+**
72	**PCIE_TX8-**	**PCIE_RX8-**	**PCIE_RX22-**	**PCIE_TX22-**
73	**GND**	**GND**	GND	GND
74	**PCIE_TX9+**	**PCIE_RX9+**	**PCIE_RX23+**	**PCIE_TX23+**
75	**PCIE_TX9-**	**PCIE_RX9-**	**PCIE_RX23-**	**PCIE_TX23-**
76	**GND**	**GND**	GND	GND
77	**PCIE_TX10+**	**PCIE_RX10+**	RSVD	RSVD
78	**PCIE_TX10-**	**PCIE_RX10-**	**PCIE_RX24+**	**PCIE_TX24+**
79	**GND**	**GND**	**PCIE_RX24-**	**PCIE_TX24-**
81	**PCIE_TX11+**	**PCIE_RX11+**	**PCIE_RX25+**	**PCIE_TX25+**
82	**PCIE_TX11-**	**PCIE_RX11-**	**PCIE_RX25-**	**PCIE_TX25-**

Type 6, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
83	LVDS_I2C_CK	LVDS_BKLT_CTRL	RSVD	RSVD
84	LVDS_I2C_DAT	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	RSVD	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	eDP_HPD	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF+	BIOS_DIS1#	PEG_RX11+	PEG_TX11+
89	PCIE_CLK_REF-	VGA_RED	PEG_RX11-	PEG_TX11-
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I2C_CK	PEG_RX13-	PEG_TX13-
96	TPM_PP	VGA_I2C_DAT	GND	GND
98	SER0_TX	RSVD	PEG_RX14+	PEG_TX14+
99	SER0_RX	RSVD	PEG_RX14-	PEG_TX14-
101	SER1_TX	FAN_PWMOUT	PEG_RX15+	PEG_TX15+
102	SER1_RX	FAN_TACH N	PEG_RX15-	PEG_TX15-

Type 7, Rev. 3.0				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
83	**GND**	**GND**	RSVD	RSVD
84	**NCSI_TX_EN**	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	**PCIE_RX26+**	**PCIE_TX26+**
86	RSVD	VCC_5V_SBY	**PCIE_RX26-**	**PCIE_TX26-**
87	**RSVD**	VCC_5V_SBY	GND	GND
88	**PCIE_CK_REF+**	BIOS_DIS1#	**PCIE_RX27+**	**PCIE_TX27+**
89	**PCIE_CK_REF-**	**NCSI_RX_ER**	**PCIE_RX27-**	**PCIE_TX27-**
91	SPI_POWER	**NCSI_CLK_IN**	**PCIE_RX28+**	**PCIE_TX28+**
92	SPI_MISO	**NCSI_RXD1**	**PCIE_RX28-**	**PCIE_TX28-**
93	GPO0	**NCSI_RXD0**	GND	GND
94	SPI_CLK	**NCSI_CRS_DV**	**PCIE_RX29+**	**PCIE_TX29+**
95	SPI_MOSI	**NCSI_TXD1**	**PCIE_RX29-**	**PCIE_TX29-**
96	TPM_PP	**NCSI_TXD0**	GND	GND
98	SER0_TX	**NCSI_ARB_IN**	**PCIE_RX30+**	**PCIE_TX30+**
99	SER0_RX	**NCSI_ARB_OUT**	**PCIE_RX30-**	**PCIE_TX30-**
101	SER1_TX	FAN_PWMOUT	**PCIE_RX31+**	**PCIE_TX31+**
102	SER1_RX	FAN_TACHIN	**PCIE_RX31-**	**PCIE_TX31-**

9.4 Type 10 Changes from Rev. 2.1 to Rev. 3.0.

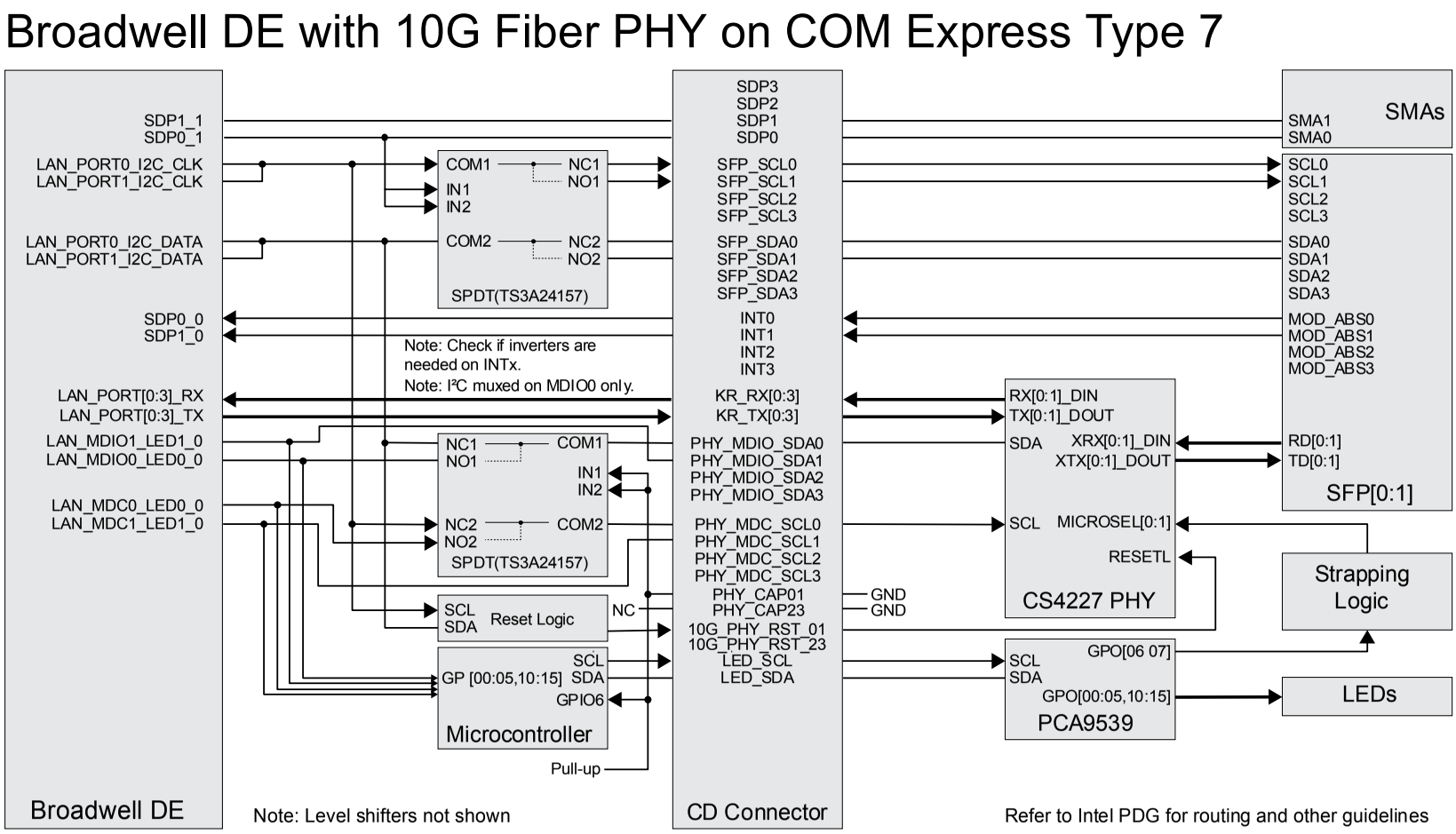
Table 9.3: Type 10 Rev. 2.1 to Rev. 3.0 Comparison

	Type 10 Rev. 2.1		Type 10 Rev. 3.0	
Pin	**Row A**	**Row B**	**Row A**	**Row B**
3	GBE0_MDI3+	LPC_FRAME#	GBE0_MDI3+	LPC_FRAME#/ **ESPI_CS0#**
4	GBE0_LINK100#	LPC_AD0	GBE0_LINK100#	LPC_AD0/ **ESPI_IO_0**
5	GBE0_LINK1000#	LPC_AD1	GBE0_LINK1000#	LPC_AD1/ **ESPI_IO_1**
6	GBE0_MDI2-	LPC_AD2	GBE0_MDI2-	LPC_AD2/ **ESPI_IO_2**
7	GBE0_MDI2+	LPC_AD3	GBE0_MDI2+	LPC_AD3/ **ESPI_IO_3**
8	GBE0_LINK#	LPC_DRQ0#	GBE0_LINK#	LPC_DRQ0#/ **ESPI_ALERT0#**
9	GBE0_MDI1-	LPC_DRQ1#	GBE0_MDI1-	LPC_DRQ1#/ **ESPI_ALERT1#**
10	GBE0_MDI1+	LPC_CLK	GBE0_MDI1+	LPC_CLK/ **ESPI_CK**
18	SUS_S4#	SUS_STAT#	SUS_S4#	SUS_STAT#/ **ESPI_RESET#**
28	(S)ATA_ACT#	AC/HDA_SDIN2	(S)ATA_ACT#	HDA_SDIN2
29	AC/HDA_SYNC	AC/HDA_SDIN1	HDA_SYNC	HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0	HDA_RST#	HDA_SDIN0
32	AC/HDA_BITCLK	SPKR	HDA_BITCLK	SPKR
33	AC/HDA_SDOUT	I2C_CK	HDA_SDOUT	I2C_CK
34	BIOS_DIS0#	I2C_DAT	BIOS_DIS0#/ **ESPI_SAFS**	I2C_DAT
47	VCC_RTC	EXCD1_PERST#	VCC_RTC	**ESPI_EN#**
48	EXCD0_PERST#	EXCD1_CPPE#	**RSVD**	**USB0_HOST_PRSNT**
49	EXCD0_CPPE#	SYS_RESET#	**GBE0_SDP**	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#	LPC_SERIRQ/ **ESPI_CS1#**	CB_RESET#
89	PCIE_CLK_REF-	DDI0_HPD	PCIE_CLK_REF-	DDI0_HPD
96	TPM_PP	USB_HOST_PRSNT	TPM_PP	**USB7_HOST_PRSNT**

9.5 Example 10 GB Ethernet Designs

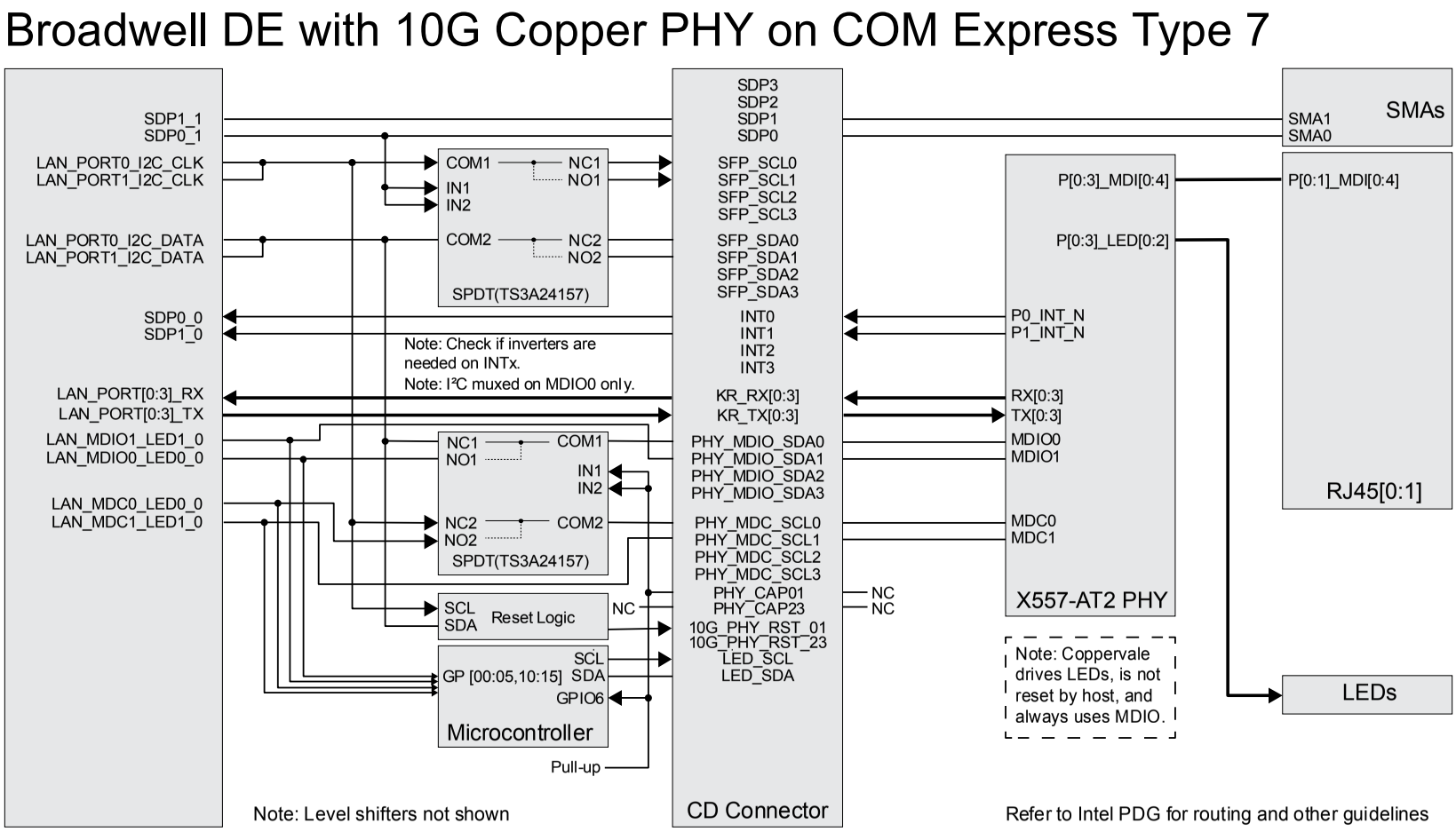
9.5.1 2016 Silicon 10GbE Fiber Implementation

Figure 9-2: 10G Ethernet Design for Fiber PHY with Broadwell DE



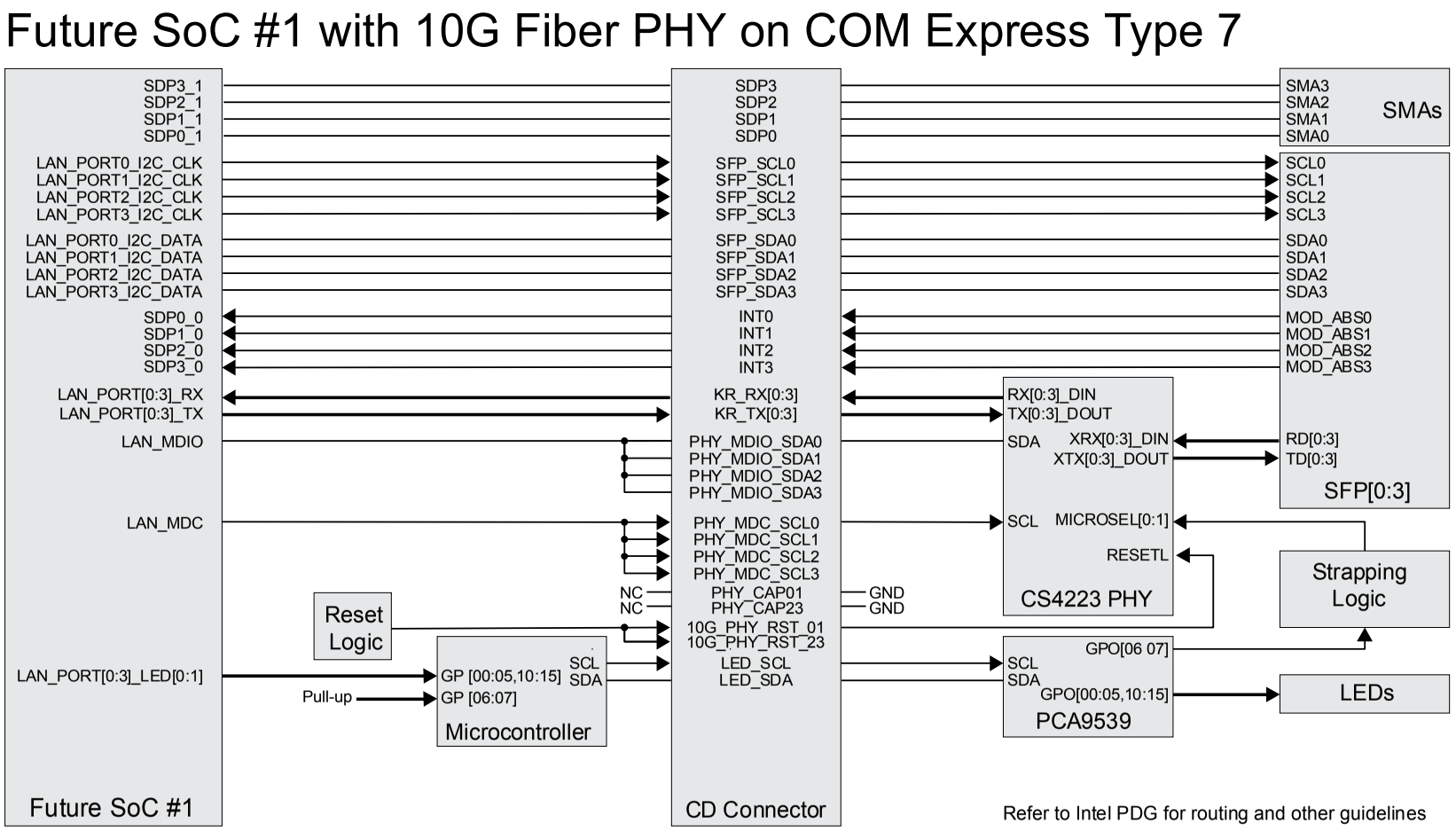
9.5.2 2016 Silicon 10GbE Copper Implementation

Figure 9-3: 10G Ethernet Design for Copper PHY with Broadwell DE



9.5.3 Future Silicon 10GbE Fiber Implementation

Figure 9-4: 10G Ethernet Design for Fiber PHY with Future SoC



9.5.4 Future Silicon 10GbE Copper Implementation

Figure 9-5: 10G Ethernet Design for Copper PHY with Future SoC