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32	RT8120_DDR_BEAD (REV0.2)
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36	NCT3933
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39	DVI CONN (REV0.82)
40	Dual DP (REV0.82)
41	F_PANEL (REV0.82)
42	R_USB30 (REV0.82)
43	INTEL I219 (REV1.11)
44	USB30_LAN CONNECTOR-I219
45	Realtek ALC892 (REV0.1)
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48	F_USB30 (REV0.82)
49	F_USB (REV0.82)
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51	CPU POWER-Z系列 (REV0.23)
52	EMI-ESD (REV0.1)
53	POWER MAP
54	NTC MAP
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Model Name: GA-Z270M-D3P

rev 1.01

Circuit or PCB layout change

Component value change history

2015/08/19

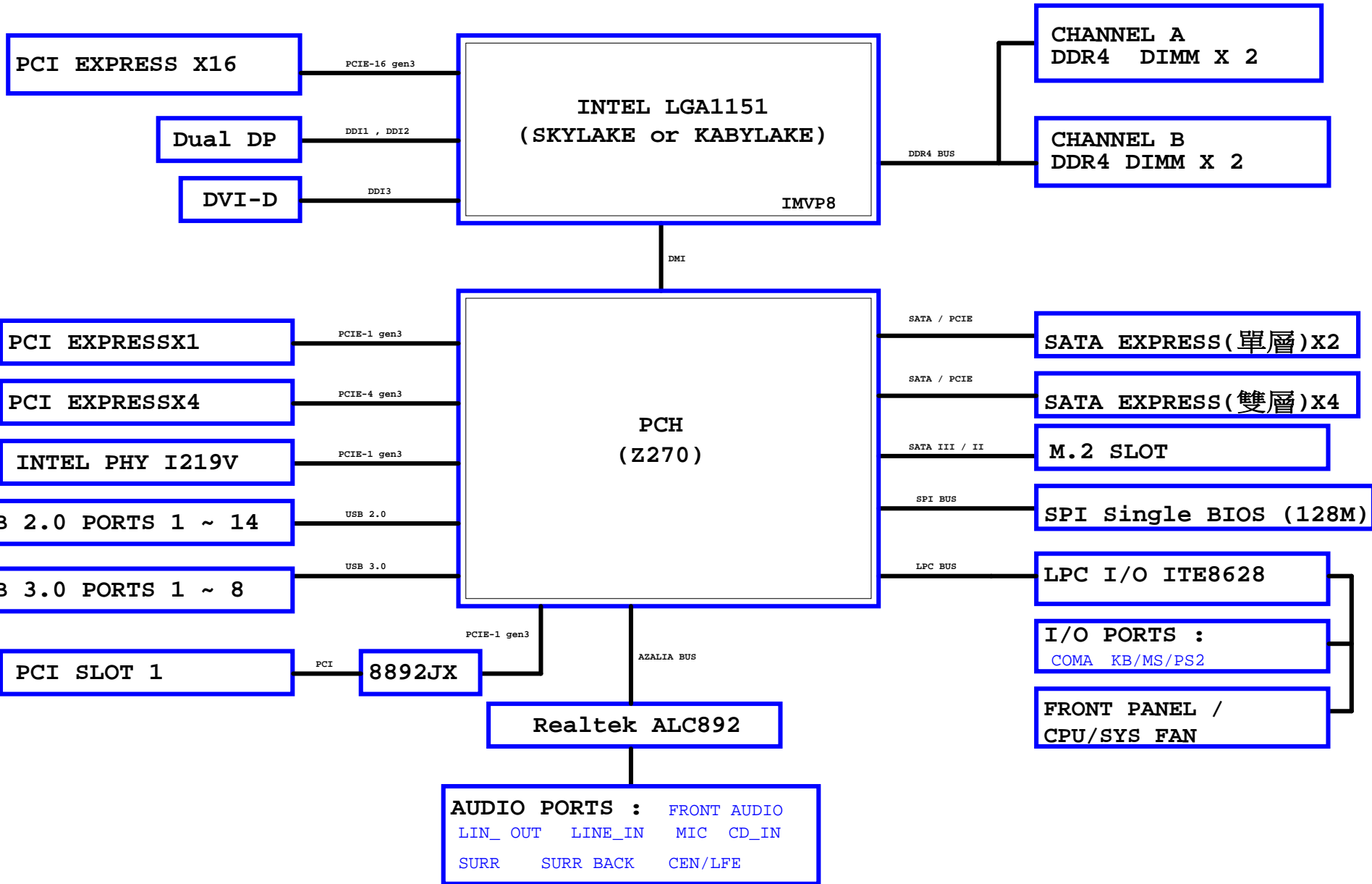
Data	Change Item	Reason
2016/07/04	first release	
	9MZ27MD3P-WG-01 BOM	
2016/09/06	9MZ27MD3P-WG-10A BOM	
	Rename PCH_CPUCLK->N_CPUCLK, BIOS->64M/Q/SPI/S08/S	
	Rename Net PQ->PP, SYS_FAN3 Rename SYS_FAN3_PUMP	
	OR56->8.2K/X, Add Net -SPI_HOLD_B, Add BSR1, BSR17, Add N_GGP_C15 For PWM MB_ID	
	, Add Net -SPI_HOLD_B, Add BSR1, BSR17, Add N_GGP_C15 For PWM MB_ID	
	, DIP 螺柱->CR/[12KSF-F10303-11R], Del OR4, NC2->22p/4/NPO/50V/J	
	DA_DL1, DC_DL1, DB_DL1, DD_DL1, DAL1, DM_DL1, DN_DL1->0.5uH/40A/IMD109/BP/D	
	, MA_L1->1uH/35A/IMD109/BP/D, NPL2->1uH/18A/IMD0809/BP/D	
	, OR79->75K/6/1, KB_MS_USB->KB/USB/A/PC99(DUAL)/GF/2/RA/D	
	Del Net CLKOUT_SRC_N_15, CLKOUT_SRC_P_15, MA_L3->1.0uH/15A/S/6.7m	
	PCIE16->BK Slot, PCIE4->BK Slot, DCL1, DCL2, DCL3, DCL4->1.0uH/15A/S/6.7m	
	DAC10->1.2n, DAR35->80.6K, DAC11->68P, DAR55->28K, DAR72->73.2K, DAC44->0.022u/4/X7R/25V/K	
	LED2, LED3->47/12 Footprint: POLYSWITCH-1206-1, Rename 42A, 60A, 80A, 110A->42, 60, 80, 110	
	MABC8->2.2u/4/X5R/6.3V/M, DDR4_4, DDR4_3->DDR4/288/BK/VA/D/GF/TWO LATCH	
	DDR4_2, DDR4_1->DDR4/288/GY/VA/D/GF/TWO LATCH, SIO->IT8686E/CX/S	
	Del N_SUSCLK, TBC3 Net->TPMCLK, 0 Ohm->short pad, OR89->22/4	
	DCL1, DCL2, DCL3, DCL4->1.0uH/15A/S/6.7m, DAU1->95866, Add DAN7C2	
2016/09/08	9MZ27MD3P-WG-10B BOM	
	全台系固態電容100uF, 270uF, 560uF	
2016/11/21	9MZ27MD3P-WG-10C BOM	
	DCR22->X, LED2, LED3->X, W_OVR8改上件, W_OVR9->X, DAC10->1.5n/4/X7R/50V/K, DAR37->2.74K	
	PCH->10HB1-03Z270-20R, DAR47->16.9K, DAR67->14K, MOS->ON	
	F_USB30_1, F_USB30_2->BH/2*10K20/BK/ON/2.0/VA/USB3.0/PRT	
2016/12/19	9MZ27MD3P-00-10D BOM	
	TMOS->12SP2-S09425-N1R/N2R/N3R, PAEC1, DAEC14, DAEC15, DAEC16->270u/FP/D/16V/88/A/12m	
	GR44->12K	

DATE	Change Item	Reason
2016/07/01 BOM:0.1	1.PCB first release	
	2.線路由Z170M-D3P-WG Rev1.0修改	
2016/09/05 BOM:1.0	Rename PCH_CPUCLK->N_CPUCLK, Del OR4,	
	Rename Net PQ->PP, SYS_FAN3 Rename SYS_FAN3_PUMP	
	, Add Net -SPI_HOLD_B, Add BSR1, BSR17, Add N_GGP_C15 For PWM MB_ID	
	KB_MS_USB->KB/USB/A/PC99(DUAL)/GF/2/RA/D	
	Del Net CLKOUT_SRC_N_15, CLKOUT_SRC_P_15,	
	LED2, LED3 Footprint: POLYSWITCH-1206-1, Rename 42A, 60A, 80A, 110A->42, 60, 80, 110	
	Del N_SUSCLK, TBC3 Net->TPMCLK, 0 Ohm->short pad, OR89->22/4	
2016/11/17 BOM:1.01	WR59, WR60, WR61->0/4/X, Rename SYS_FAN3, NR32, NR174->SHORT PAD	
	GR70, GR78, GR66->0402 SHORT PAD, GL14, GL10, GL16, GL17, GR73->0603 SHORT PAD	
	Add N_SUSCLK, NR286 SHORT PAD, MOS_H51 Rename TMOS	
	Del MAR25, MC20, MR26, Add MABC6, Add DCC1, DCC2, DCC3, Del DC_SBC7, SBC8	
	Add DCC54, DCC51, DCC52, DCC43, DCC54	

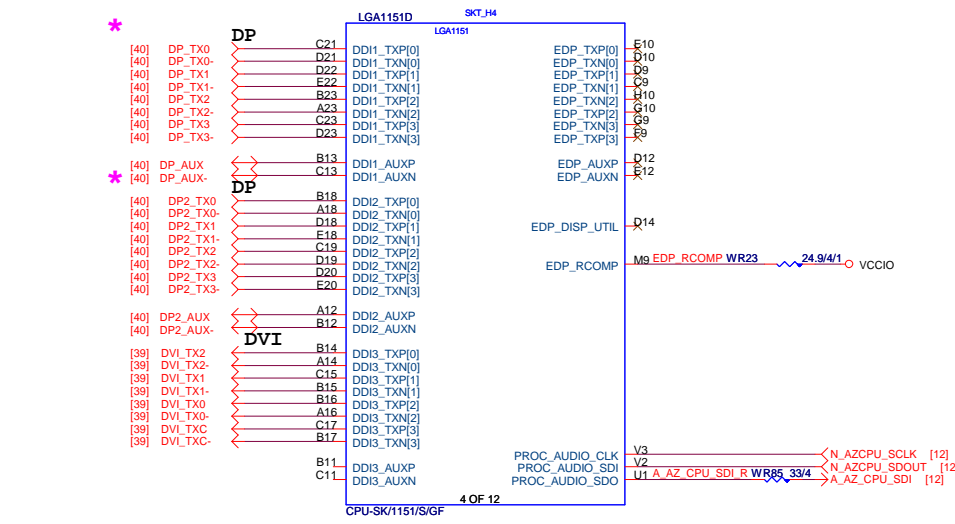
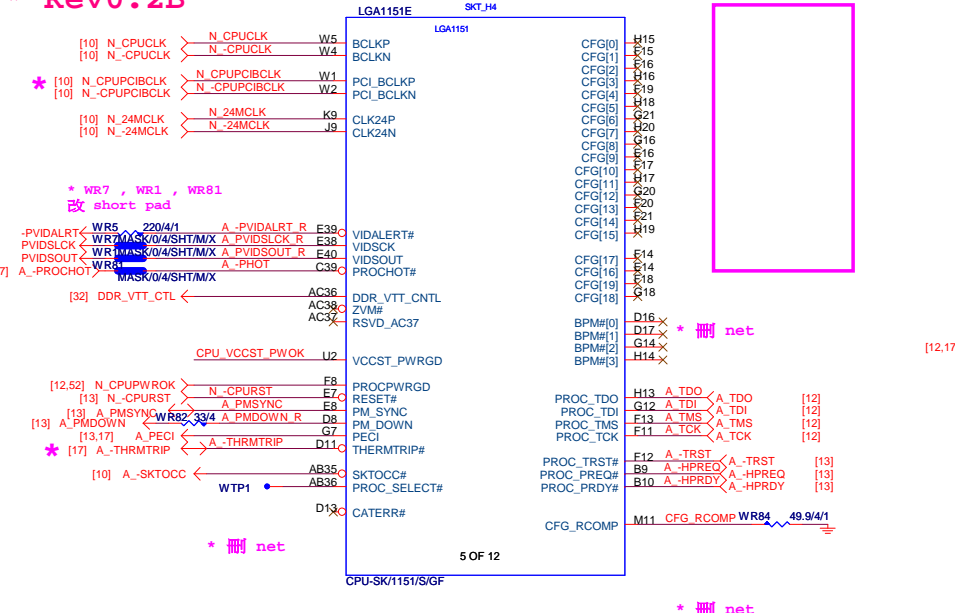
**GIGABYTE**™

Title				BOM & PCB MODIFY HISTORY	
Size	Document Number	GA-Z270M-D3P		Rev	1.01
Date:	Monday, December 19, 2016	Sheet	2	of	55

# BLOCK DIAGRAM

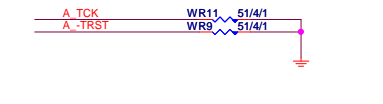
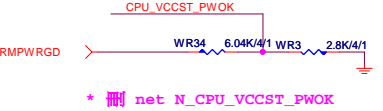
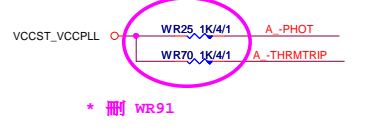
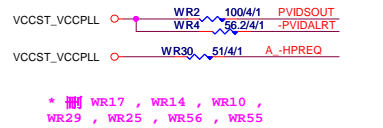


**\* Rev0.2B**



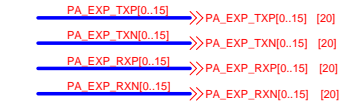
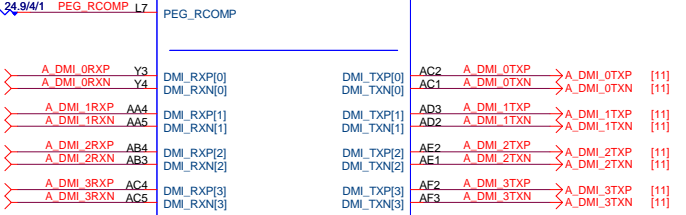
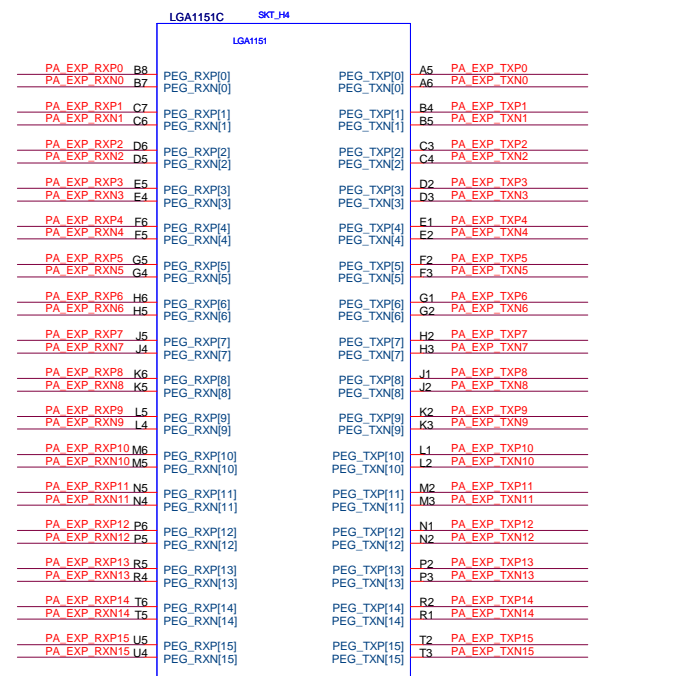
G-15u : (CPU-SK/1151/S/15)  
 10SCL-F01151-11R / 10SCL-F01151-12R  
 G-FL : (CPU-SK/1151/S/GF)  
 10SCL-F01151-21R / 10SCL-F01151-22R

-----  
 4 layer HDMI/DP/eDP/=====4/4///15  
 6 layer HDMI/DP/eDP/=====4/5.5/4//15  
 -----  
 Impedance=85 +- 15%



CFG[2]:xl6 Lane Numbering  
 Reversal. 1=  
 NORMAL/0=reversal  
 CFG[4]: eDP  
 enable:1:disable/0=enable  
 CFG[6:5]:PCI Express\* Bifurcation; 11=  
 1 x16 PCI Express;10=2x8 PCI Express  
 CFG[7]: PEG Training;1=(default) PEG Train  
 immediately following RESET#;0=PEG Wait  
 for BIOS

Bifurcation Config.	Signals	Lanes	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1	1	1
1x16 Reversed	1	1	0	1	1
2x8	1	0	0	1	1
2x8 Reversed	1	0	0	1	1
1x8+2x4	0	0	0	1	1
1x8+2x4 Reversed	0	0	0	0	1



-----  
 4 layer PEG/DMI=====4/4///15  
 6 layer PEG/DMI=====4/5.5/4//15  
 -----

Impedance=85 +- 15%  
 W=12 mil out of CPU  
 S=15 mil out of CPU

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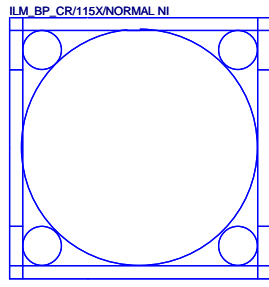
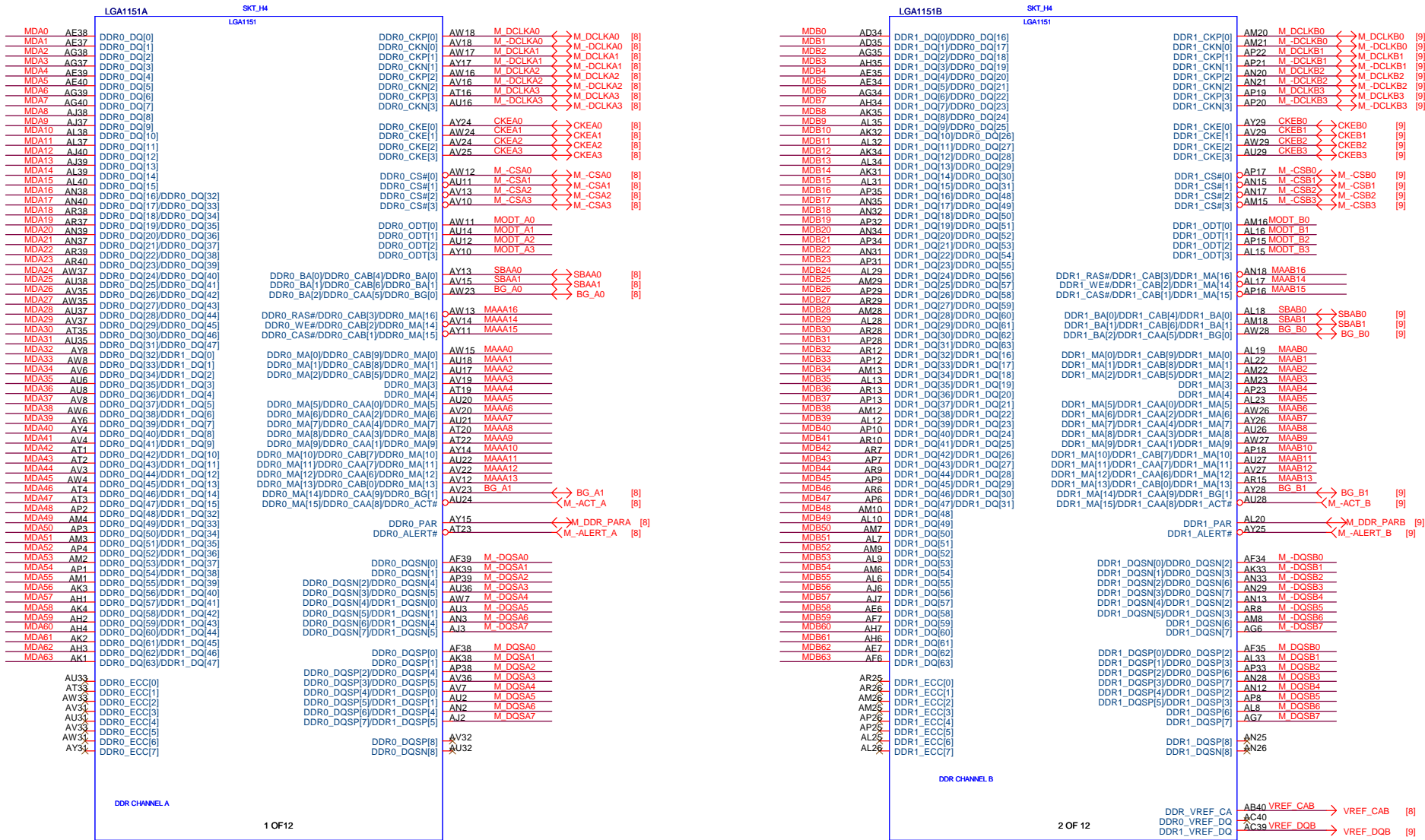
**CPU LGA1151-A**

**GA-Z270M-D3P**

Rev **1.0**

Size: Document Number  
 Custom: \_\_\_\_\_  
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\* 改DDR4 net



Need check the new CPU ME

- [8] MODT\_A[0..3] ↔ MODT\_A[0..3]
- [9] MODT\_B[0..3] ↔ MODT\_B[0..3]
- [8] MDA[0..63] ↔ MDA[0..63]
- [9] MDB[0..63] ↔ MDB[0..63]
- [8] M-QDSA[0..7] ↔ M-QDSA[0..7]
- [8] M-QDSB[0..7] ↔ M-QDSB[0..7]
- [8] MAA[0..16] ↔ MAA[0..16]
- [9] MAAB[0..16] ↔ MAAB[0..16]
- [9] M-QDSB[0..7] ↔ M-QDSB[0..7]
- [9] M-QDSB[0..7] ↔ M-QDSB[0..7]

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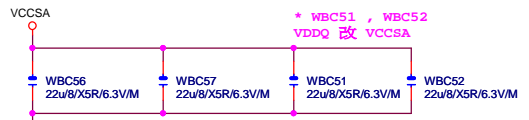
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**Size** Document Number

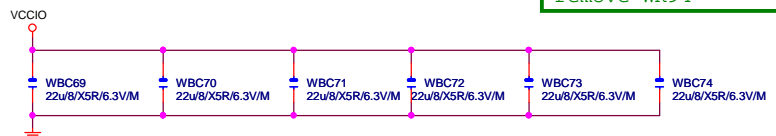
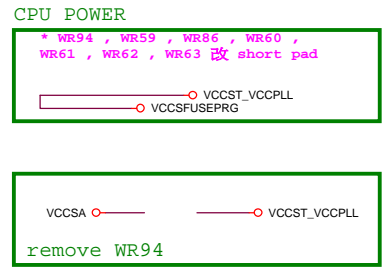
**Custom** GA-Z770M-D3P **Rev** 1.01

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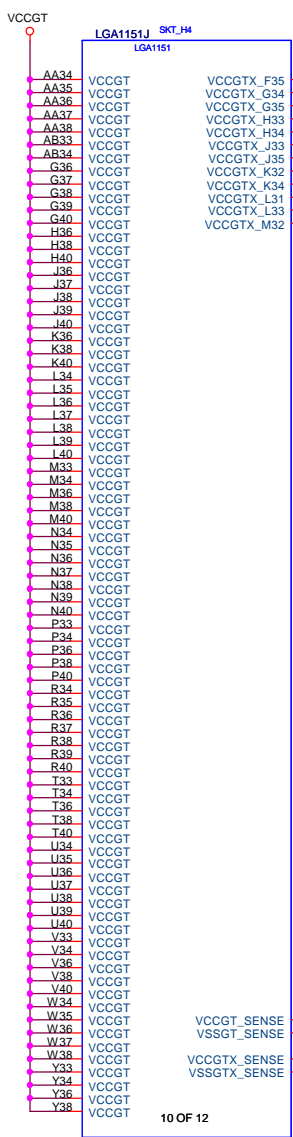
\* WBC49 移到 RT8120\_DDR  
\* 删 WBC50 电容



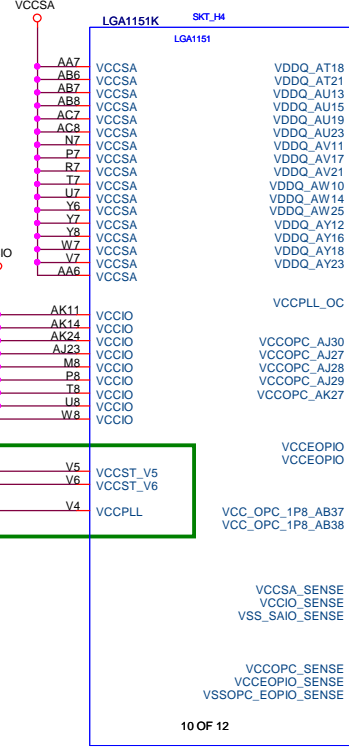
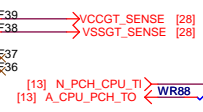
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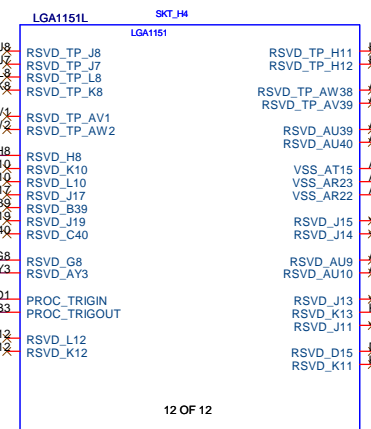
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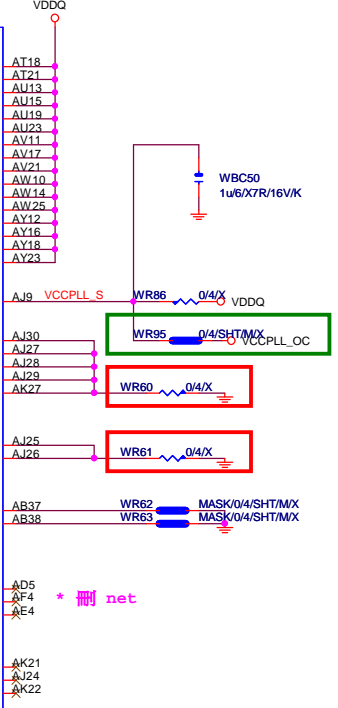
CPU-SK/1151/S/GF



CPU-SK/1151/S/GF

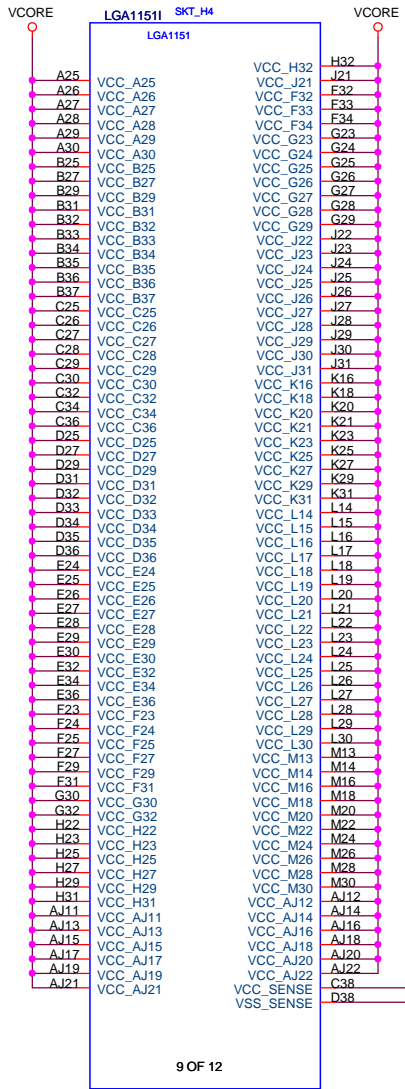


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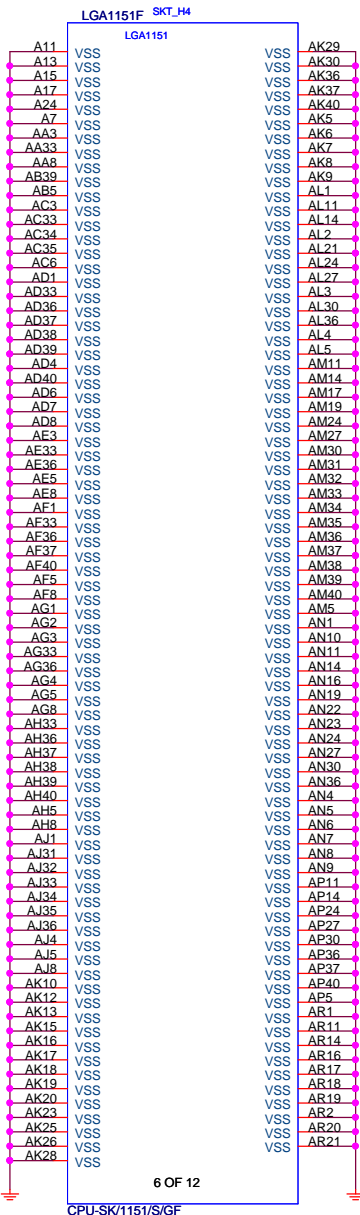
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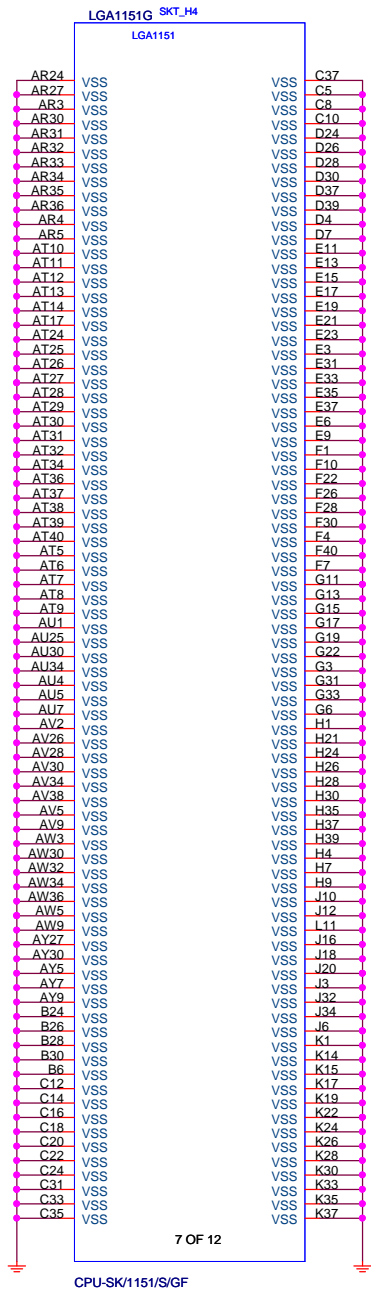


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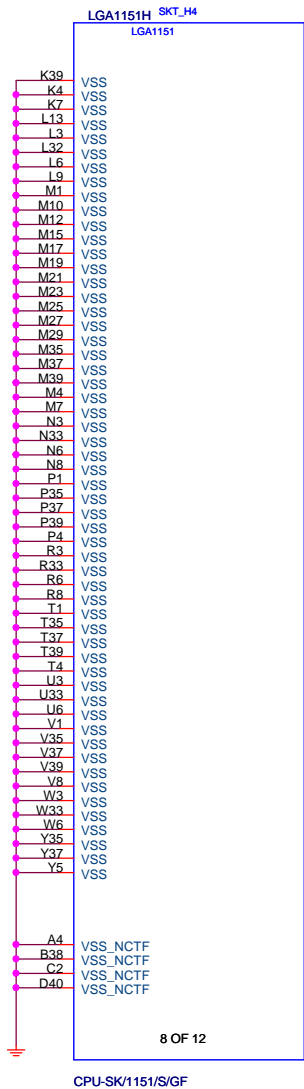
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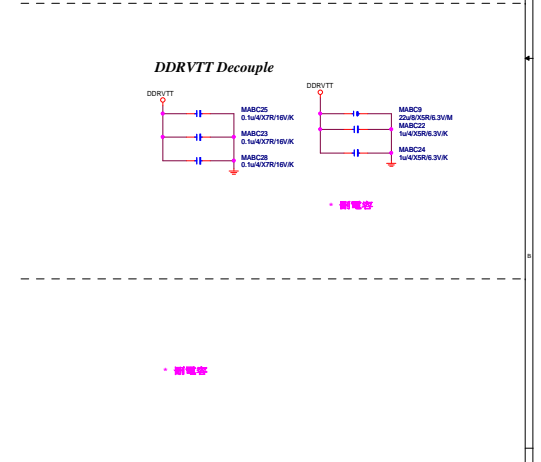
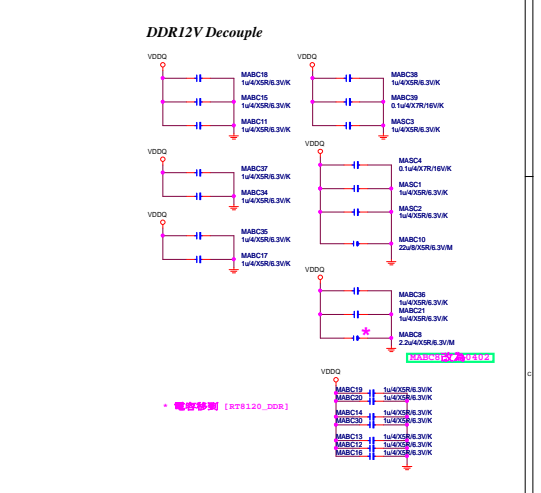
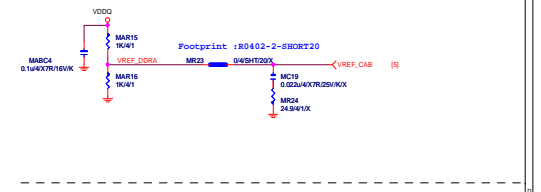
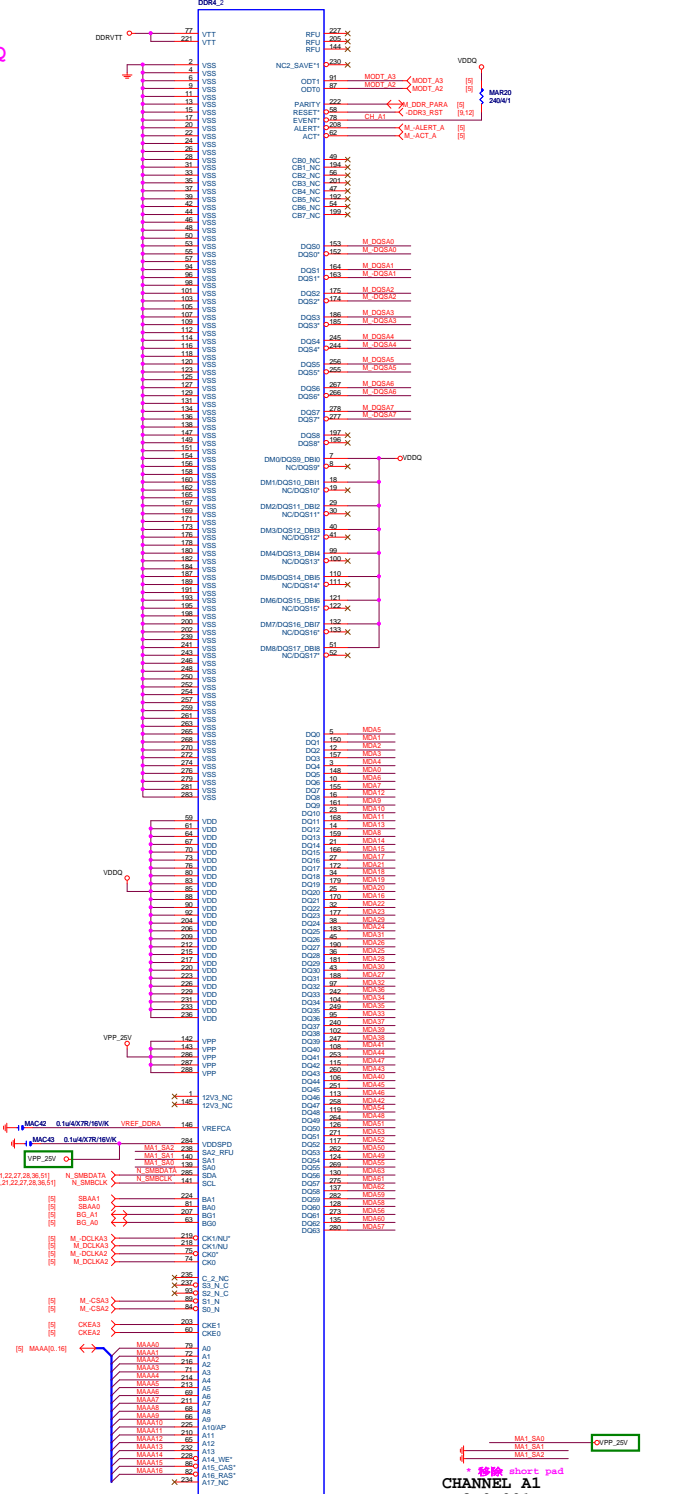
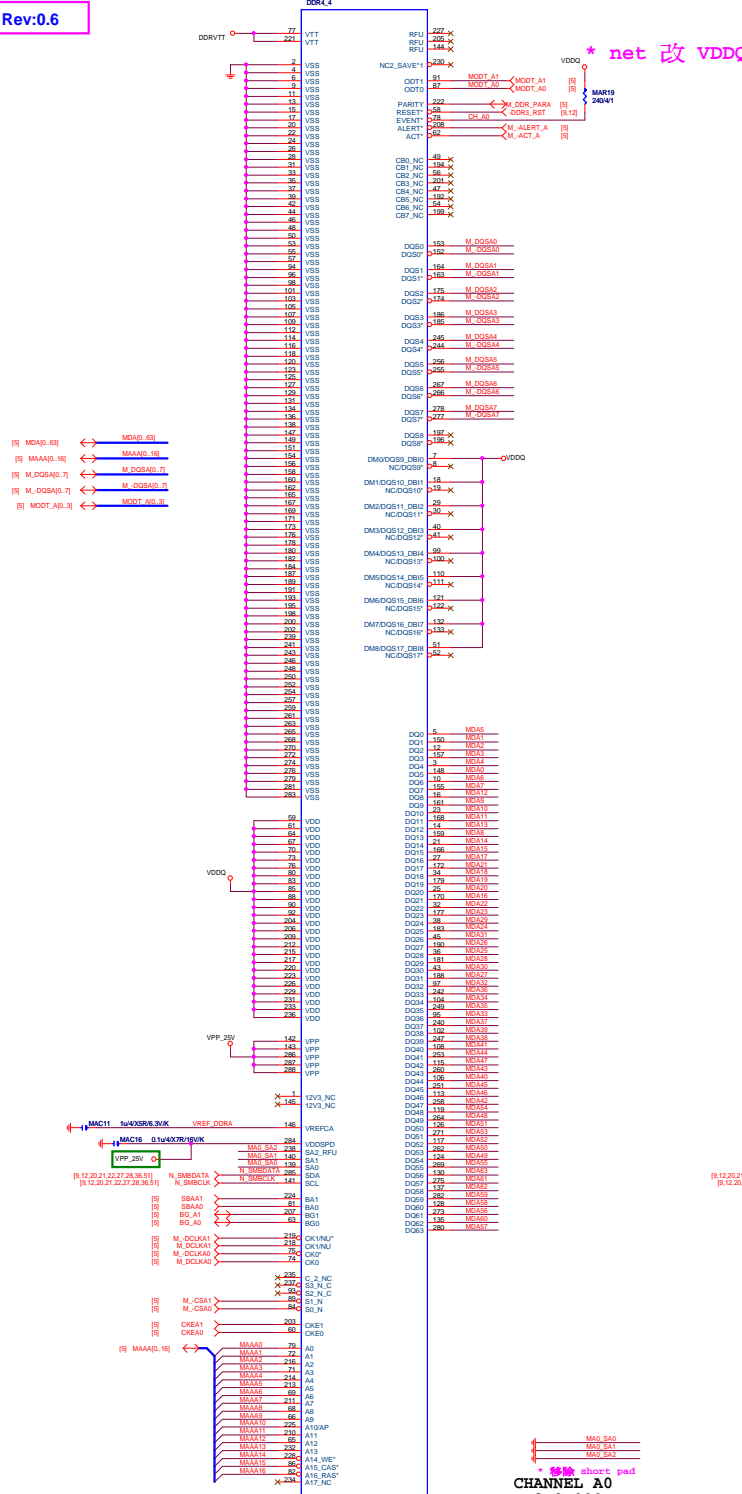
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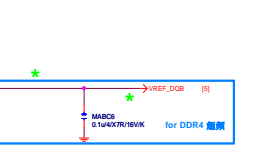
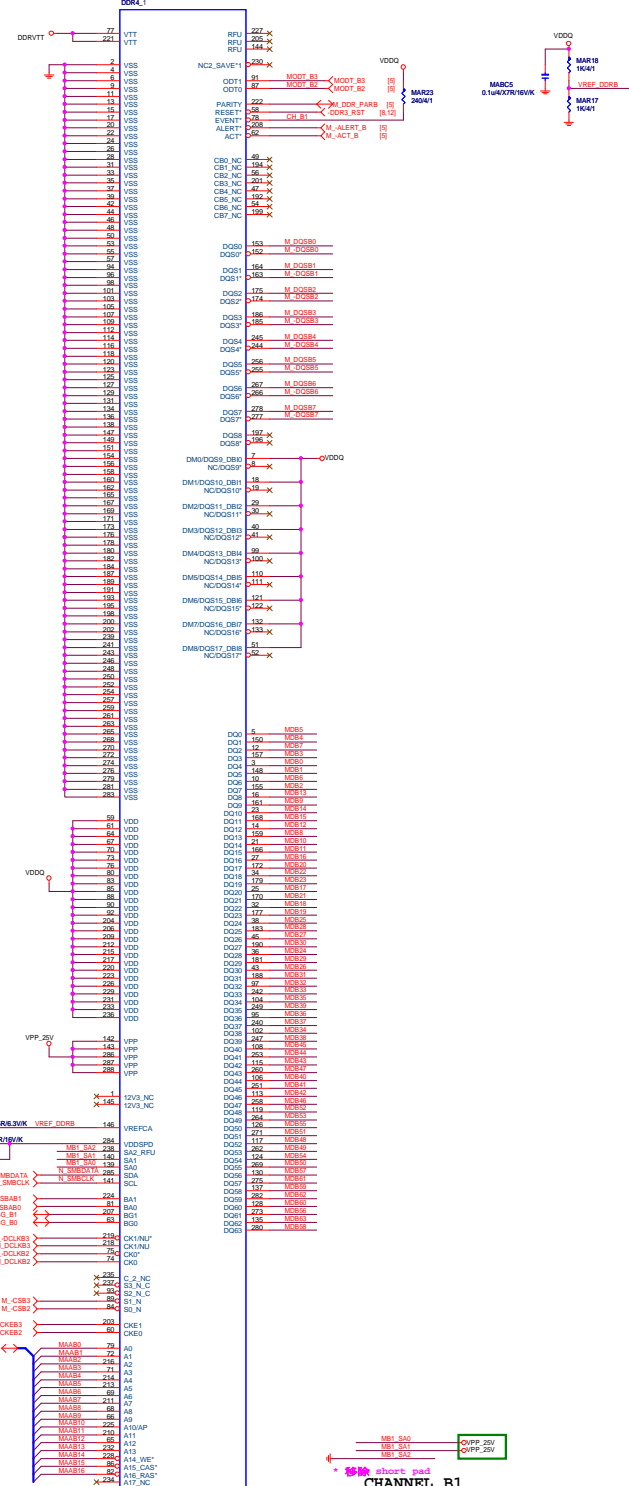
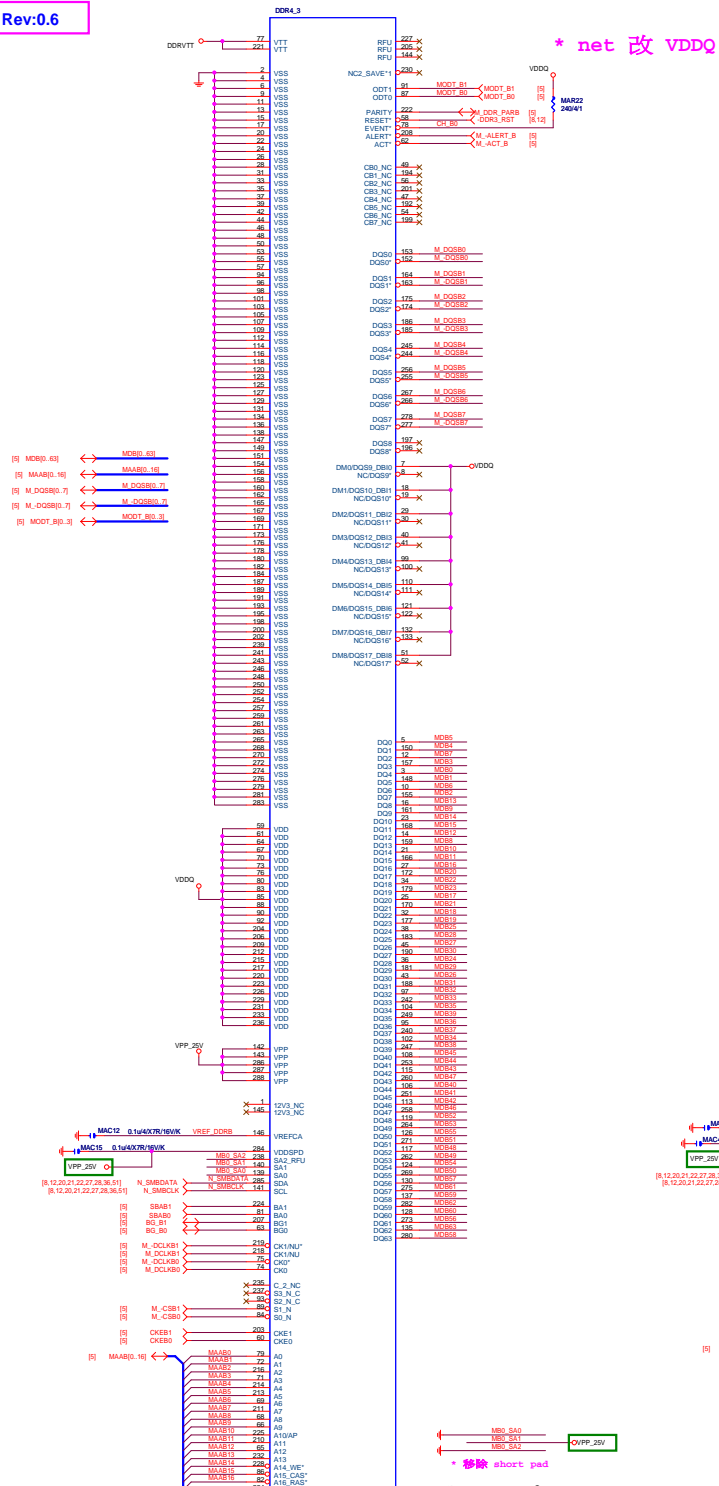
CPU-SK/1151/S/GF

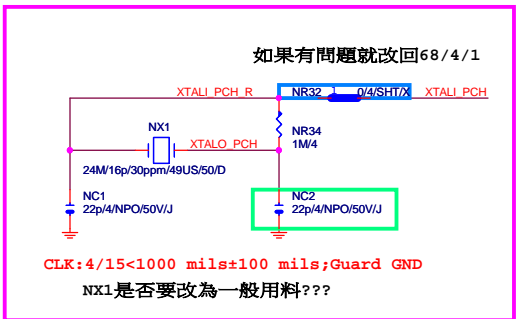
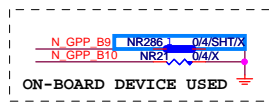
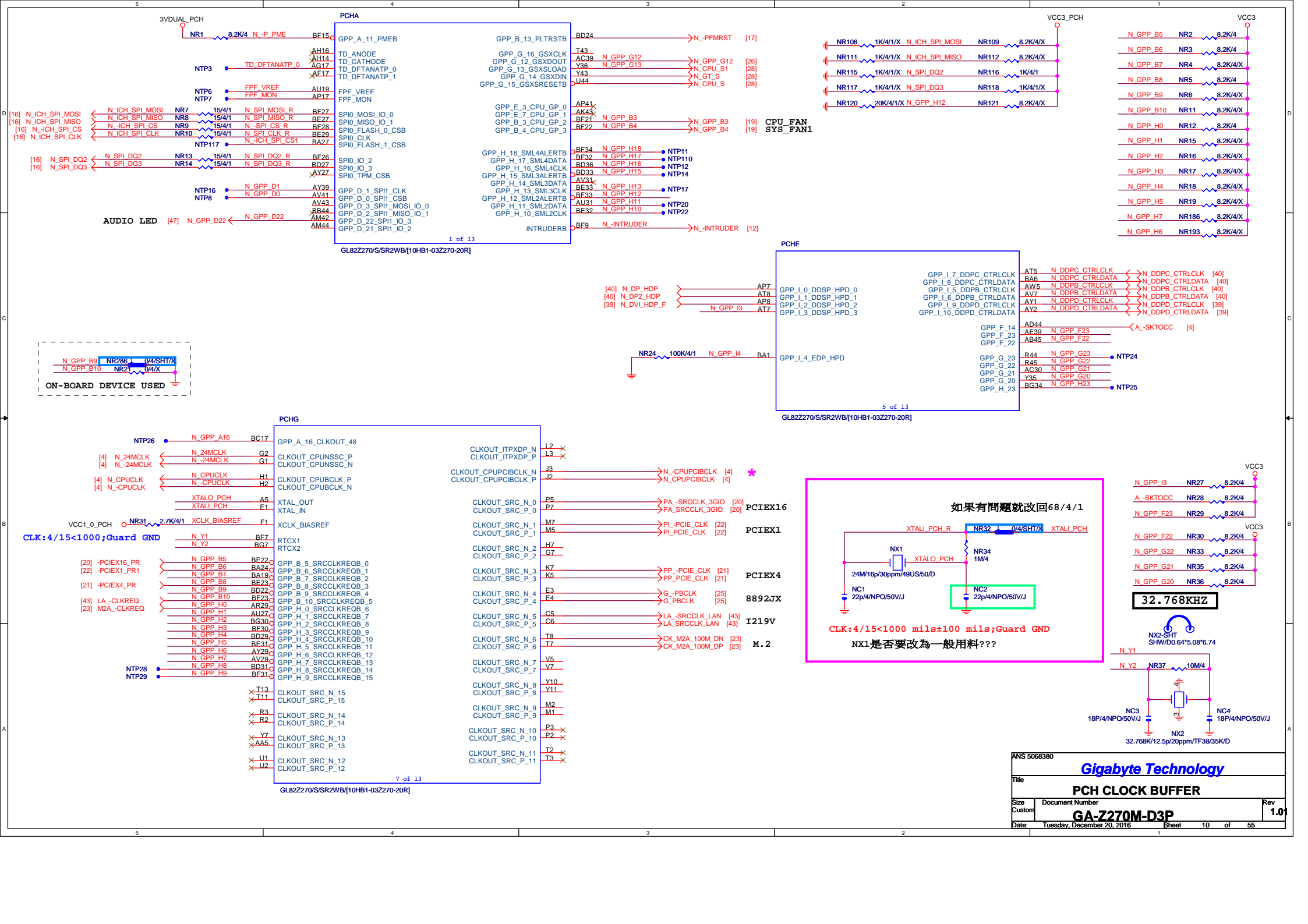


CPU-SK/1151/S/GF









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### Gigabyte Technology

**PCH CLOCK BUFFER**

Size: Custom    Document Number: **GA-Z270M-D3P**    Rev: **1.01**

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- [16] N\_ICH\_SPI\_MOSI
- [16] N\_ICH\_SPI\_MISO
- [16] N\_ICH\_SPI\_CS
- [16] N\_ICH\_SPI\_CLK

AUDIO LED [47] N\_GPP\_D22

CPU\_FAN SYS\_FAN1

- [40] N\_DP\_HDP
- [40] N\_DP2\_HDP
- [39] N\_DVI\_HDP\_F

PCHE

ON-BOARD DEVICE USED

PCHG

VCC1\_0\_PCH NR31 2.7K/4/1 XCLK\_BIASREF

CLK: 4/15 < 1000; Guard GND

- NTP26 N\_GPP A16 BC17
- [4] N\_24MCLK N\_24MCLK G2
- [4] N\_24MCLK N\_24MCLK G1
- [4] N\_CPUCCLK N\_CPUCCLK H1
- [4] N\_CPUCCLK N\_CPUCCLK H2
- XTALO\_PCH XTALO\_PCH A5
- XTALI\_PCH XTALI\_PCH E1
- VCC1\_0\_PCH NR31 2.7K/4/1 XCLK\_BIASREF F1
- N Y1 BE7
- N Y2 BG7
- [20] -PCIEX16\_PR N\_GPP B5 BE22
- [22] -PCIEX1\_PR1 N\_GPP B6 BA24
- [21] -PCIEX4\_PR N\_GPP B7 BA19
- [43] LA\_CLKREQ N\_GPP B8 BE23
- [23] M2A\_CLKREQ N\_GPP B9 BE22
- N\_GPP B10 BE23
- N\_GPP H0 AR29
- N\_GPP H1 AU27
- N\_GPP H2 BG30
- N\_GPP H3 BF30
- N\_GPP H4 BD29
- N\_GPP H5 BE31
- N\_GPP H6 AY29
- N\_GPP H7 AV29
- N\_GPP H8 BD31
- N\_GPP H9 BE31
- NTP28 N\_GPP H8 BD31
- NTP29 N\_GPP H9 BE31

GL82Z270/S/SR2WB(10HB1-03Z270-20R)

GL82Z270/S/SR2WB(10HB1-03Z270-20R)

PCIEX16

PCIEX1

PCIEX4

8892JX

I219V

M.2

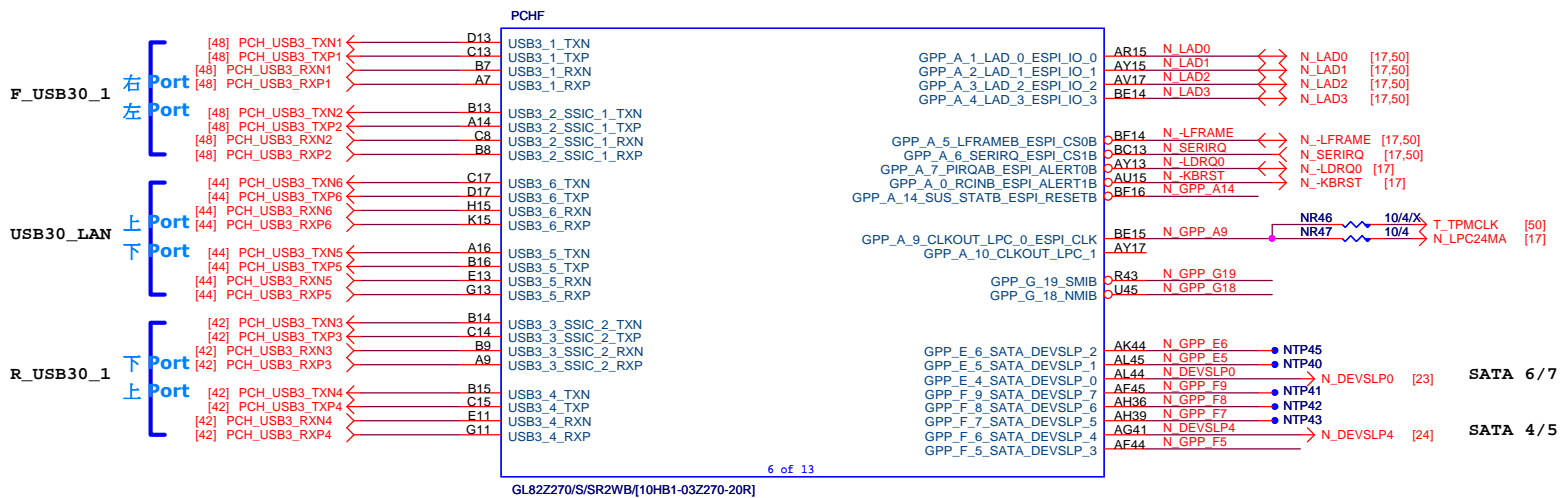
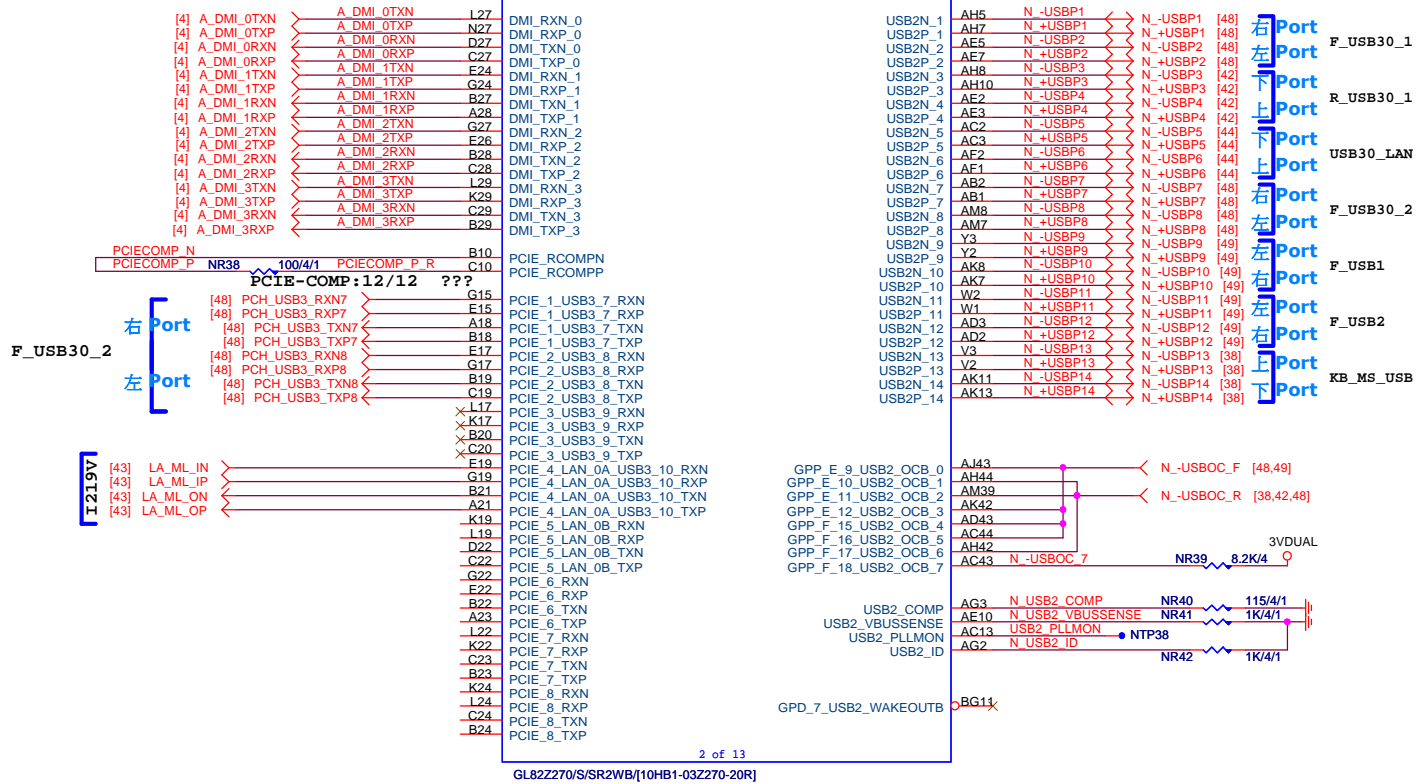
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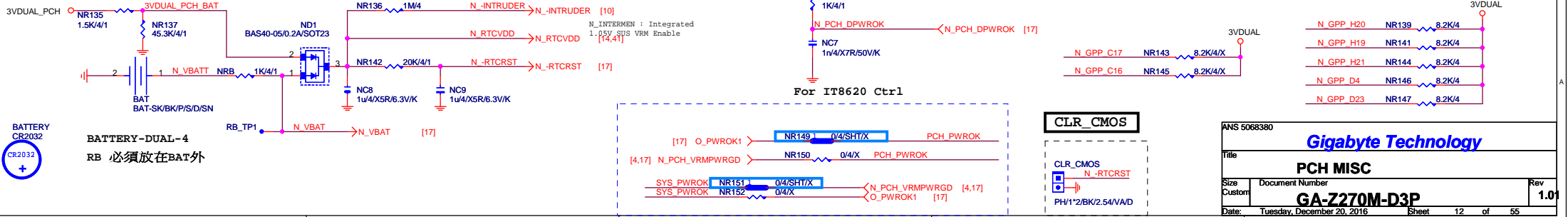
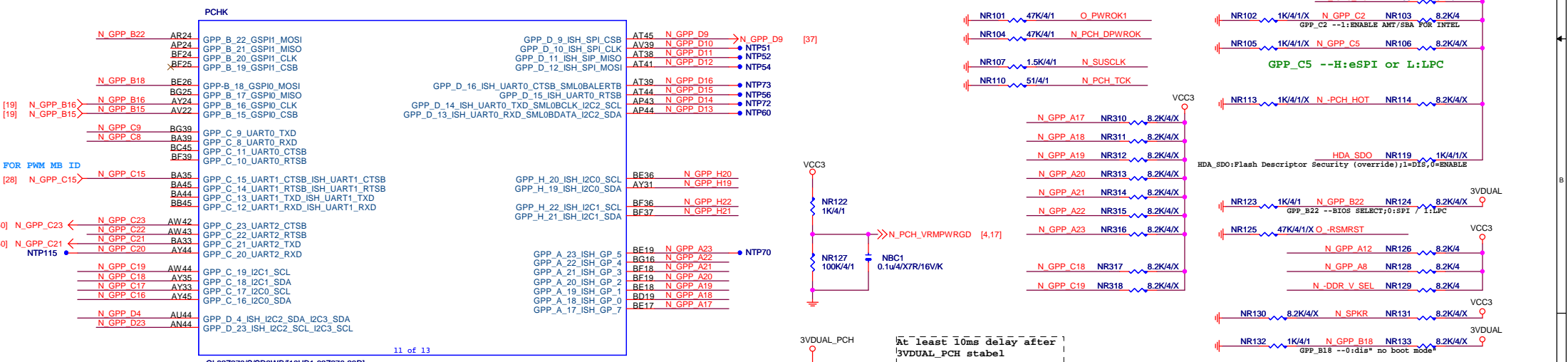
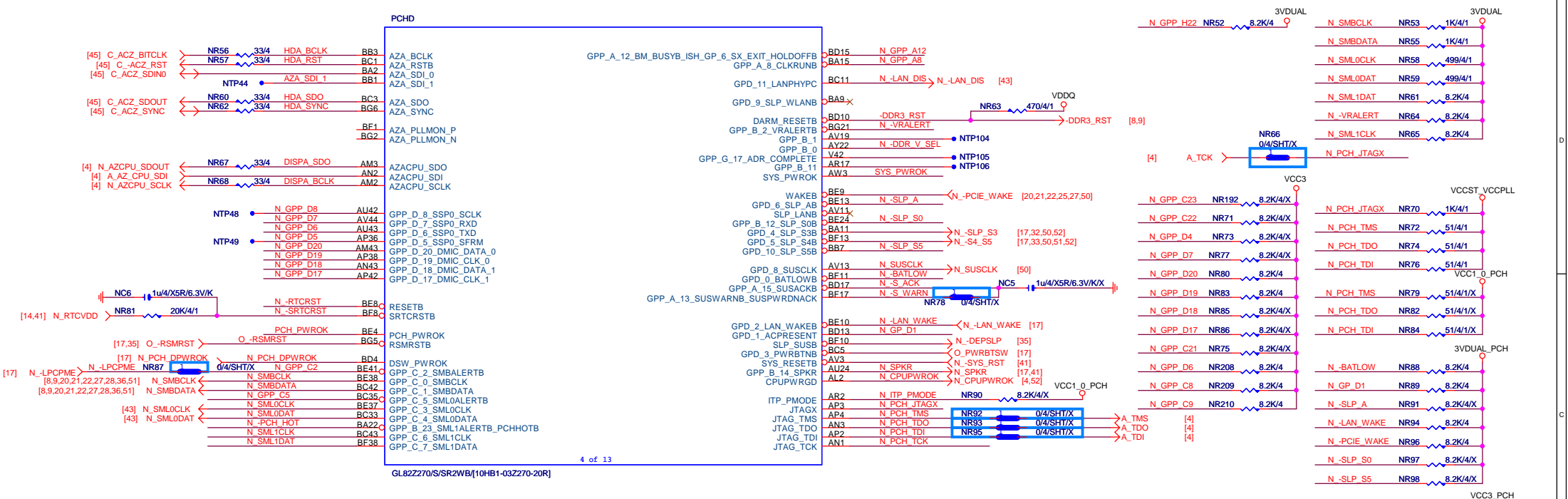
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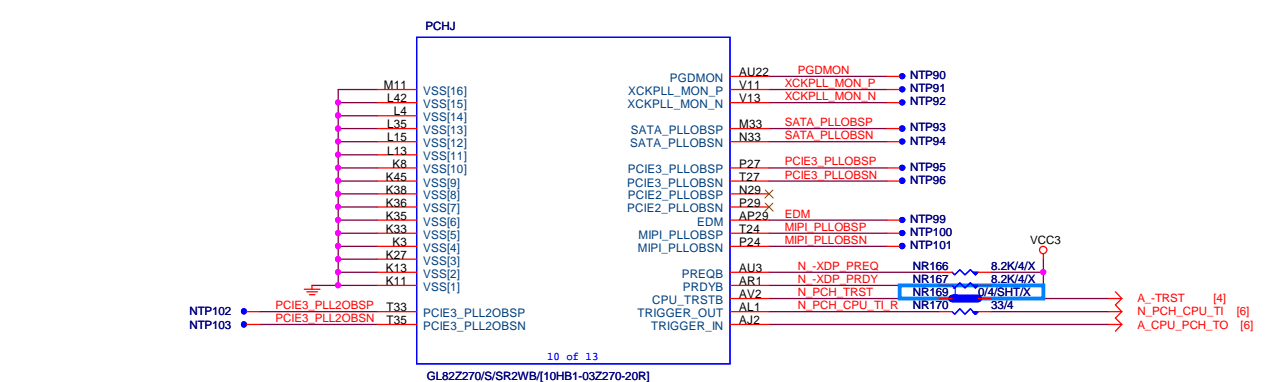
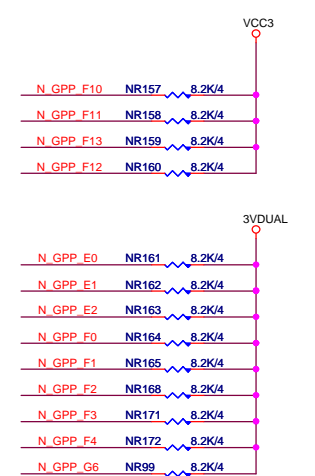
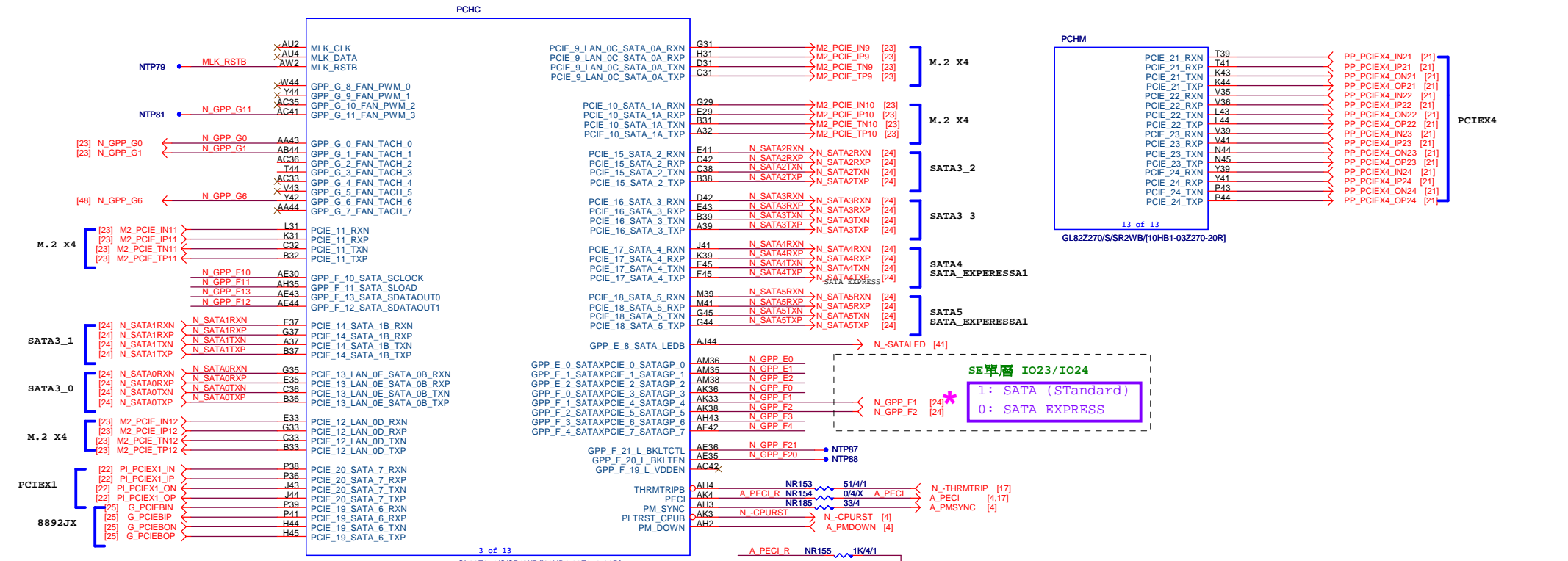
## PCH CLOCK BUFFER

Size: Custom    Document Number: **GA-Z270M-D3P**    Rev: **1.01**

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 [4] A\_HPRDY ← NR328 0/4/SHT/X N\_XDP\_PRDY

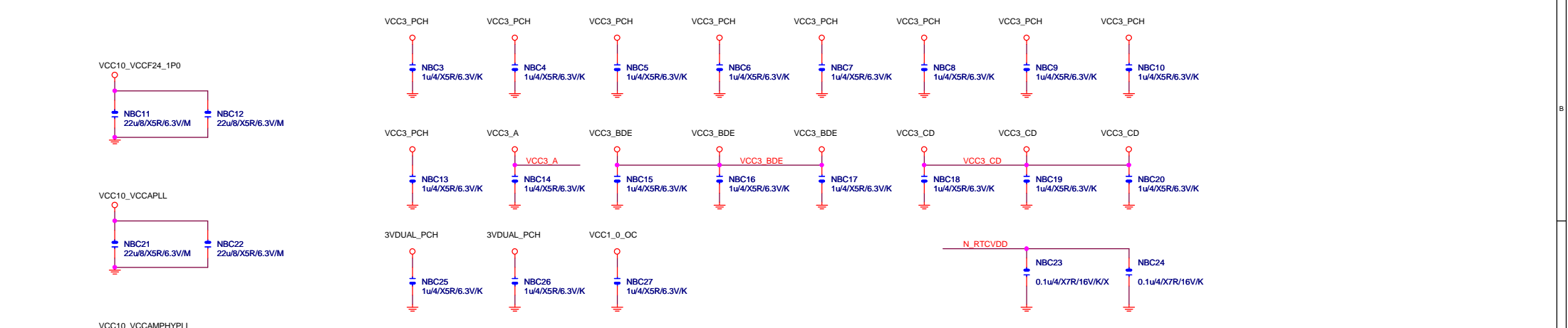
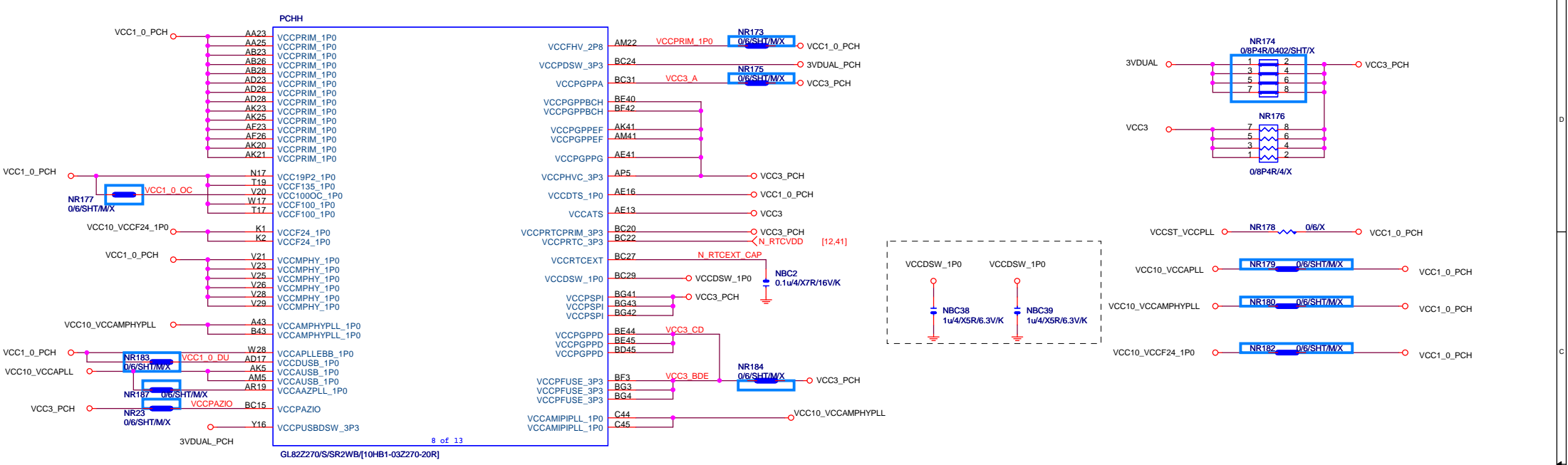
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**Gigabyte Technology**

Title: **PCH SATA,PCIe,SATA\_EXPRESS**

Size: Custom Document Number: **GA-Z270M-D3P** Rev: 1.01

Date: Tuesday, December 20, 2016 Sheet: 13 of 55



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<b>Gigabyte Technology</b>		
<b>PCH PWR</b>		
Size	Document Number	Rev
Custom	<b>GA-Z270M-D3P</b>	<b>1.01</b>
Date:	Tuesday, December 20, 2016	Sheet 14 of 55



PCHL		
A25	VSS	A42
A30	VSS	D45
P22	VSS	BG44
AV38	VSS	BF44
AV45	VSS	BF45
AV8	VSS	BF2
AY11	VSS	W29
AY19	VSS	A35
AY37	VSS	A40
AY4	VSS	A41
AY42	VSS	AA17
AY4L	VSS	AA18
B25	VSS	AA20
B3	VSS	AA21
B30	VSS	AA26
E35	VSS	AA28
B4	VSS	AA29
B41	VSS	AB17
BA13	VSS	AC32
A17	VSS	AE4
BA23	VSS	AE8
BA31	VSS	AF18
BA37	VSS	AF20
BA4	VSS	AF21
BA42	VSS	AF25
BB40	VSS	AF28
BC38	VSS	AF29
BC40	VSS	AF4
BC9	VSS	AF42
BD11	VSS	AG18
BD16	VSS	AG20
BD2	VSS	AG21
BD21	VSS	AG23
BD28	VSS	AG25
F2	VSS	AG26
E31	VSS	AG28
E6	VSS	AG29
F39	VSS	AH11
F43	VSS	AH13
G4	VSS	AH30
G40	VSS	AH32
G42	VSS	AH33
F6	VSS	AH38
G9	VSS	AJ1
H11	VSS	AJ17
H13	VSS	AJ18
H17	VSS	AJ20
H19	VSS	AJ21
H22	VSS	AJ23
H24	VSS	AJ25
H27	VSS	AJ26
H29	VSS	AJ28
H33	VSS	AJ29
H35	VSS	AJ45
H38	VSS	AK10
H4	VSS	AK14
H42	VSS	AK16
H9	VSS	AK17
J4	VSS	AK18
M35	VSS	AK26
M38	VSS	AK28
M4	VSS	AM14
M8	VSS	AN14
M9	VSS	AP19
N13	VSS	AR22
N15	VSS	AR27
N19	VSS	AU29
N22	VSS	AJ33
N24	VSS	AV1
N31	VSS	AV10
N42	VSS	AV15
P10	VSS	AV24
P12	VSS	AV27
AV35	VSS	AV33

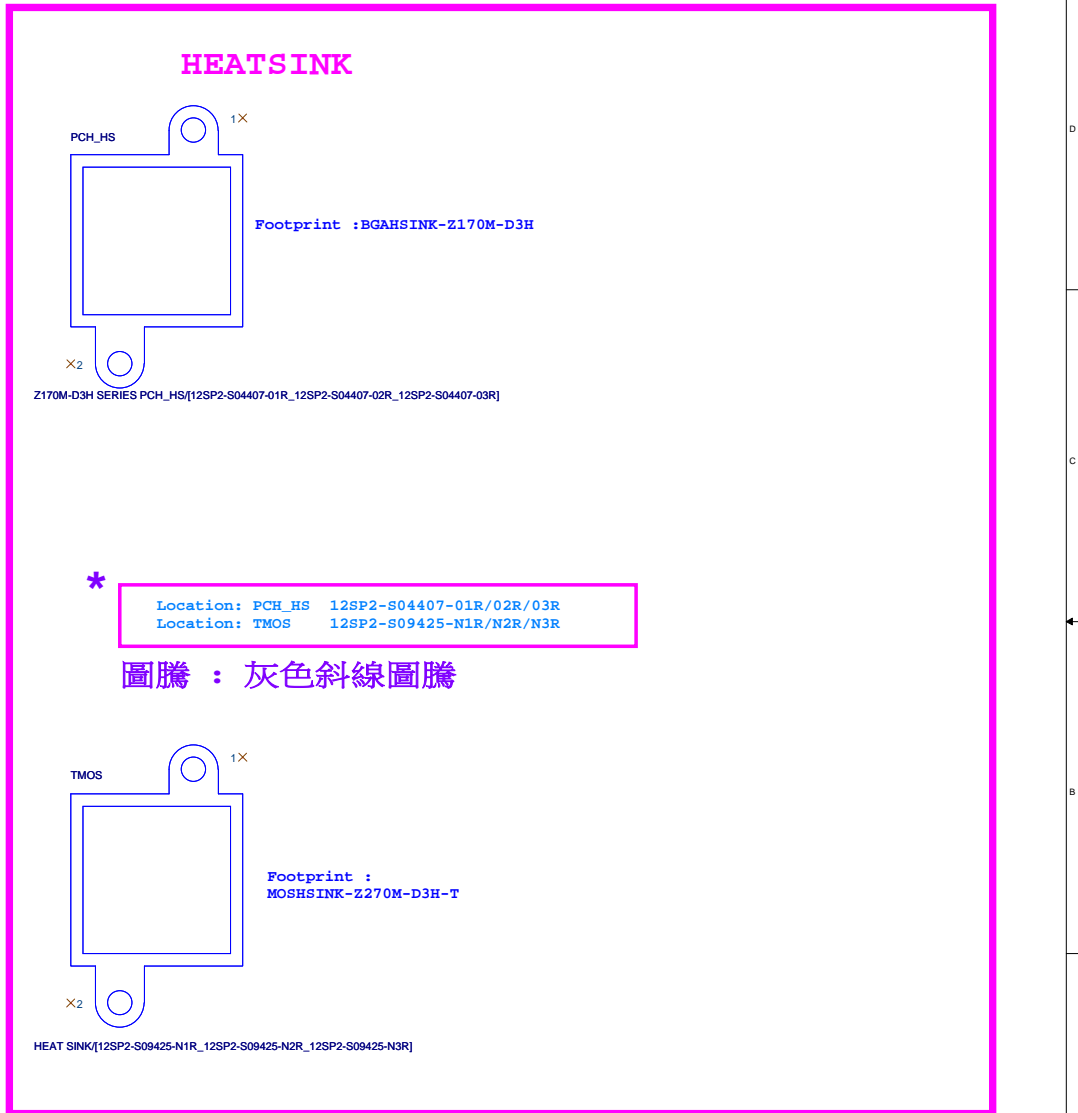
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GL82270/S/SR2WB[10HB1-032270-20R]

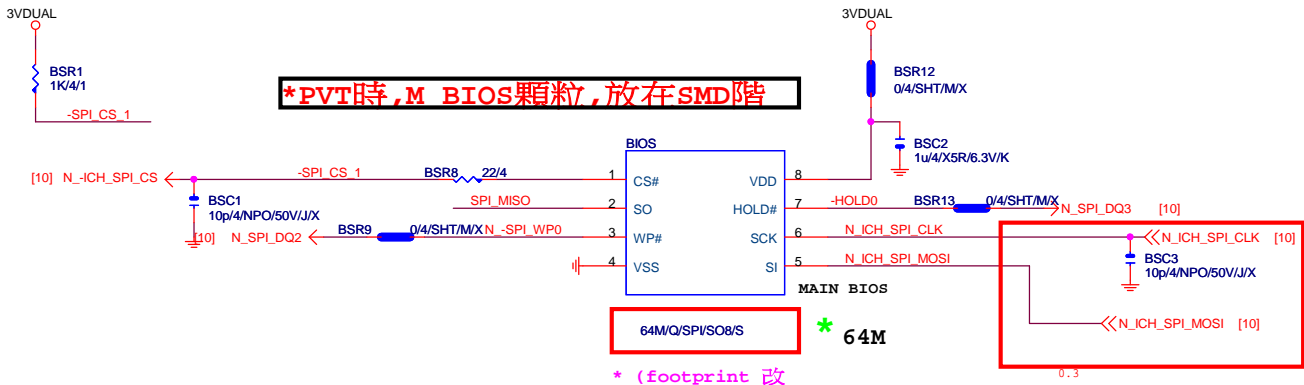
PCHL		
BD34	VSS[70]	VSS[11]
BD39	VSS[71]	AB18
BE2	VSS[72]	AB20
BF43	VSS[73]	AB21
BF5	VSS[75]	AB25
BG18	VSS[76]	AB29
BG23	VSS[77]	AB4
BG28	VSS[78]	AC10
BG32	VSS[79]	AC11
BG37	VSS[80]	AC14
BG40	VSS[81]	AC16
BG9	VSS[83]	AC4
C1	VSS[84]	AC5
A12	VSS[85]	AC7
AA28	VSS[86]	AC8
C37	VSS[87]	AD1
A6	VSS[88]	AD18
C9	VSS[89]	AD20
D1	VSS[90]	AD21
D10	VSS[91]	AD25
D12	VSS[92]	AD29
D15	VSS[93]	AD45
D16	VSS[94]	AE11
B12	VSS[95]	AE14
D19	VSS[96]	AE32
D21	VSS[97]	AE33
D24	VSS[98]	AE38
D25	VSS[99]	AK29
D29	VSS[100]	AK30
D30	VSS[101]	AK32
D33	VSS[102]	AK35
D35	VSS[103]	AK39
D36	VSS[104]	AL4
D39	VSS[105]	AL42
D44	VSS[106]	AM10
D7	VSS[107]	AM11
P13	VSS[108]	AM13
P15	VSS[109]	AM17
P17	VSS[110]	AM19
P19	VSS[111]	AM24
P31	VSS[112]	AM27
P32	VSS[113]	AM29
P35	VSS[114]	AM32
P4	VSS[115]	AM33
P42	VSS[116]	AM4
P8	VSS[117]	AN45
R1	VSS[118]	AP10
R32	VSS[119]	AP11
T10	VSS[120]	AP13
T14	VSS[121]	AP15
T22	VSS[122]	AP22
T29	VSS[123]	AP27
T32	VSS[124]	AP31
T36	VSS[125]	AP33
T38	VSS[126]	AP34
Y38	VSS[127]	AP39
Y4	VSS[128]	T4
Y8	VSS[129]	W26
T42	VSS[130]	V16
T5	VSS[131]	V17
U4	VSS[132]	V18
U42	VSS[133]	V30
V10	VSS[134]	V32
Y14	VSS[135]	V33
W3	VSS[136]	V38
AR22	VSS[137]	V4
W3	VSS[138]	V8
AR13	VSS[139]	W18
AR33	VSS[140]	W20
AR4	VSS[141]	W21
AT10	VSS[142]	W23
AT13	VSS[143]	W25
AT35	VSS[144]	A44
AT37	VSS[145]	BE1
AT42	VSS[146]	BD1
AU11	VSS[147]	B1
AU17	VSS[148]	A2
BD30	VSS[149]	B2
W45	VSS[150]	A3
Y13	VSS[151]	A4
Y14	VSS[152]	B44
Y30	VSS[153]	B45
Y32	VSS[154]	
Y33	VSS[155]	
Y34	VSS[156]	
Y35	VSS[157]	
Y36	VSS[158]	
Y37	VSS[159]	
Y38	VSS[160]	
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Y40	VSS[162]	
Y41	VSS[163]	
Y42	VSS[164]	
Y43	VSS[165]	
Y44	VSS[166]	
Y45	VSS[167]	
Y46	VSS[168]	
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Y77	VSS[199]	
Y78	VSS[200]	
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Y80	VSS[202]	
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Y82	VSS[204]	
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Y87	VSS[209]	
Y88	VSS[210]	
Y89	VSS[211]	
Y90	VSS[212]	
Y91	VSS[213]	
Y92	VSS[214]	
Y93	VSS[215]	
Y94	VSS[216]	
Y95	VSS[217]	
Y96	VSS[218]	
Y97	VSS[219]	
Y98	VSS[220]	
Y99	VSS[221]	
Y100	VSS[222]	

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GL82270/S/SR2WB[10HB1-032270-20R]



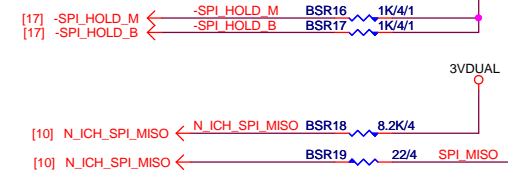
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<b>PCH GND</b>			
Size	Document Number	Rev	
Custom	<b>GA-Z270M-D3P</b>	<b>1.01</b>	
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**\*PVT時, M BIOS顆粒, 放在SMD階**

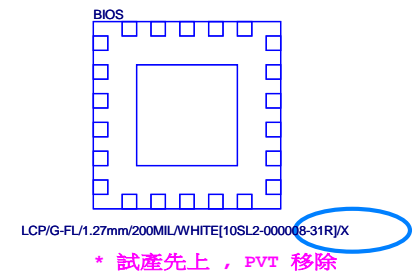
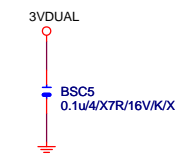
**64M/Q/SPV/SO8/S \* 64M**

*\* (footprint 改 SOIC8-SPI-SOCKET)  
\* (MP footprint 改 IC8-BIOS)*

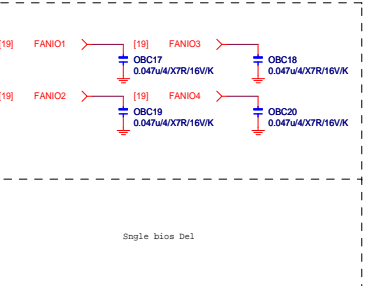
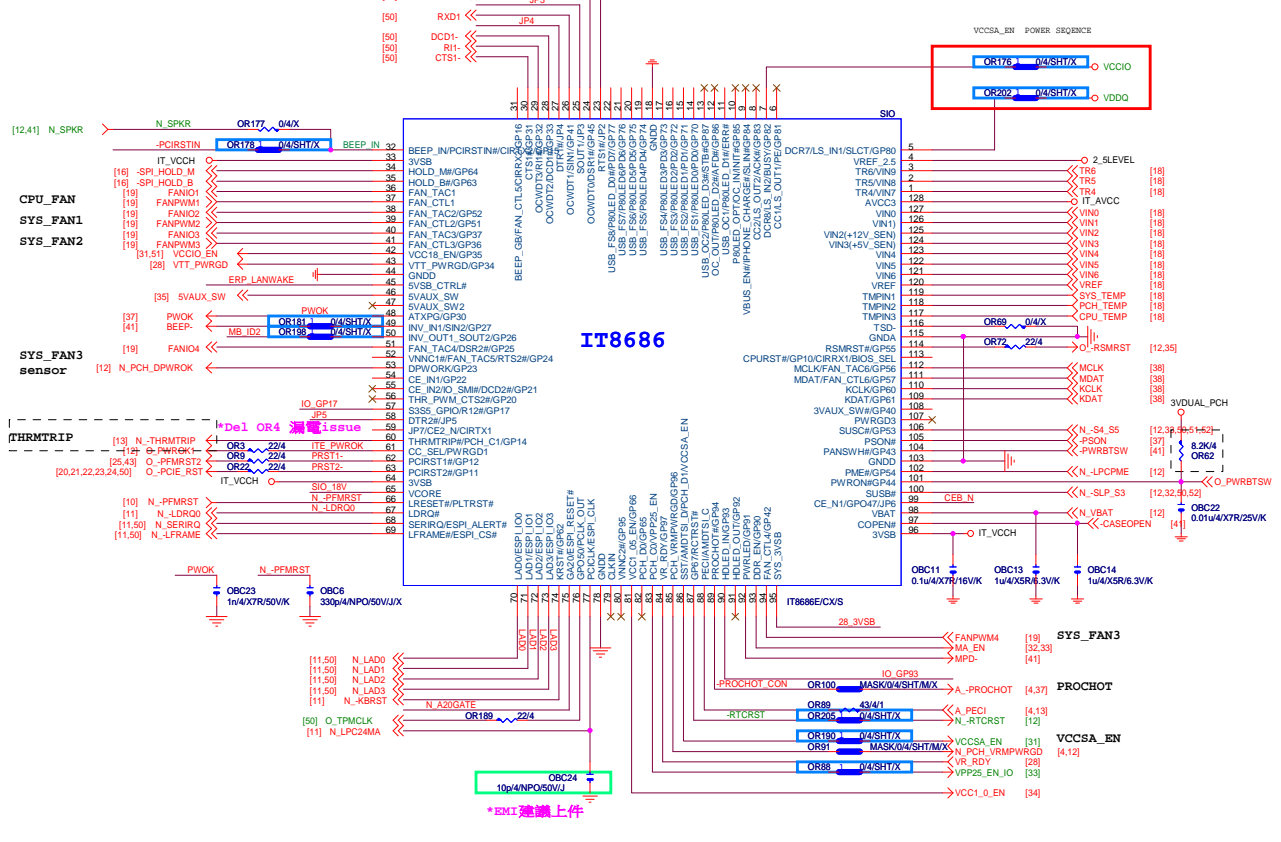


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

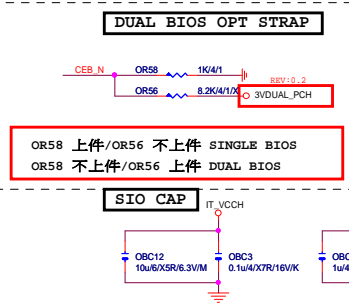
1 means floating  
0 means PD 1k



IT8686

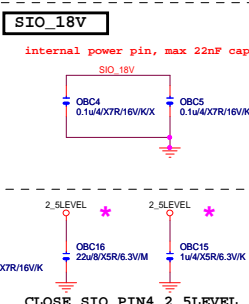


FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT FAN OR SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

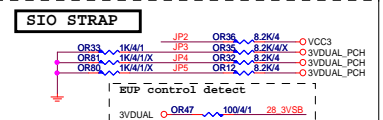
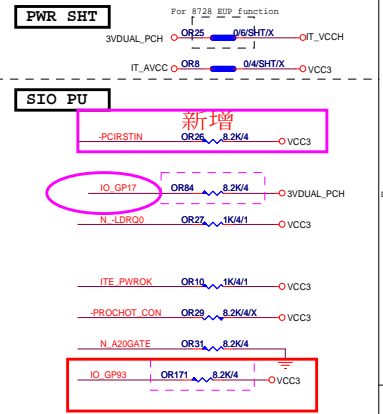
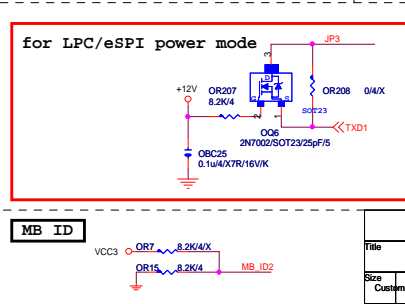


**Placement CPU**  
[4] A\_THRMTRIP ← WR10\_1K/41 N\_THRMTRIP

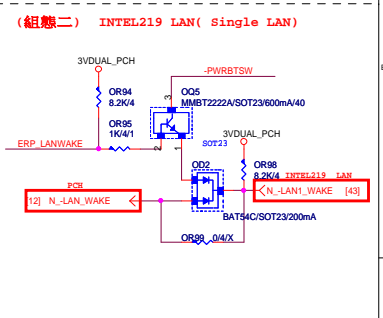
CPU 端 A\_THRMTRIP不可與PCH及SIO N\_THRMTRIP直接連接。否則會出現無法拉低情況。



ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN (只留一個 LAN 支援 ERP 下 WAKE UP)	Intel 219	組態一
	Atheros+Atheros	組態二
	Intel 219+Atheros	組態三
No Support ERP	Single LAN BOM 只上 OR97。 Dual LAN BOM 只上 OR97、OR99。	



JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7	1	Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 0	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3



for LPC/esPI power mode

**Gigabyte Technology**

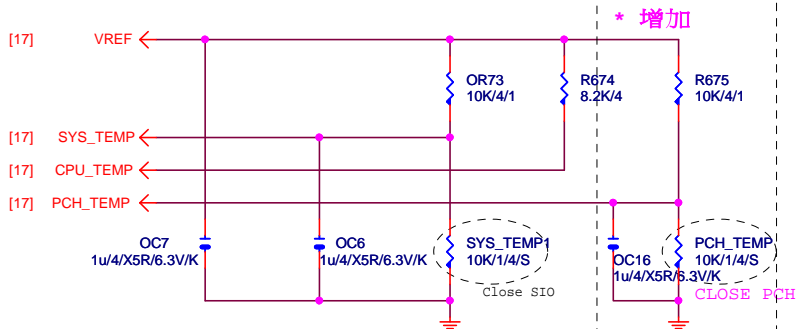
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Size: Document Number: GA-Z270M-D3P

Customer: Rev: 1.01

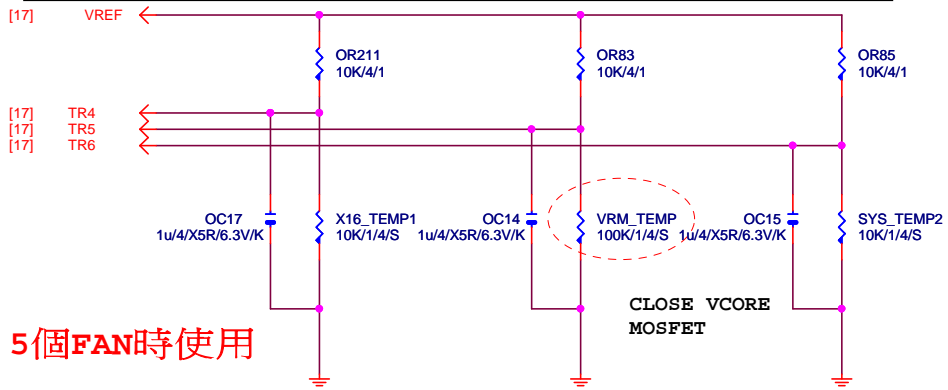
Date: Monday, December 19, 2016 Sheet: 17 of 55

**TEMP H/W MONITOR**



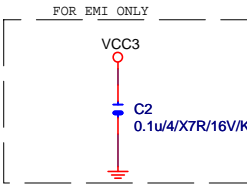
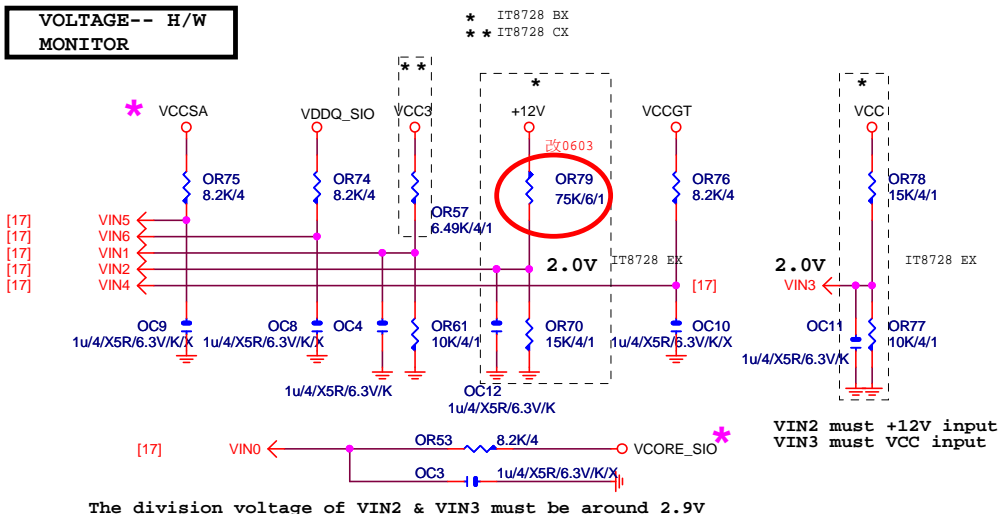
**RS VCORE、RS VCCGT、CLOSE CPU VCORE & VCCGT MOSFET**

-PROCHOT:有mos heatsink不用prochot function

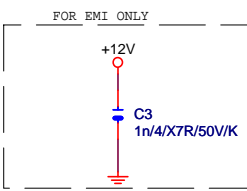


5個FAN時使用

**VOLTAGE-- H/W MONITOR**

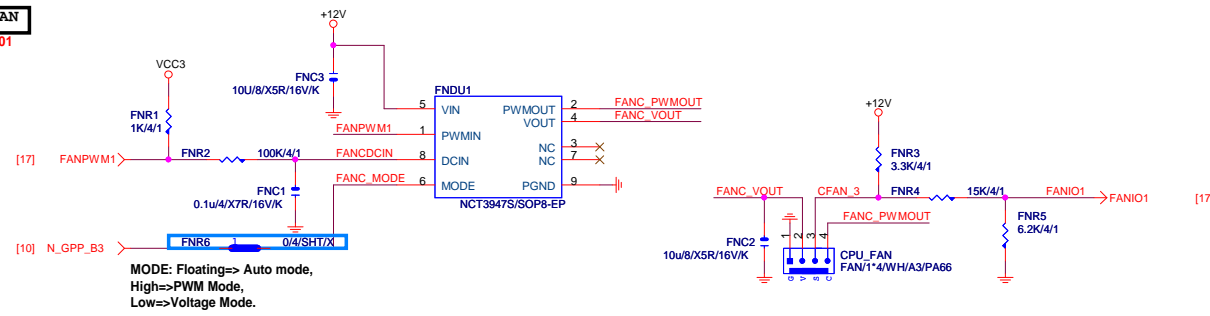


★Update 2015-04.24

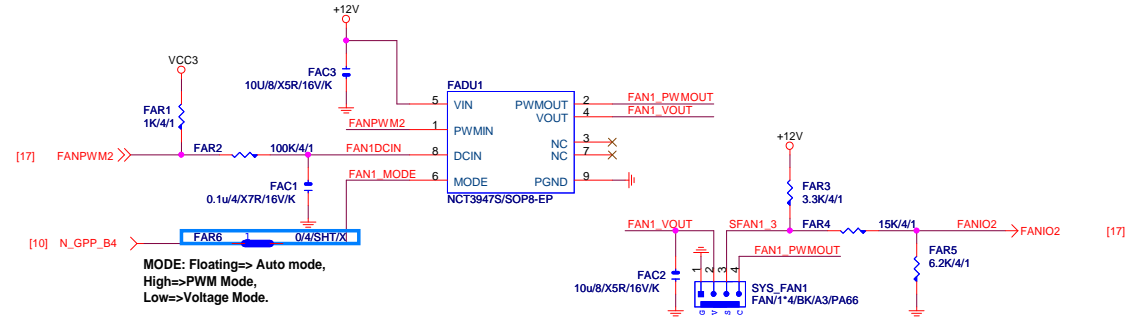


**Gigabyte Technology**

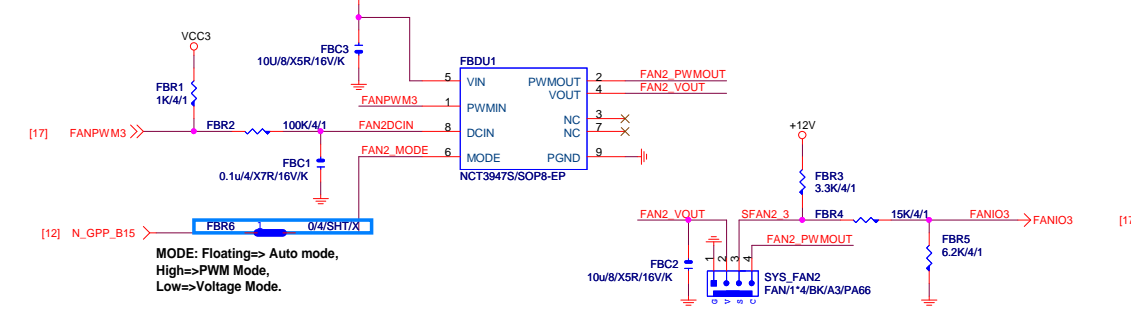
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HWM,KB/MS, FAN CTRL		
Size	Document Number	Rev
Custom	<b>GA-Z270M-D3P</b>	<b>1.01</b>
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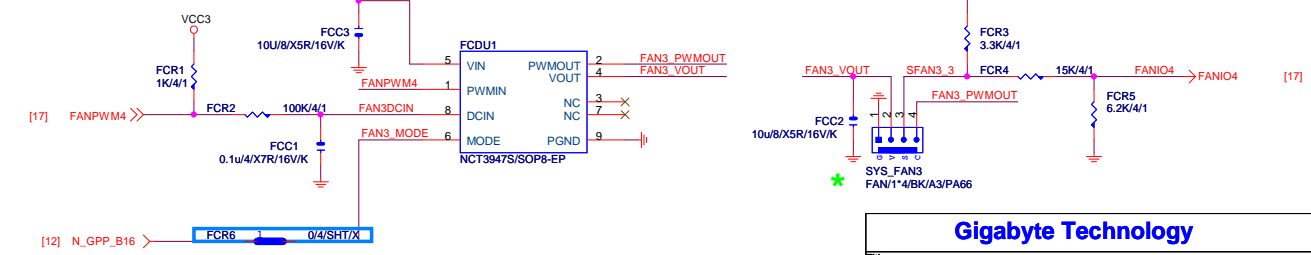
SYSTEM FAN1



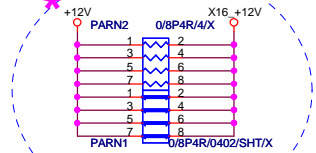
SYSTEM FAN2



SYSTEM FAN3



+12\_protect  
short-wire test



[8,9,12,21,22,27,28,36,51] N\_SMBCLK  
[8,9,12,21,22,27,28,36,51] N\_SMBDATA

[12,21,22,25,27,50] N\_-PCIE\_WAKE

[10] -PCIE16\_PR

PA\_EXP\_RXP[0..15] >>> PA\_EXP\_RXP[0..15] [4]  
PA\_EXP\_RXN[0..15] >>> PA\_EXP\_RXN[0..15] [4]  
PA\_EXP\_TXP[0..15] >>> PA\_EXP\_TXP[0..15] [4]  
PA\_EXP\_TXN[0..15] >>> PA\_EXP\_TXN[0..15] [4]

PA_EXP_TXP0	PAC5	0.22u4/X5R6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u4/X5R6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u4/X5R6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u4/X5R6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u4/X5R6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u4/X5R6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u4/X5R6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u4/X5R6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u4/X5R6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u4/X5R6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u4/X5R6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u4/X5R6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u4/X5R6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u4/X5R6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u4/X5R6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u4/X5R6.3V/K	PA_EXP_TXN7_C
PA_EXP_TXP8	PAC21	0.22u4/X5R6.3V/K	PA_EXP_TXP8_C
PA_EXP_TXN8	PAC20	0.22u4/X5R6.3V/K	PA_EXP_TXN8_C
PA_EXP_TXP9	PAC22	0.22u4/X5R6.3V/K	PA_EXP_TXP9_C
PA_EXP_TXN9	PAC23	0.22u4/X5R6.3V/K	PA_EXP_TXN9_C
PA_EXP_TXP10	PAC24	0.22u4/X5R6.3V/K	PA_EXP_TXP10_C
PA_EXP_TXN10	PAC25	0.22u4/X5R6.3V/K	PA_EXP_TXN10_C
PA_EXP_TXP11	PAC26	0.22u4/X5R6.3V/K	PA_EXP_TXP11_C
PA_EXP_TXN11	PAC27	0.22u4/X5R6.3V/K	PA_EXP_TXN11_C
PA_EXP_TXP12	PAC28	0.22u4/X5R6.3V/K	PA_EXP_TXP12_C
PA_EXP_TXN12	PAC29	0.22u4/X5R6.3V/K	PA_EXP_TXN12_C
PA_EXP_TXP13	PAC31	0.22u4/X5R6.3V/K	PA_EXP_TXP13_C
PA_EXP_TXN13	PAC30	0.22u4/X5R6.3V/K	PA_EXP_TXN13_C
PA_EXP_TXP14	PAC32	0.22u4/X5R6.3V/K	PA_EXP_TXP14_C
PA_EXP_TXN14	PAC33	0.22u4/X5R6.3V/K	PA_EXP_TXN14_C
PA_EXP_TXP15	PAC34	0.22u4/X5R6.3V/K	PA_EXP_TXP15_C
PA_EXP_TXN15	PAC35	0.22u4/X5R6.3V/K	PA_EXP_TXN15_C

PCIEX16:16/5/5/16

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

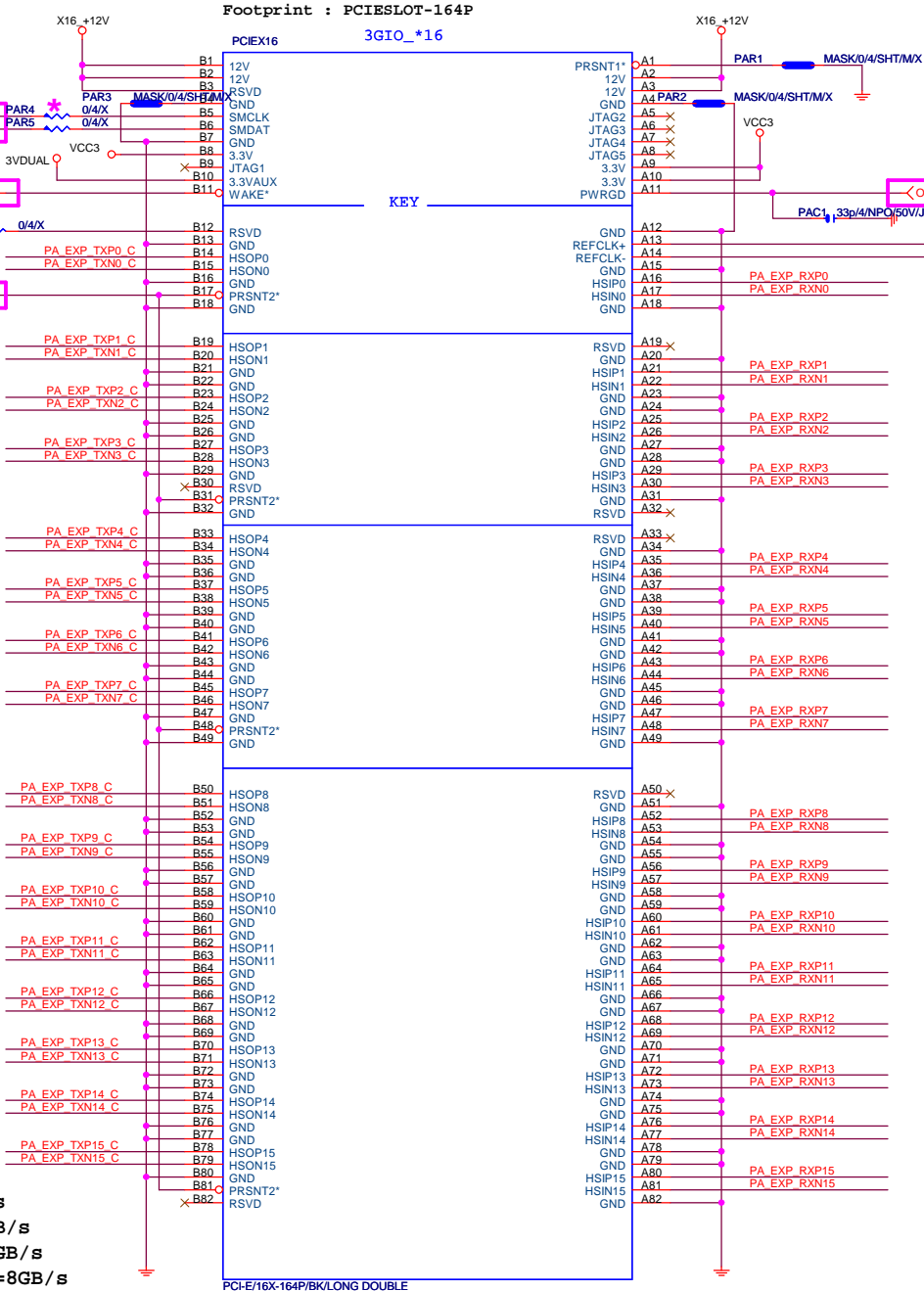
PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCE-E X1(單向) BANDWIDTH=5GHz\*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--> 8GHZ

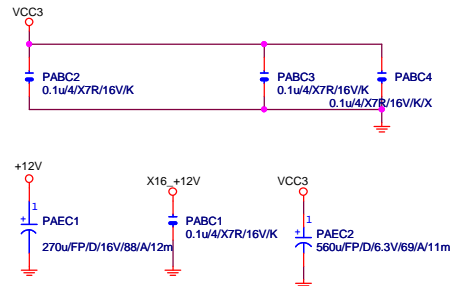
PCE-E X1(單向) BANDWIDTH=8GHz\*(128b/130b)=8Gb/s=1GB/s



PCI-E16X-164P/BK/LONG DOUBLE

BACK

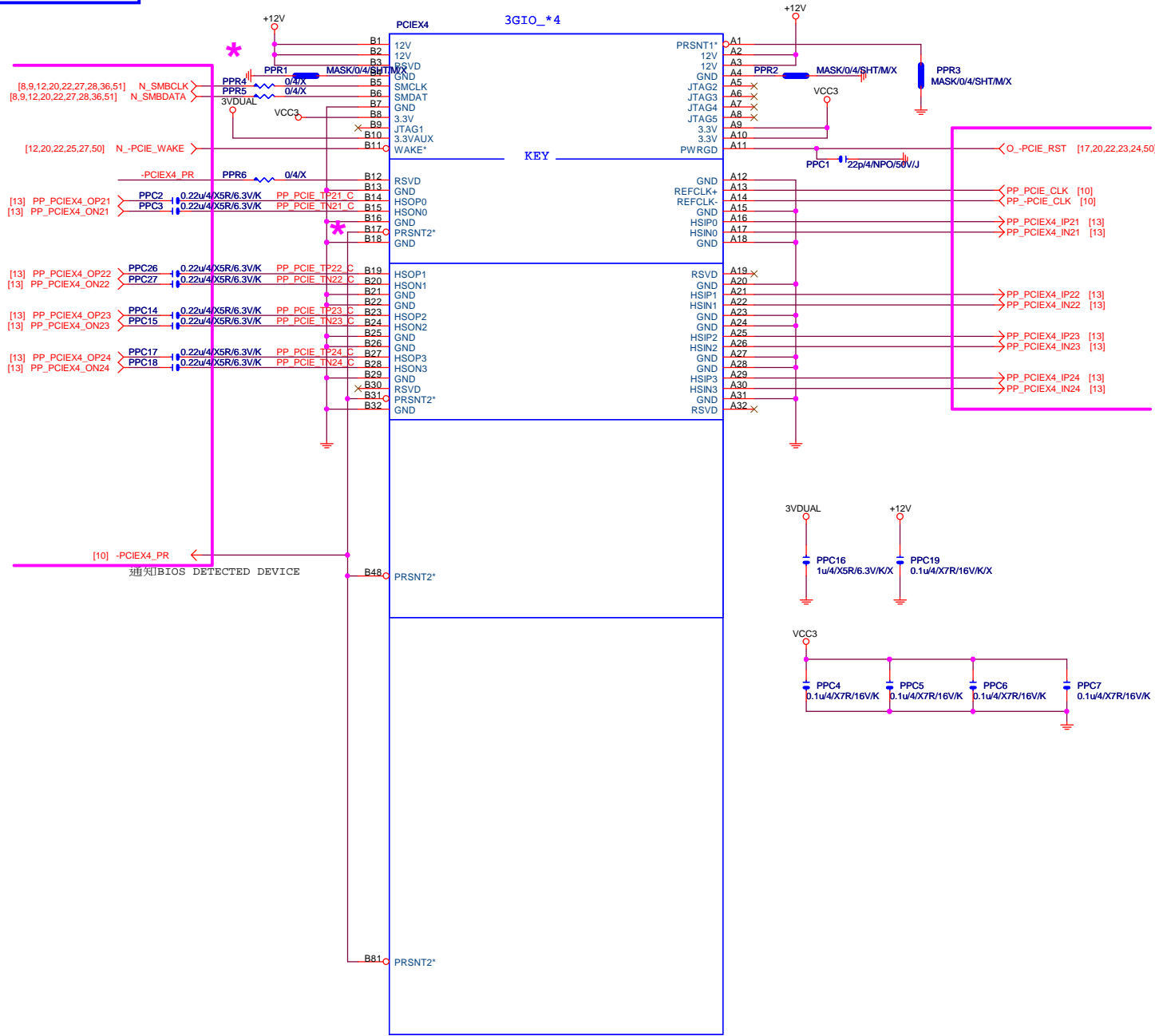
\* 黑色



\*改台系固態電容

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Size Custom: Document Number: GA-Z270M-D3P Rev: 1.01  
Date: Monday, December 19, 2016 Sheet: 20 of 55





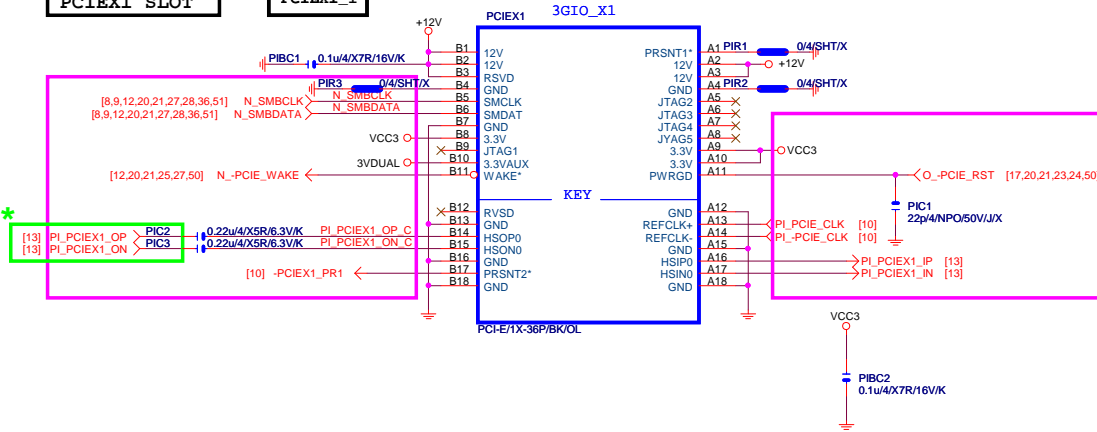
PCI-E/4X-66P/BK/LONG DOUBLE  
BACK

\* 黑色

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<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
Custom	<b>GA-Z270M-D3P</b>	1.01
<b>Date:</b> Monday, December 19, 2016	<b>Sheet</b> 21	<b>of</b> 55

PCIEX1 SLOT

PCIEX1\_1



1個x1 ,不用SWITCH

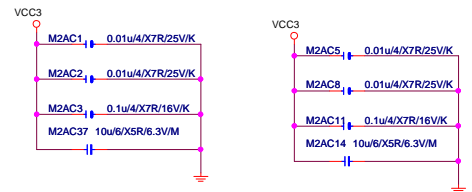
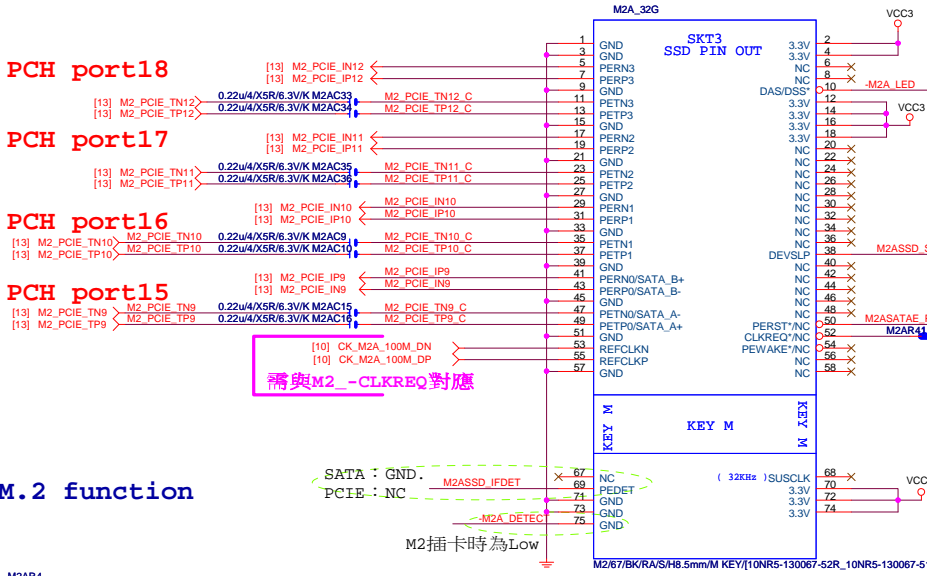
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<b>PCIEX1</b>		
Size	Document Number	Rev
Custom	<b>GA-Z270M-D3P</b>	<b>1.01</b>
Date:	Monday, December 19, 2016	Sheet 22 of 55

M.2 Lane4 from PCH port18

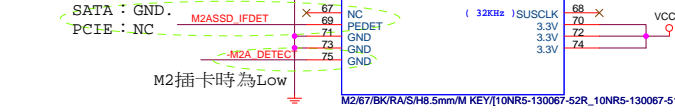
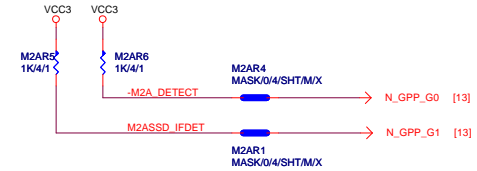
M.2 Lane3 from PCH port17

M.2 Lane2 from PCH port16

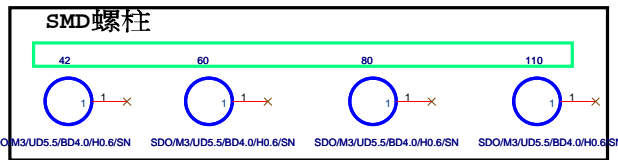
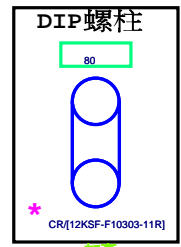
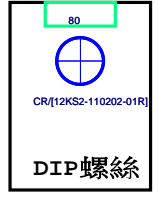
M.2 Lane1 from PCH port15



支援SATA and M.2 function

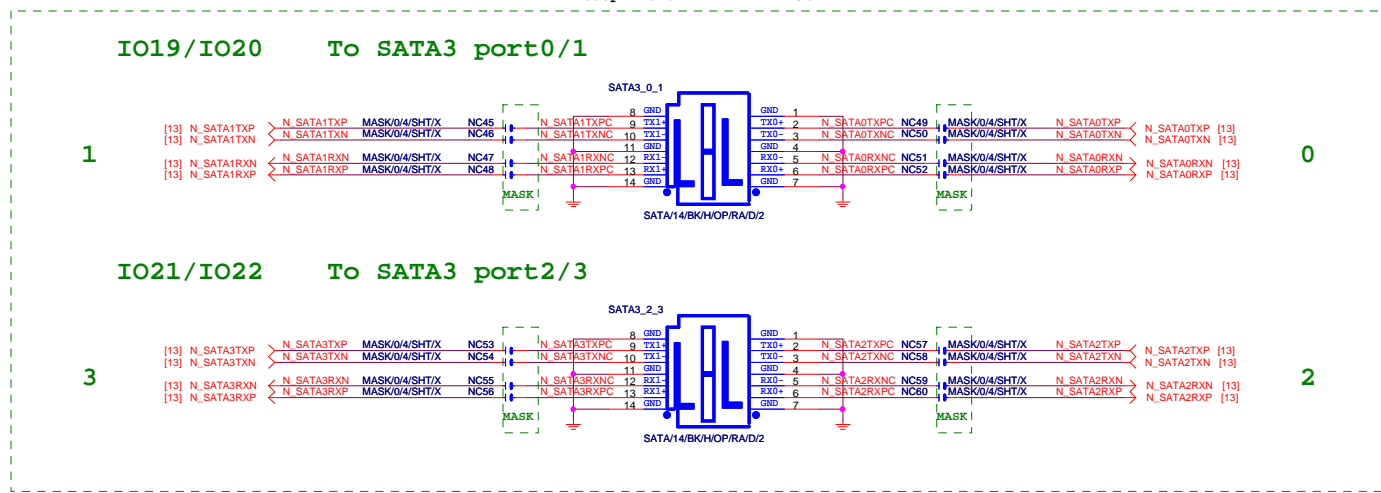
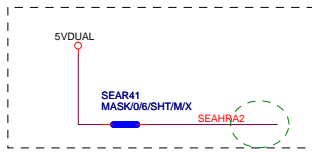


\* Footprint : NGFF-M-75P-11CM-3-SMD



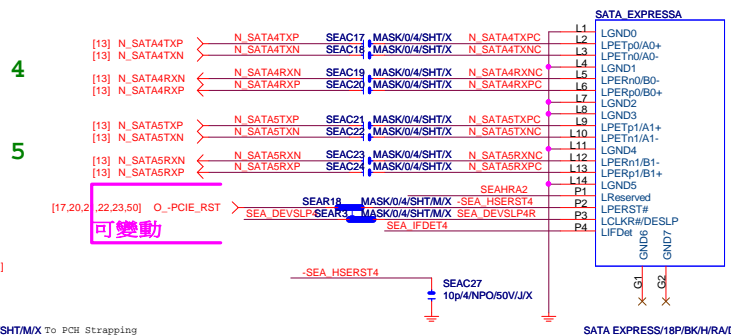
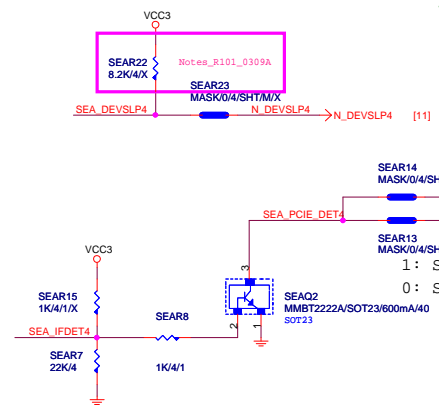
\* Footprint : HOLE\_C236D165-A

M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)		PCIE x4 (For M.2)			SATA	SATA
		SATA Express (Low)		PCIE x4 (For M.2)			SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)		PCIE x4			SATA	SATA
		SATA Express (Low)		PCIE x4			SATA Express	



SATA EXPRESS新增power for USB3.1小卡  
每個CONNECT都要留一顆0603 0 OHM,走線40MILS 即可

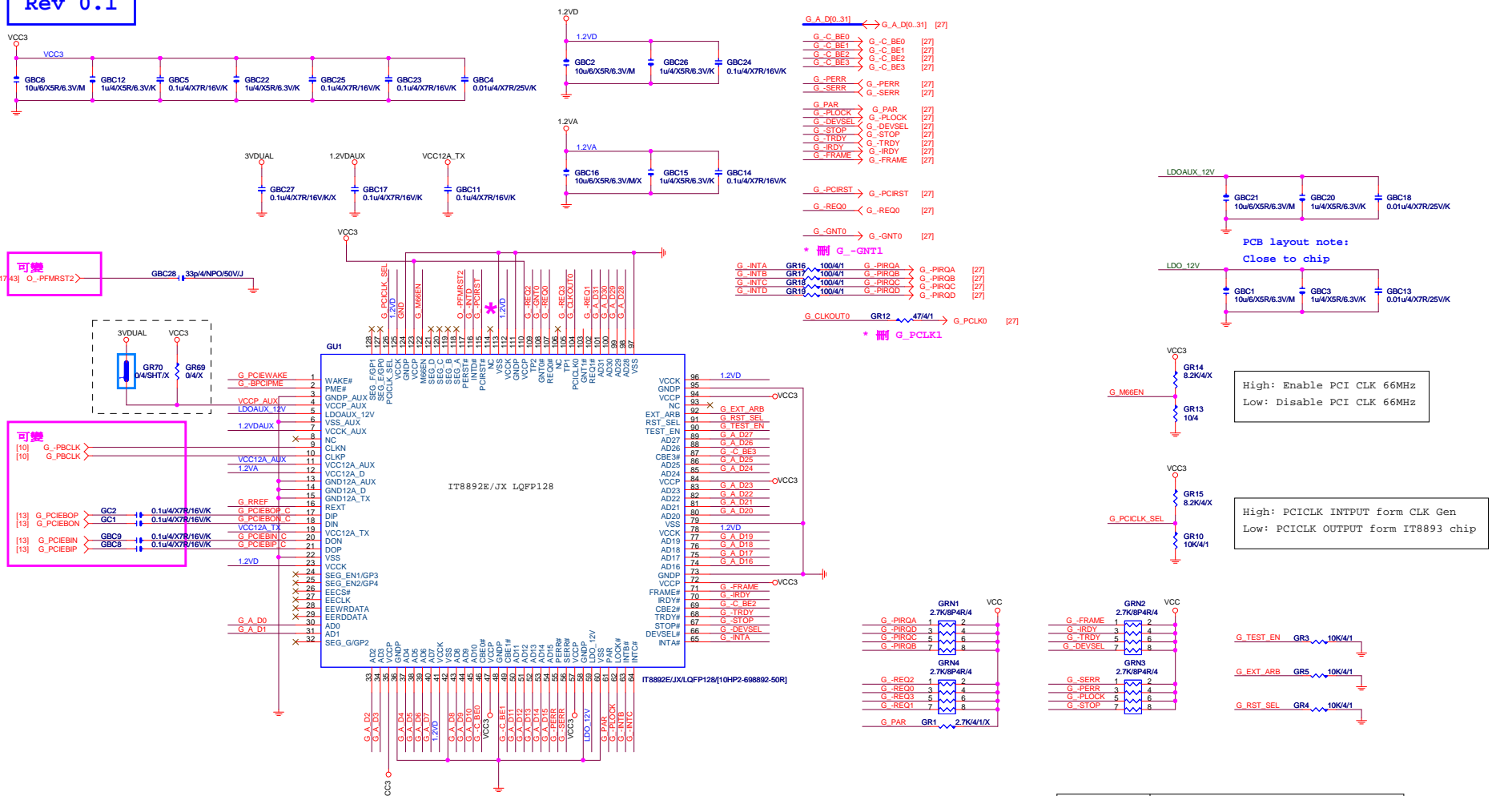
單層 IO23/IO24 To SATA3 [port4/5]



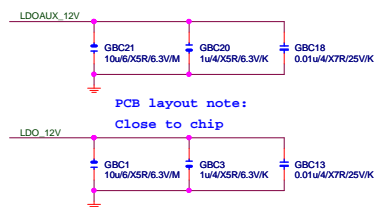
SATA 5 (文字面寫SATA 1)  
SATA 4 (文字面寫SATA 0)  
SATA 3  
SATA 2  
SATA 1 (文字面寫SATA 5)  
SATA 0 (文字面寫SATA 4)

SATA EXPRESS 訊號 SATA EXPRESS 文字面

SATA 1	SATA 3
SATA 0	SATA 2
SATA 5	SATA 4



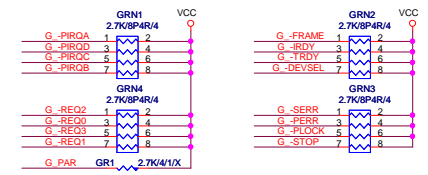
- G\_A\_D0[0..31] ← G\_A\_D0[0..31] [27]
- G\_C\_BE0 → G\_C\_BE0 [27]
- G\_C\_BE1 → G\_C\_BE1 [27]
- G\_C\_BE2 → G\_C\_BE2 [27]
- G\_C\_BE3 → G\_C\_BE3 [27]
- G\_PERR → G\_PERR [27]
- G\_SERR → G\_SERR [27]
- G\_PAR → G\_PAR [27]
- G\_PLOCK → G\_PLOCK [27]
- G\_DEVSEL → G\_DEVSEL [27]
- G\_STOP → G\_STOP [27]
- G\_TRDY → G\_TRDY [27]
- G\_IRDY → G\_IRDY [27]
- G\_FRAME → G\_FRAME [27]
- G\_PCI\_RST → G\_PCI\_RST [27]
- G\_REQ0 → G\_REQ0 [27]
- G\_GNT0 → G\_GNT0 [27]
- \* 刪 G\_GNT1
- G\_INTA GR16 100K/41 → G\_PIRQA → G\_PIRQA [27]
- G\_INTB GR17 100K/41 → G\_PIRQB → G\_PIRQB [27]
- G\_INTC GR18 100K/41 → G\_PIRQC → G\_PIRQC [27]
- G\_INTD GR19 100K/41 → G\_PIRQD → G\_PIRQD [27]
- G\_CLKOUT0 GR12 47K/41 → G\_PCLK0 [27]
- \* 刪 G\_PCLK1



PCB layout note:  
Close to chip

High: Enable PCI CLK 66MHz  
Low: Disable PCI CLK 66MHz

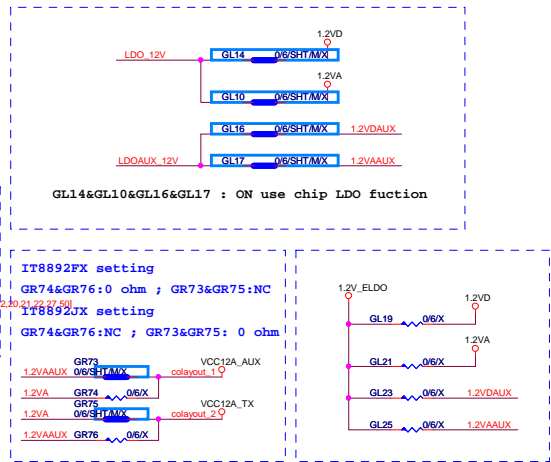
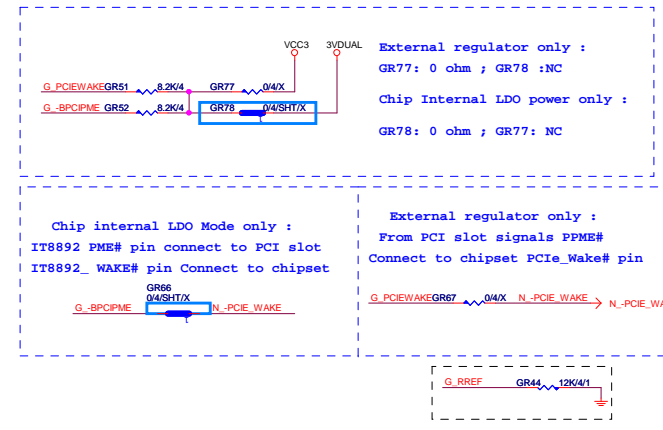
High: PCICLK INPUT form CLK Gen  
Low: PCICLK OUTPUT form IT8893 chip



可變  
O\_PPMRST2

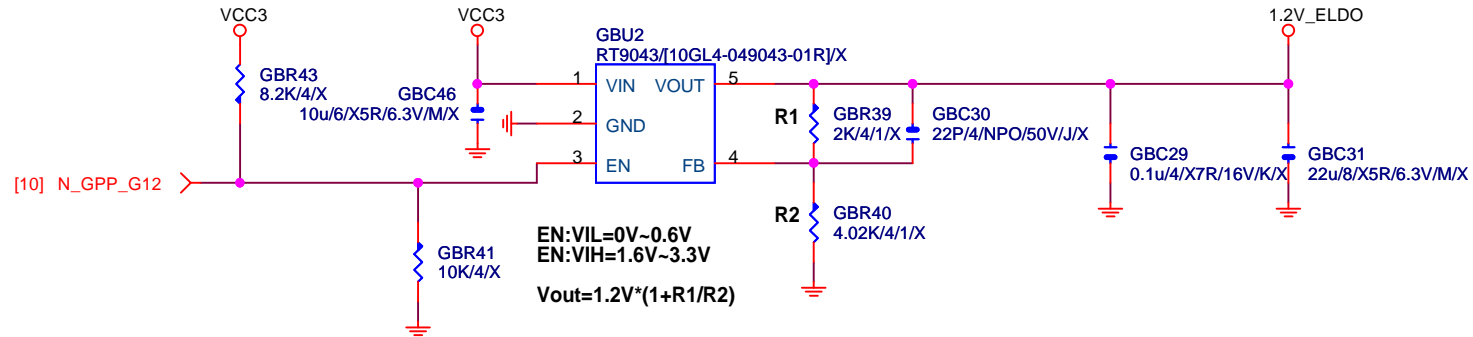
可變  
G\_PBCLK  
G\_PBCLK

Component change note	
IT8892FX	GR70,GR74,GR76,GR78,GR66 : ON GR69,GR73,GR75,GR77,GR67 : NC GR44 resistor is 12k ohm GL14,GL10,GL16,GL17 : ON GL19,GL21,GL23,GL25: NC
IT8892JX	GR70,GR73,GR75,GR78,GR66 : ON GR69,GR74,GR76,GR77,GR67 : NC GR44 resistor is 18k ohm GL14,GL10,GL16,GL17 : ON GL19,GL21,GL23,GL25: NC
External LDO Power (IT8892JX)	GR69,GR73,GR75,GR77,GR67 : ON GR70,GR78,GR66 : NC GR44 resistor is 18k ohm GL19,GL21,GL23,GL25 : ON GL14,GL10,GL16,GL17 : ON



Rev 0.1

\* 全部不上件



Gigabyte Technology

Title

LDO POWER

Size  
Custom

Document Number

GA-Z270M-D3P

Rev  
1.01

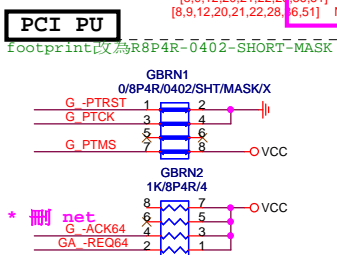
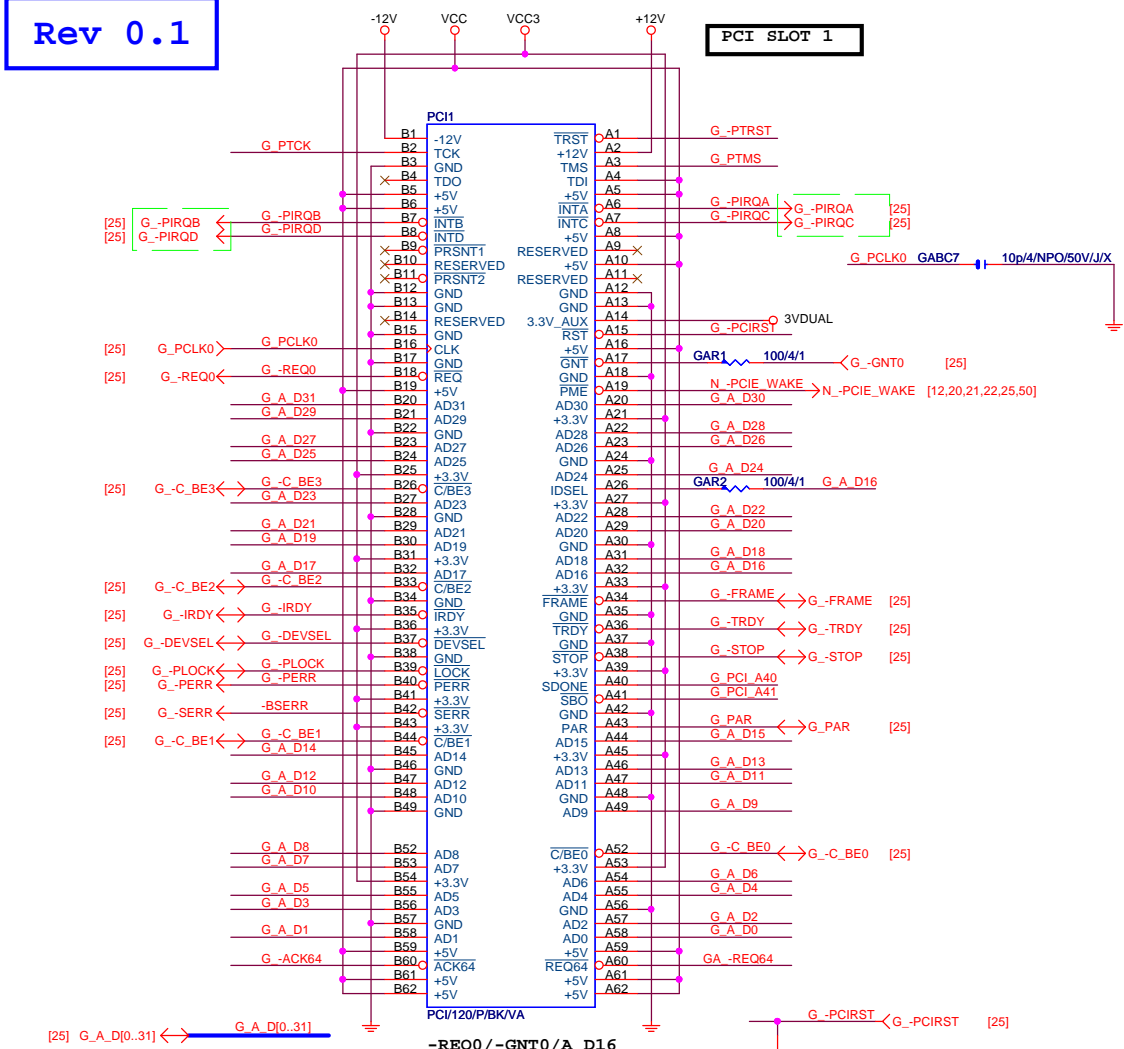
Date:

Monday, December 19, 2016

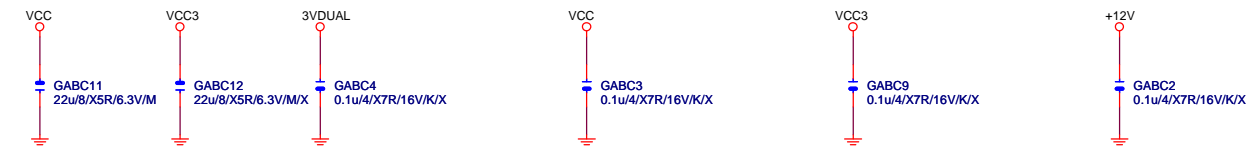
Sheet

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**PCI CAP**



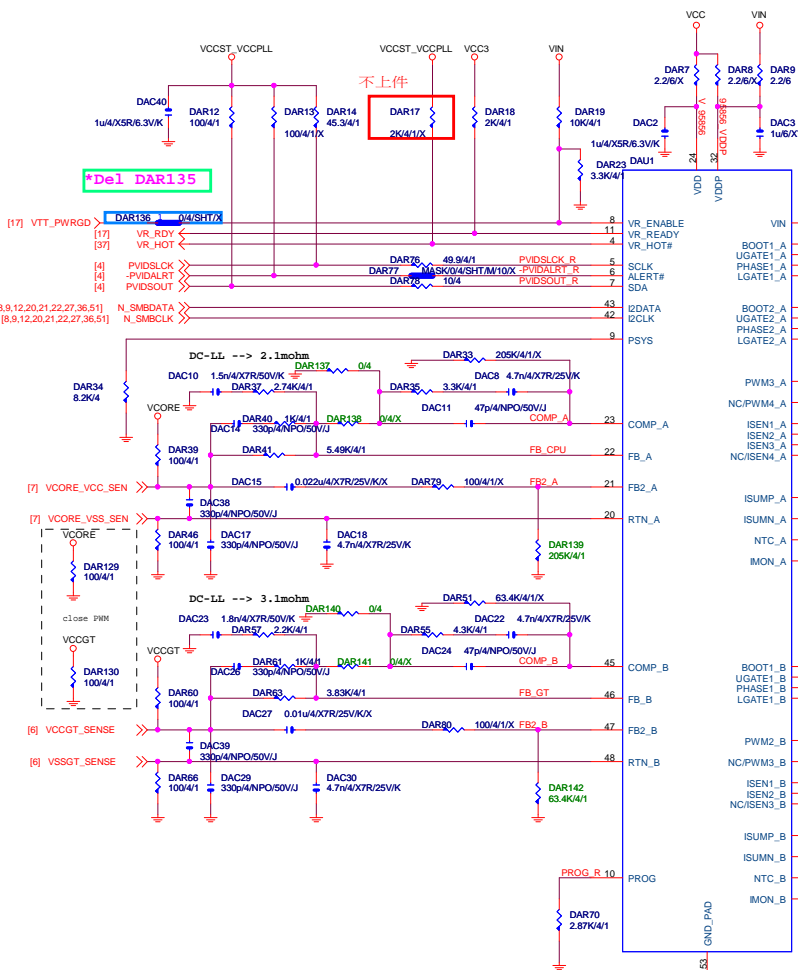
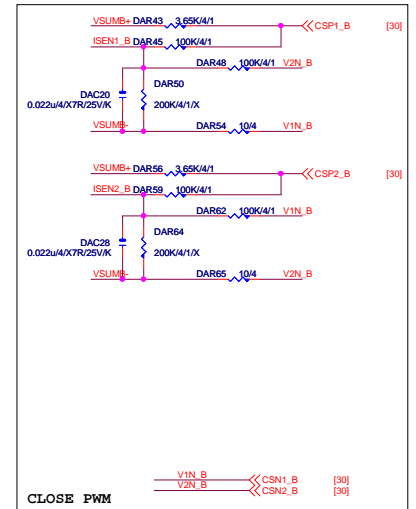
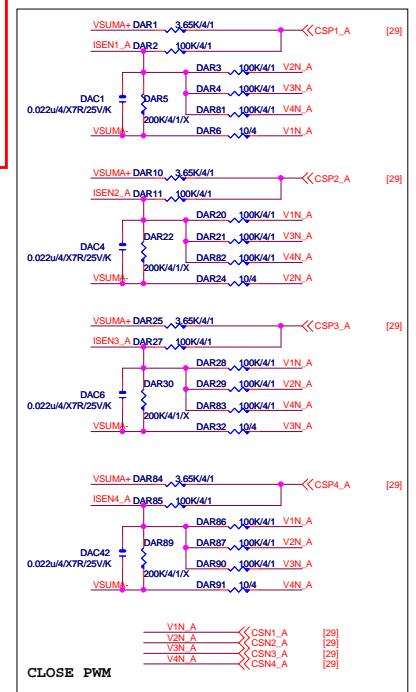
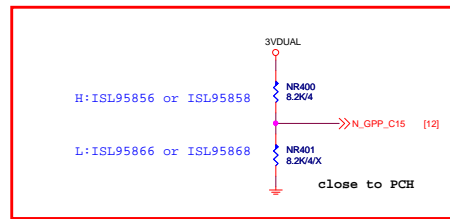
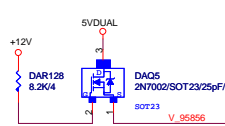
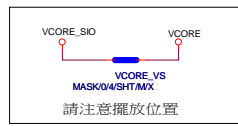
**GIGABYTE™**

Title: **PCI SLOT 1**

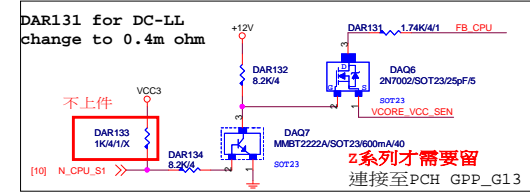
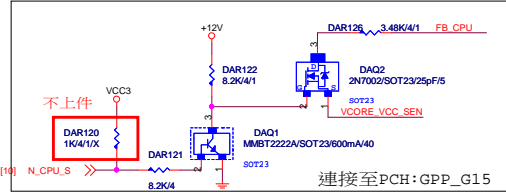
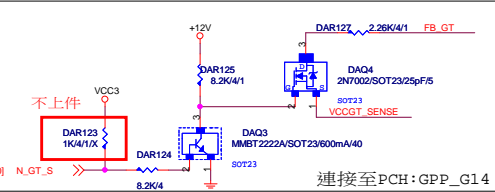
Size: Custom | Document Number: **GA-Z270M-D3P** | Rev: 1.01

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0.2 (IRON CHOKE)



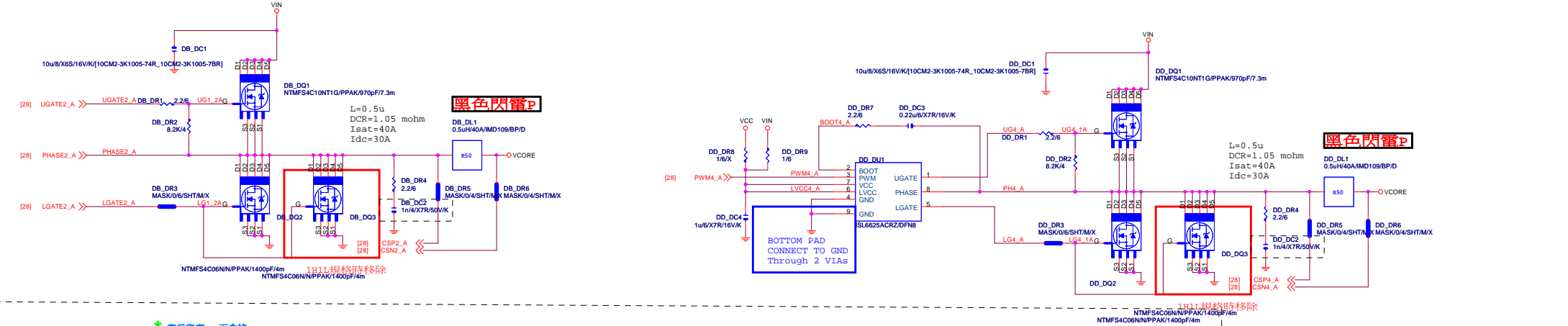
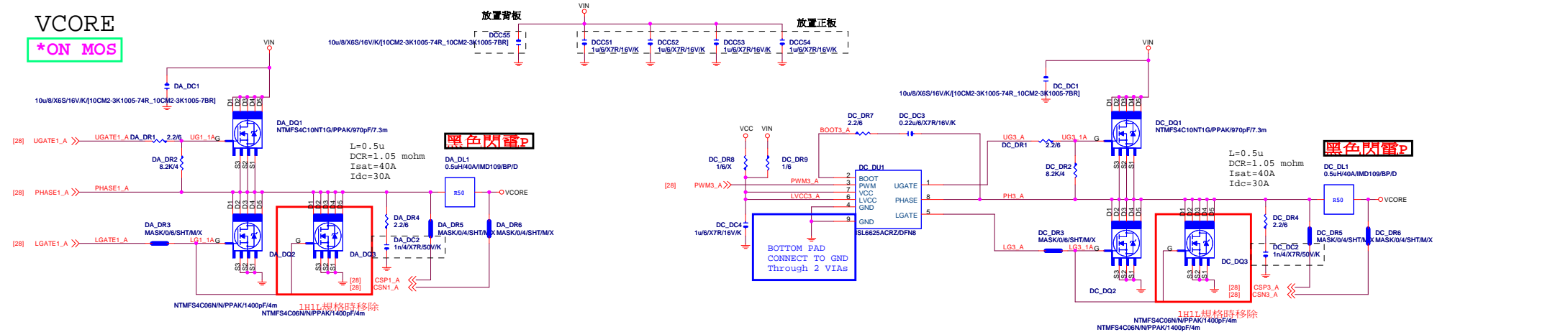
Vcore	ISL95856	ISL95866	VCCGT	ISL95856	ISL95866
DAR137	X	V	DAR140	X	V
DAR138	V	X	DAR141	V	X
DAR139	X	V	DAR142	X	V
DAC15	V	X	DAC27	V	X
DAR79	V	X	DAR80	V	X
DAR33	V	X	DAR51	V	X



0.2 (IRON CHOKE)

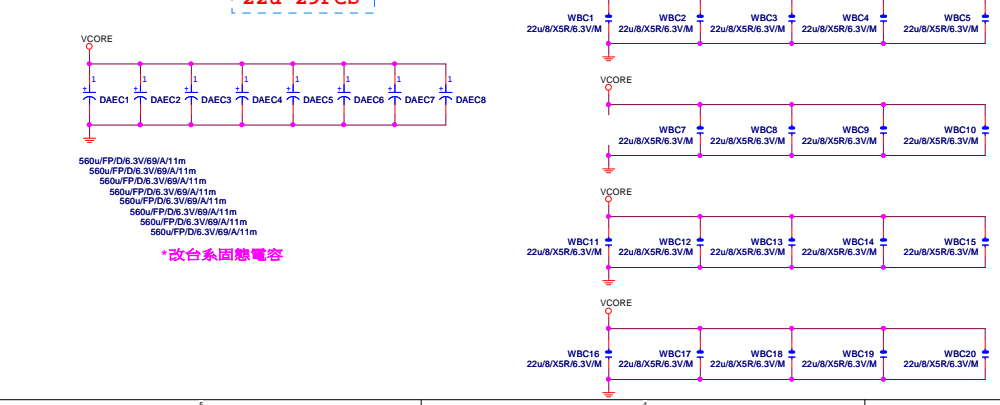
VCORE

\*ON MOS



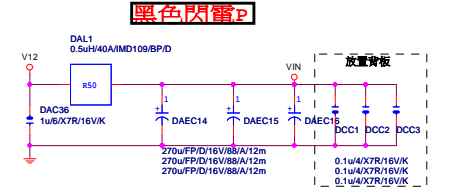
VCORE CAP

\* 客戶指定，不拿掉  
560u\*8PCS  
22u\*29PCS



VIN CAP

\*改台系固態電容  
270u\*3PCS



**GIGABYTE**

Title: ISL95866\_MOS\_VCORE

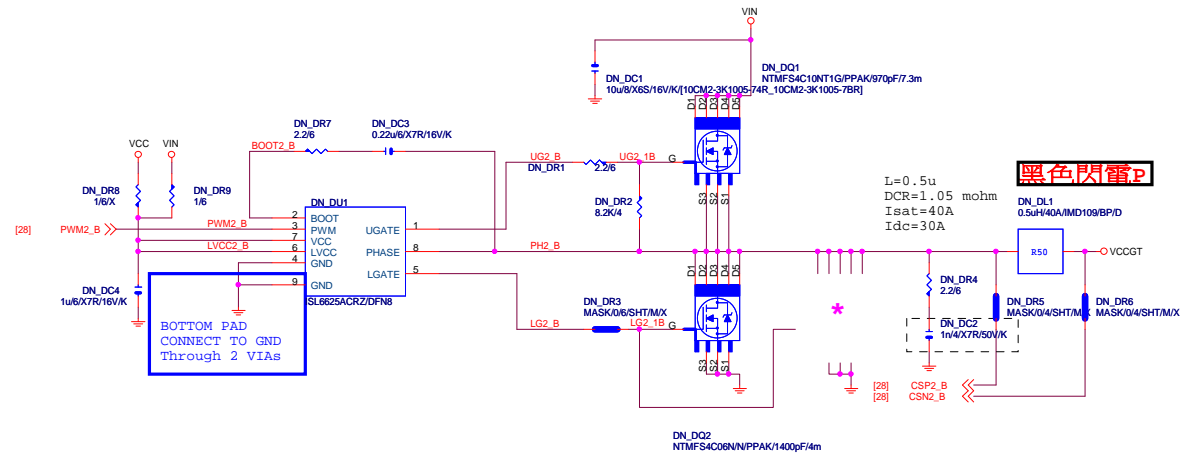
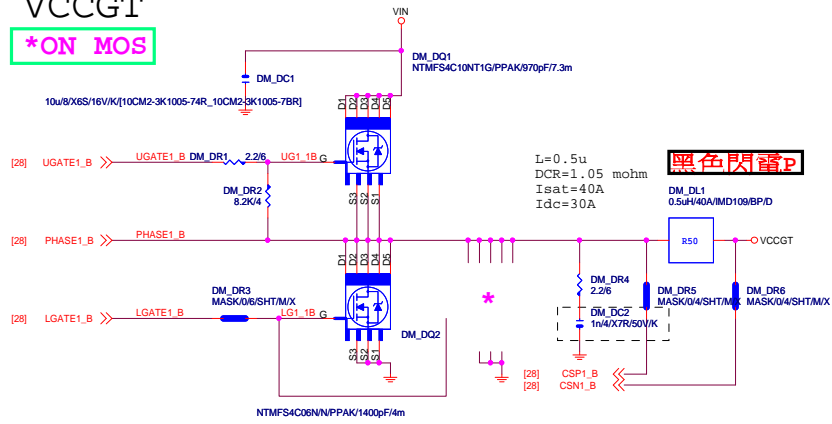
Size: Custom Document Number: GA-Z270M-D3P Rev: 1.01

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# 0.2 (IRON CHOKE)

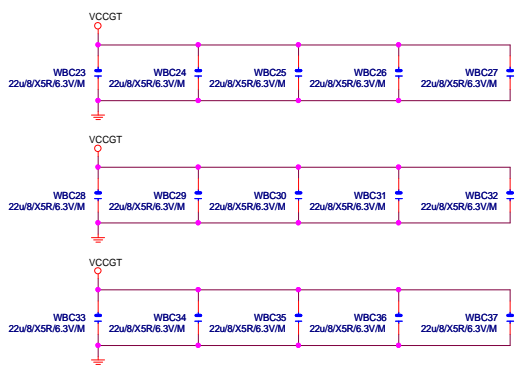
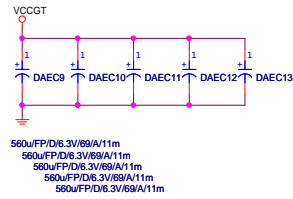
## VCCGT

\*ON MOS



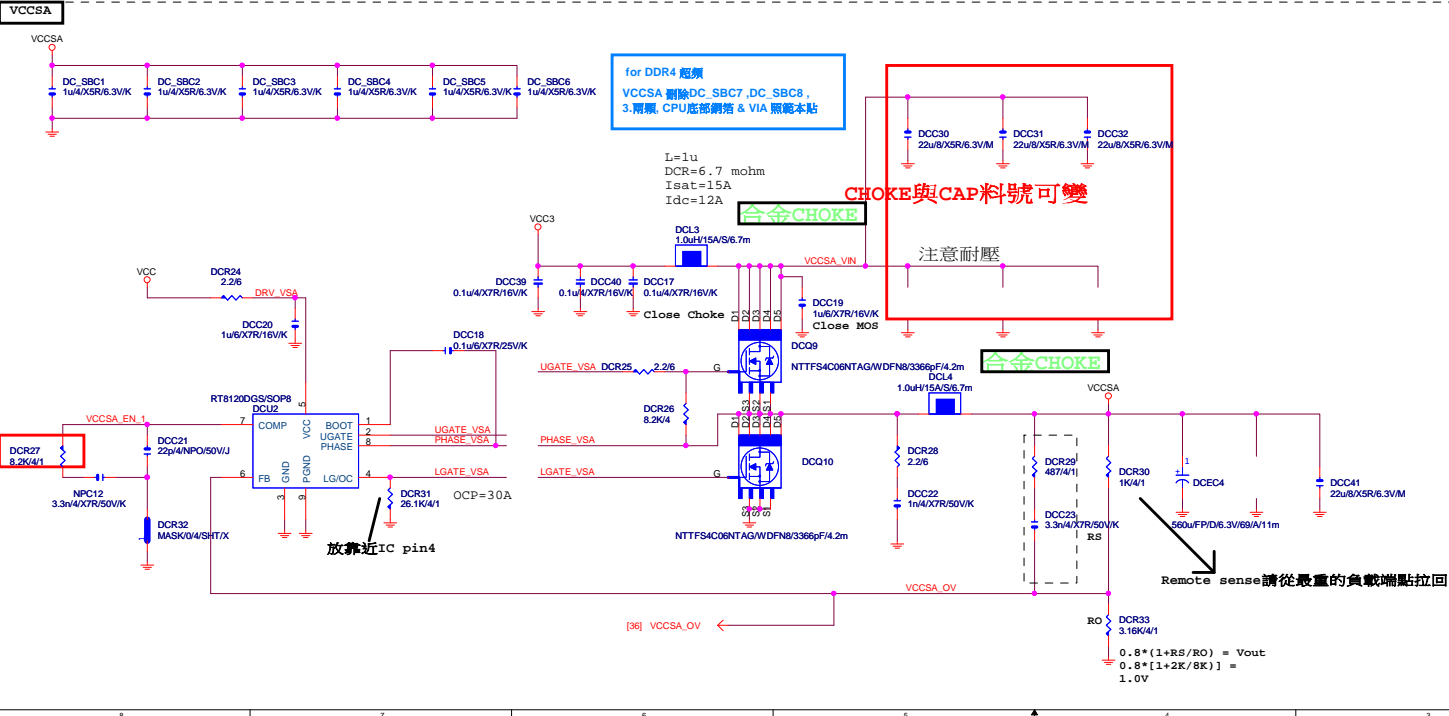
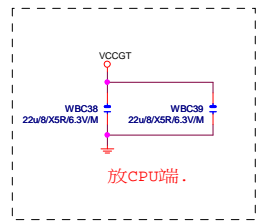
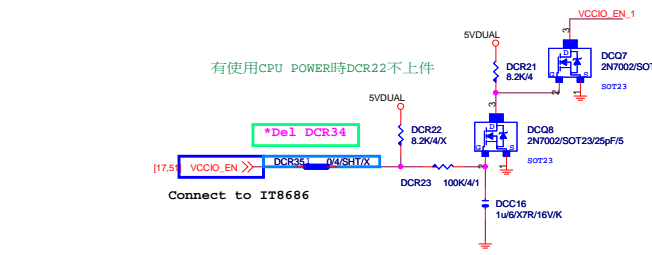
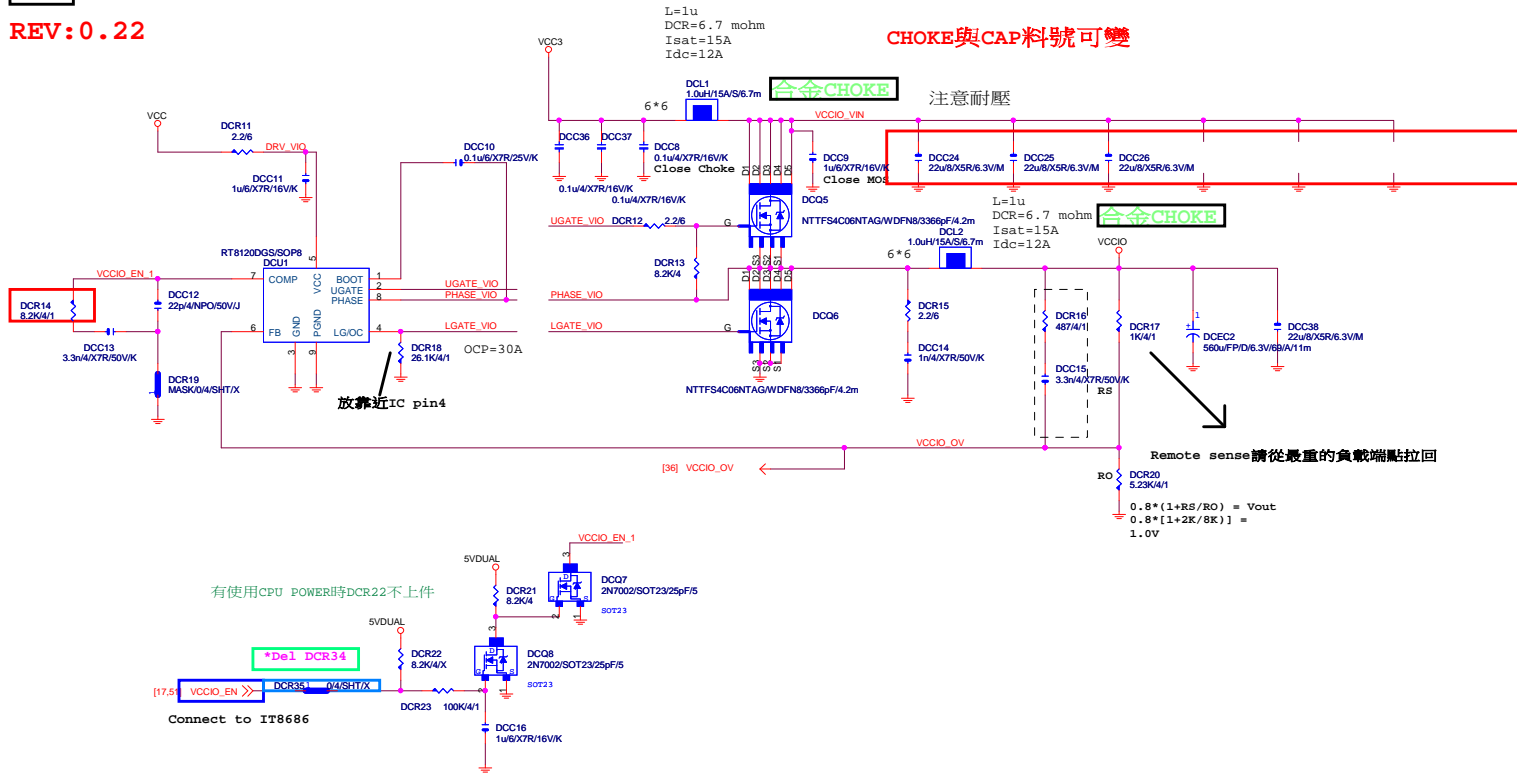
## VCCGT CAP

\* 客戶指定，不拿掉  
 560u\*5PCS  
 22u\*15PCS



\*改台系固態電容

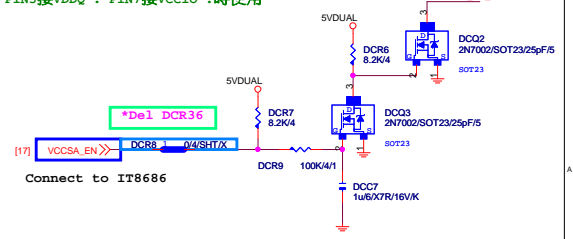
<b>GIGABYTE™</b>		
Title: <b>ISL95866_MOS_VCCGT</b>		
Size:	Document Number:	Rev:
Custkm:	<b>GA-Z270M-D3P</b>	<b>1.01</b>
Date:	Monday, December 19, 2016	Sheet 30 of 55



for DDR4 超頻  
VCCSA 刪除DC\_SBC7, DC\_SBC8,  
3.兩顆, CPU底部銅箔 & VIA 照範本貼

SIO PINS . PIN7 用在其他function時使用

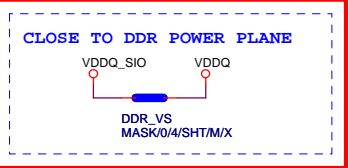
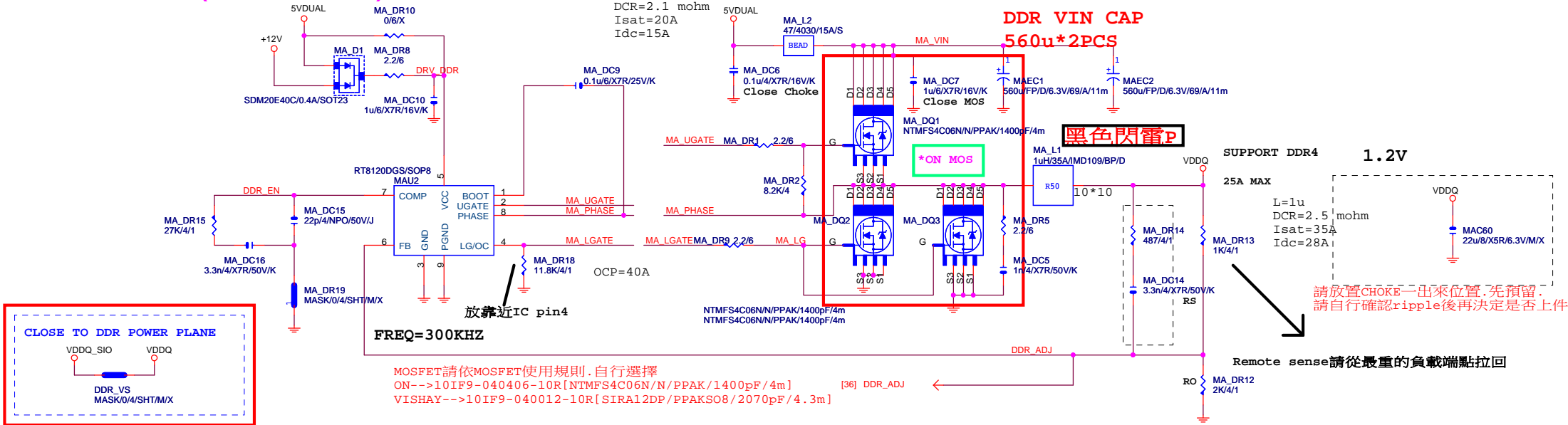
SIO PINS接VDDQ . PIN7接VCCIO . 時使用



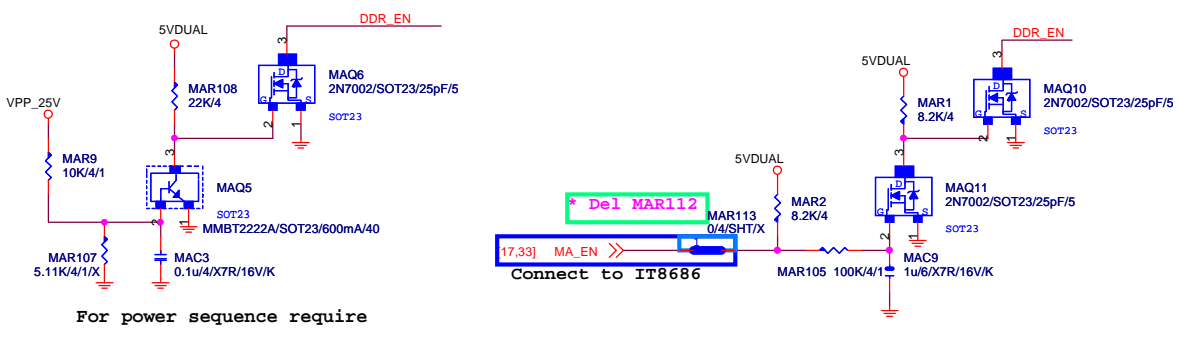
**DDR4**

**REV:0.2 (IRON CHOKE)**

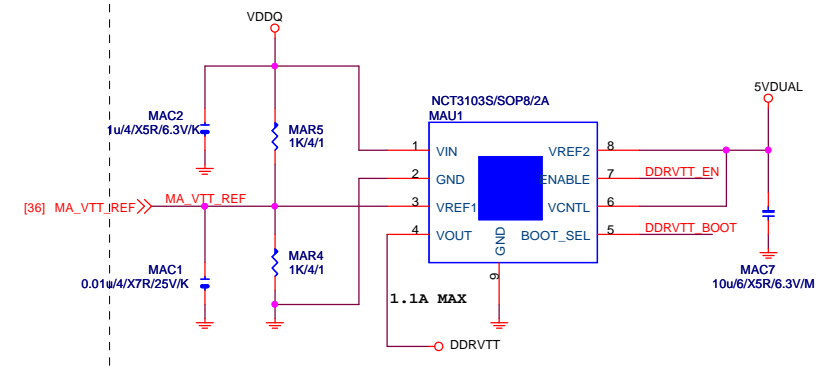
L=0.5u  
DCR=2.1 mohm  
Isat=20A  
Idc=15A



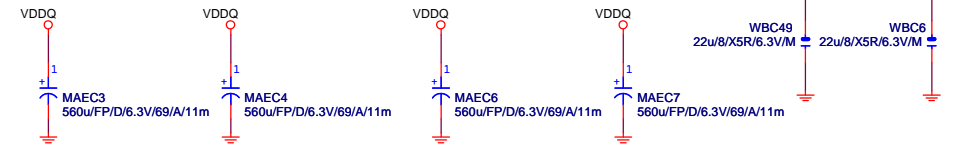
**PWR SEQ**



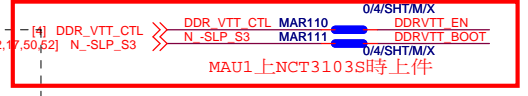
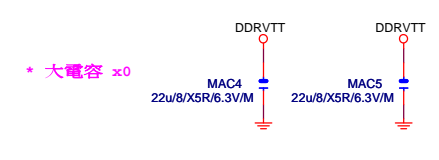
**DDRVTT**



**DDR CAP**



**DDRVTT CAP**



Title		Rev	
<b>RT8120_DDR POWER</b>		1.01	
Size	Document Number		
Custom	<b>GA-Z270M-D3P</b>		
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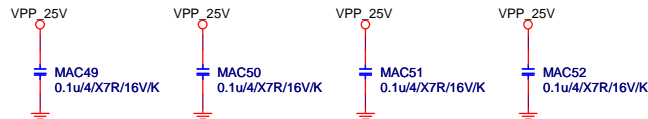
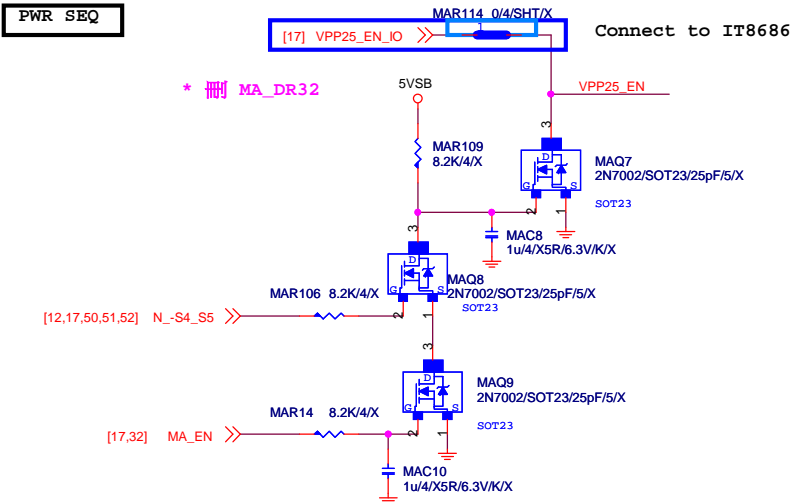
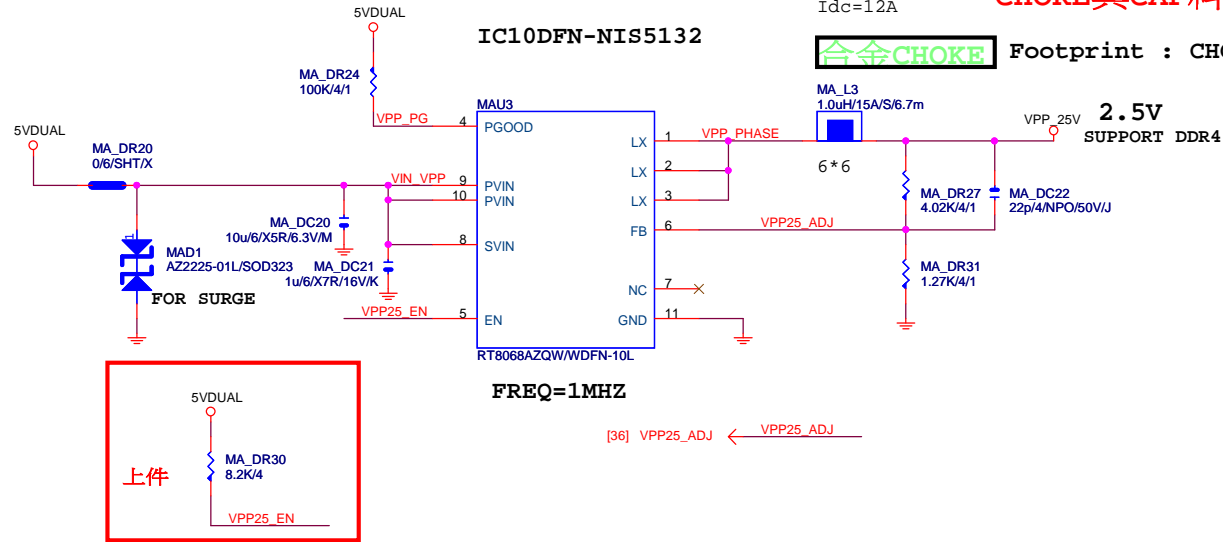


L=1u  
DCR=6.7 mohm  
Isat=15A  
Idc=12A

CHOKE與CAP料號可變

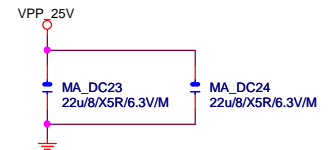


Footprint : CHOKE6X6mm\_SMD-1



22u\*2PCS

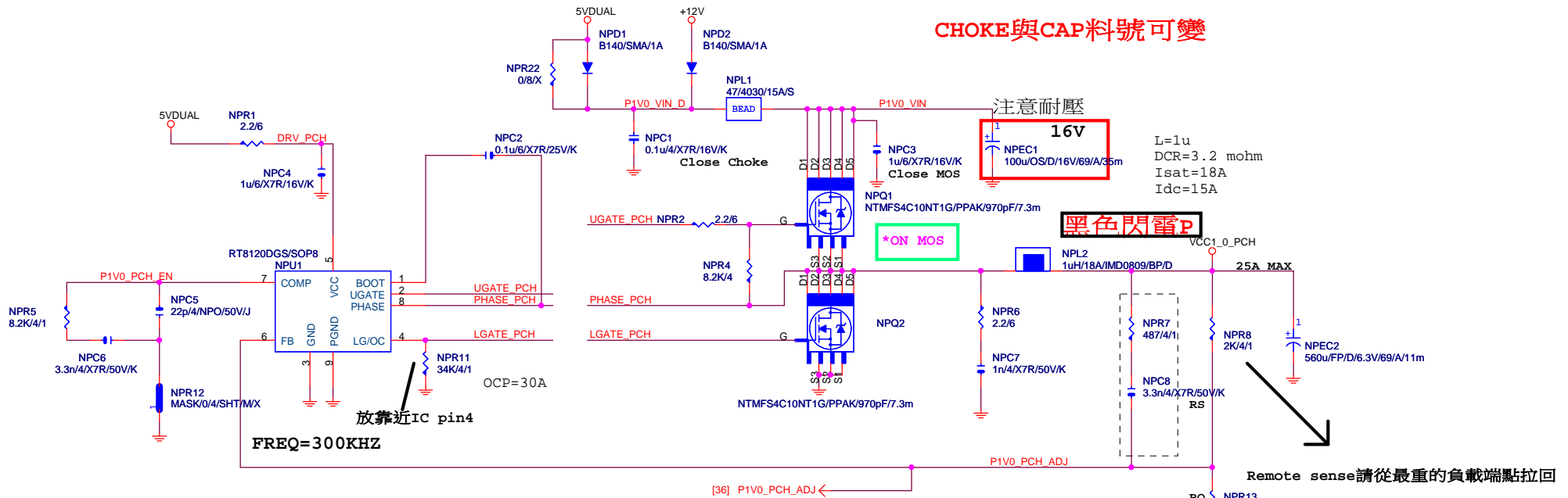
\* 大電容 x0



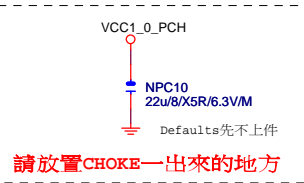
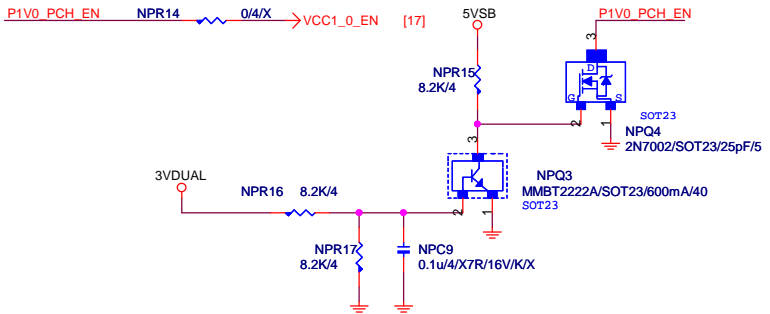
# GIGABYTE™

Title		
RT8068A_VPP25 POWER		
Size	Document Number	Rev
Custom	GA-Z270M-D3P	1.01
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CHOKE與CAP料號可變



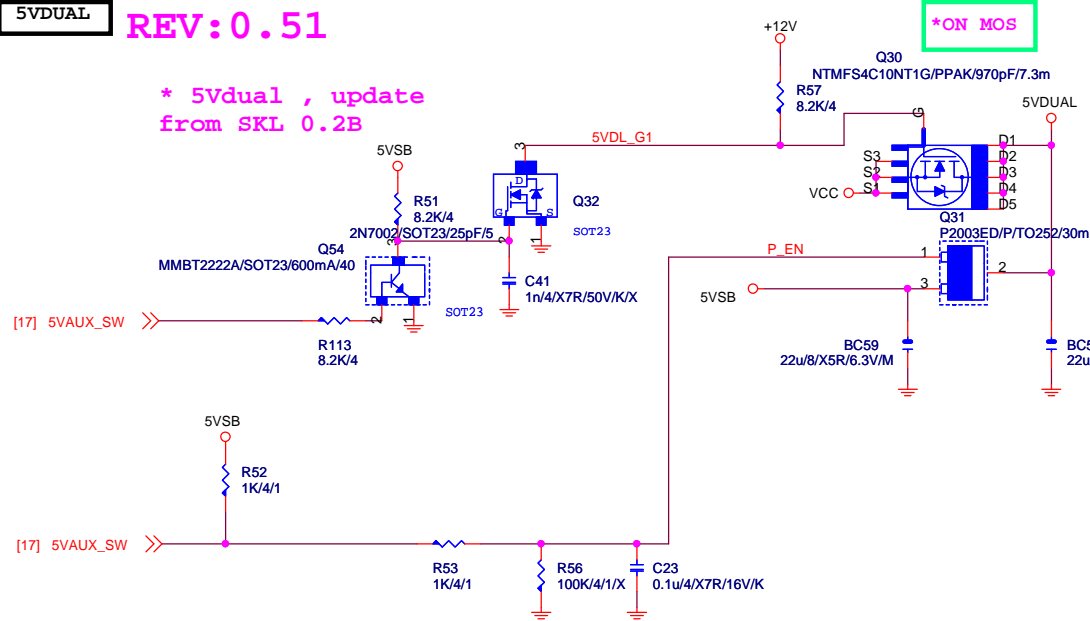
PWR SEQ



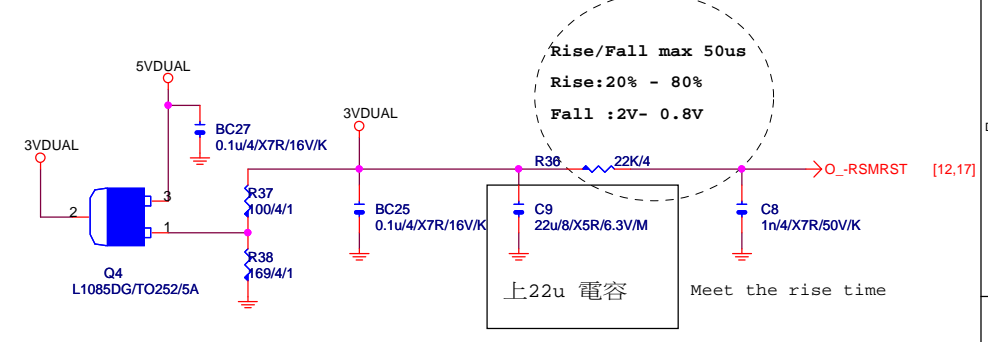
<b>GIGABYTE™</b>			
Title <b>RT8120_PCH POWER</b>			
Size Custom	Document Number <b>GA-Z270M-D3P</b>		Rev <b>1.01</b>
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**5VDUAL** REV:0.51

\* 5Vdual , update from SKL 0.2B



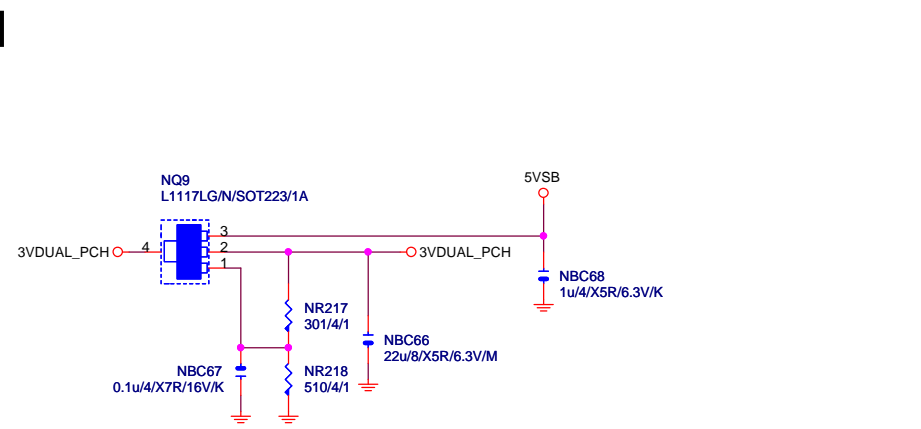
**3VDUAL**



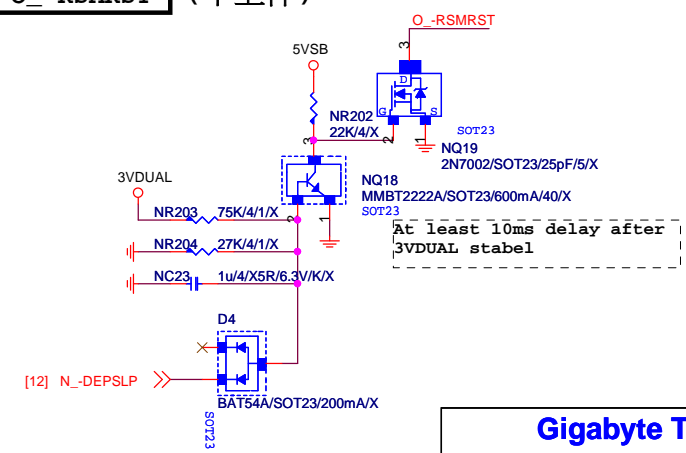
Rise/Fall max 50us  
Rise:20% - 80%  
Fall :2V- 0.8V

上22u 電容 Meet the rise time

**3VDUAL\_PCH**



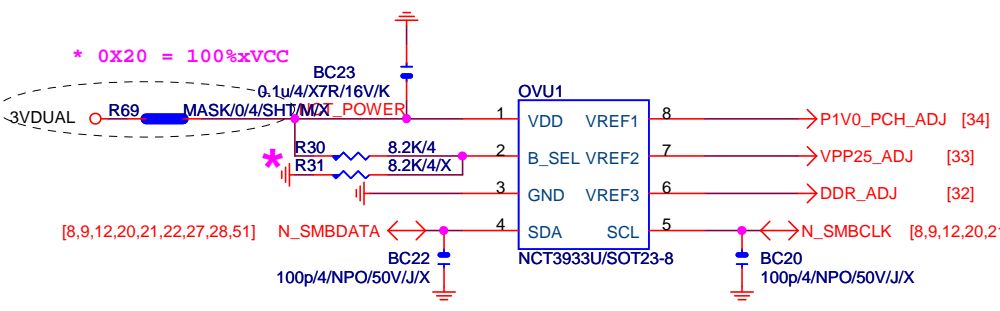
**O\_-RSMRST (不上件)**



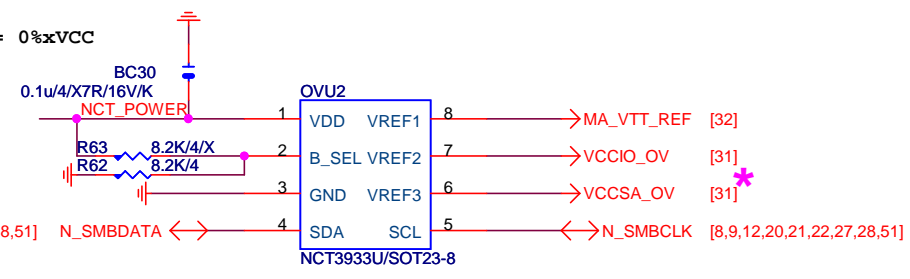
At least 10ms delay after 3VDUAL stabel

<b>Gigabyte Technology</b>			
Title			
<b>DISCRETE POWER</b>			
Size	Document Number	<b>GA-Z270M-D3P</b>	
Custom			Rev <b>1.01</b>
Date:	Monday, December 19, 2016	Sheet	35 of 55

**OVER VOLTAGE**



0X2A = 0%xVCC



0X22 = 75%xVCC

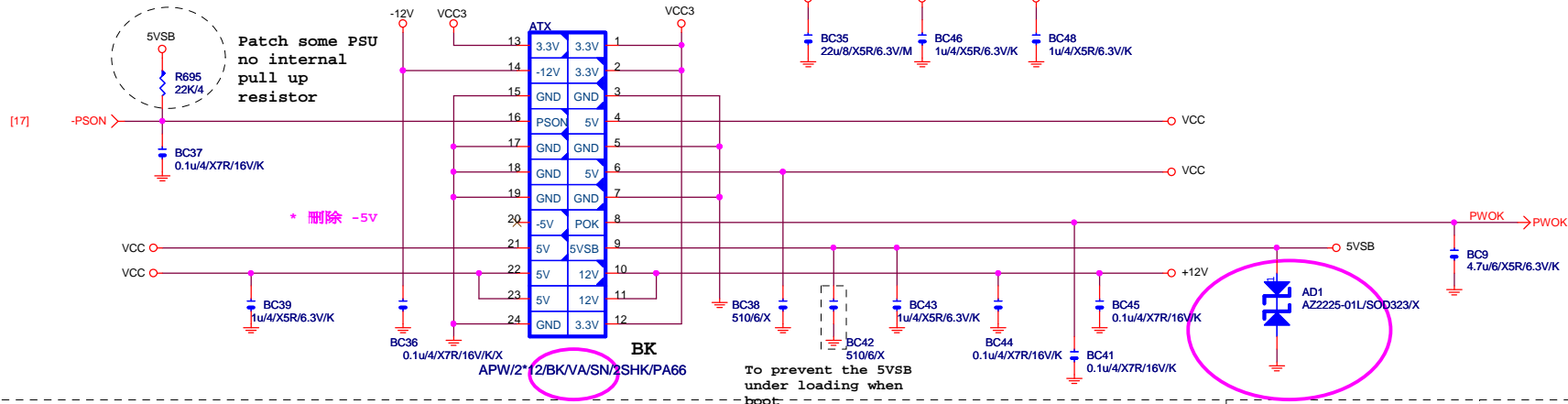
NCT3933	0X20	0X2A
VREF1	VCC1_0_PCH	DDRVTT
VREF2	VPP_25V	VCCIO
VREF3	VDDQ	VCCSA

**Gigabyte Technology**

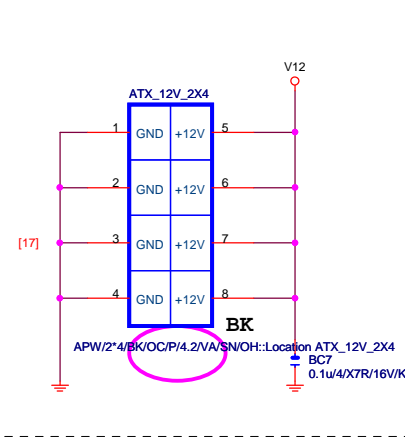
**CPU CORE VR-2**

Size Custom	Document Number	<b>GA-Z270M-D3P</b>	Rev
			<b>1.01</b>
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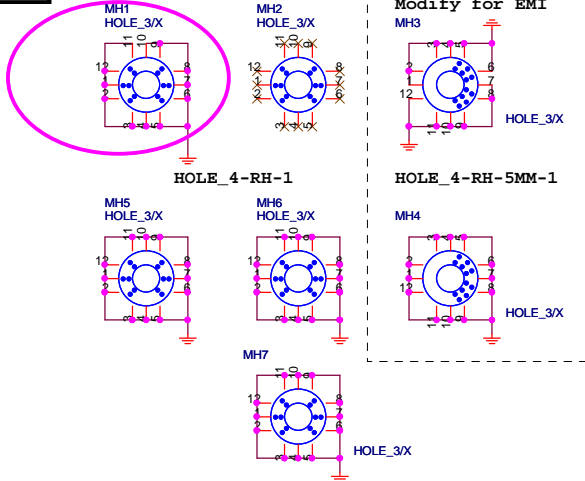
# ATXX24 POWER CONNECTOR



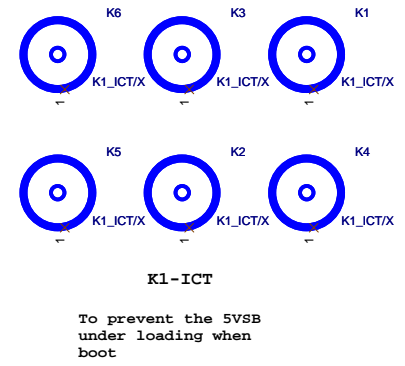
# ATXX4 POWER CONNECTOR



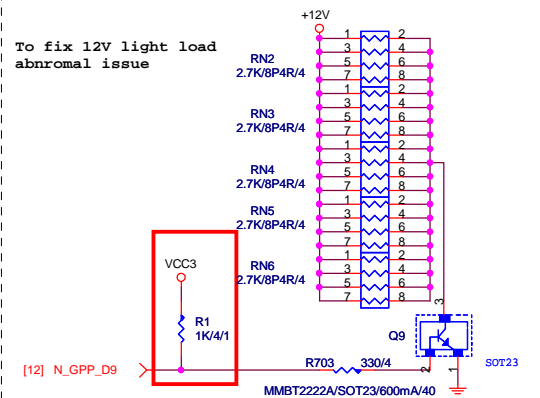
## 螺絲孔



## 固定孔/光學點

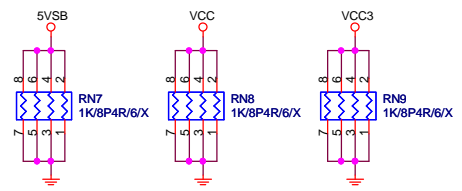


## +12V DUMMY LOAD

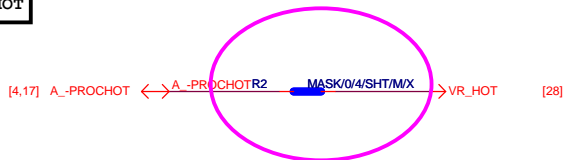


【技術通報R&D技術通報153】

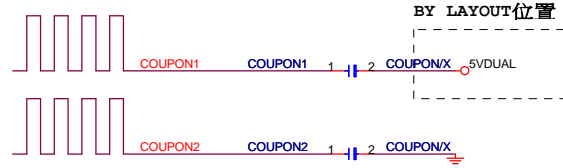
## DUMMY LOAD



## -PROHOT



## COUPON



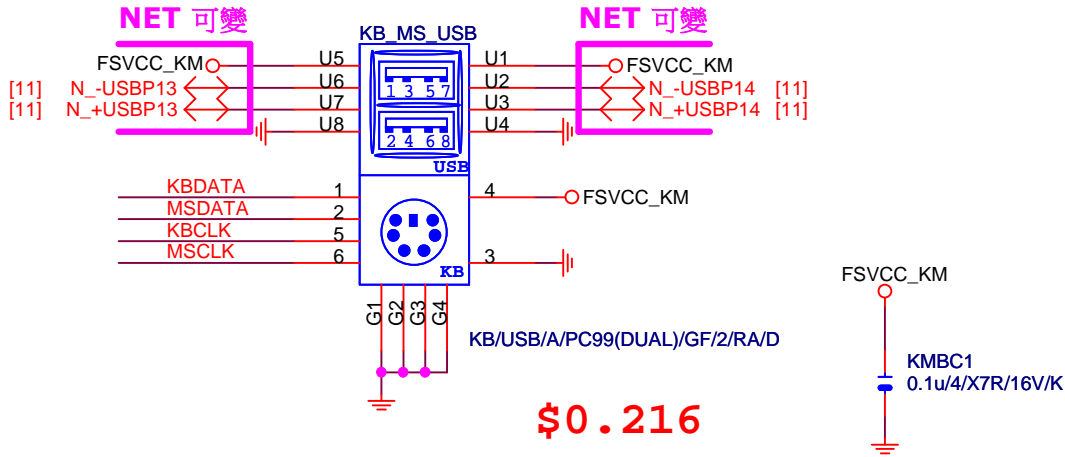
**Gigabyte Technology**

Title: **ATX POWER CONNECTOR**

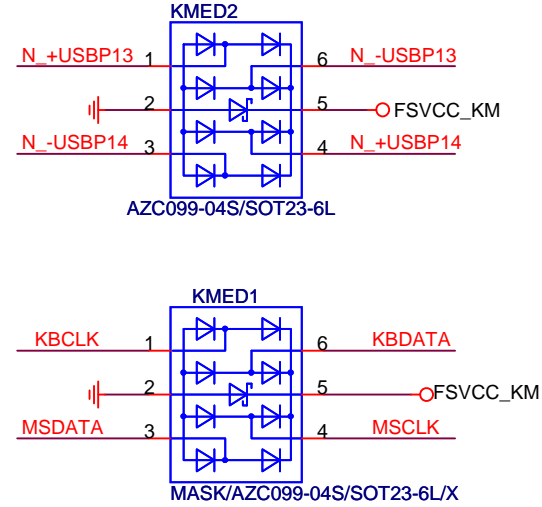
Size: Custom | Document Number: **GA-Z270M-D3P** | Rev: **1.01**

Date: Monday, December 19, 2016 | Sheet: 37 of 55

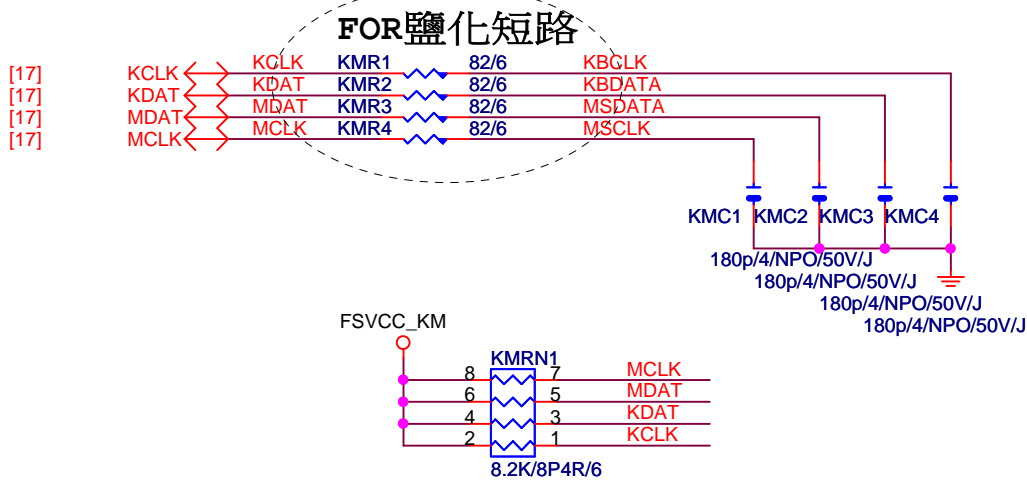
改回原來的上USB, 下PS2



\*SWAP KMED2

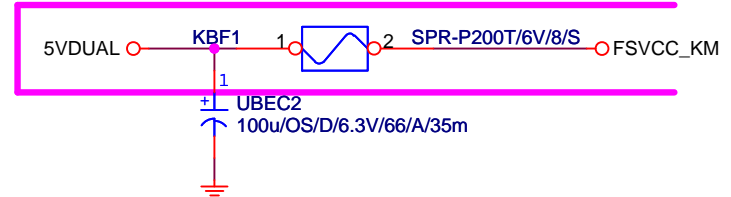


KB\_MS\_USB DAMPING/PU

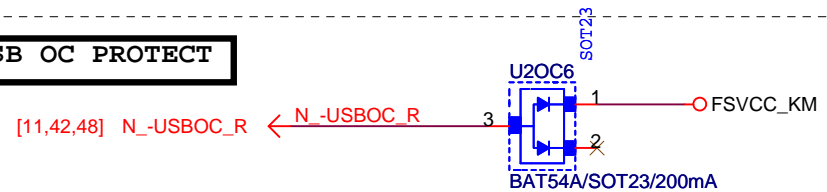


KB\_MS\_USB PWR

NET 可變, 與其他USB SHARE



USB OC PROTECT



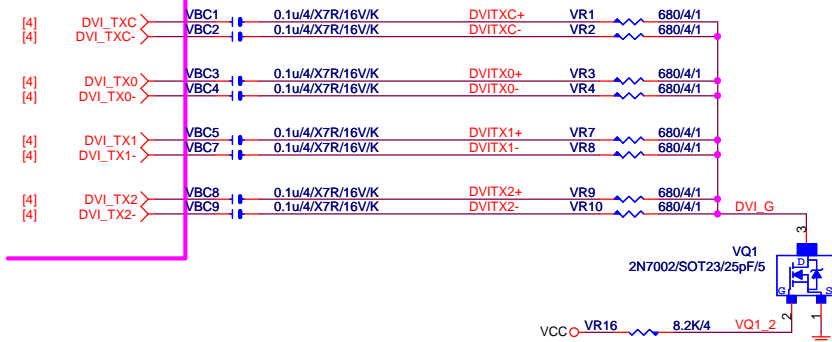
Gigabyte Technology

Title		
KB_MS_USB		
Size	Document Number	Rev
A	GA-Z270M-D3P	1.01
Date:	Monday, December 19, 2016	Sheet 38 of 55

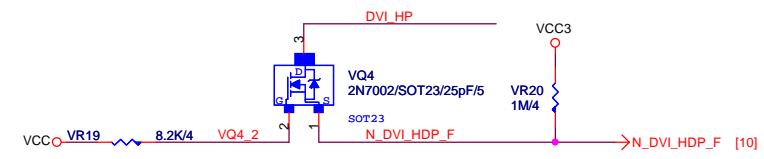
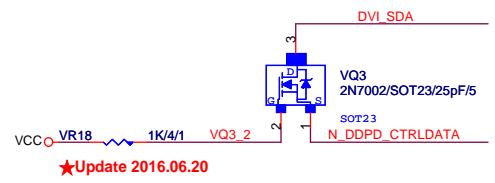
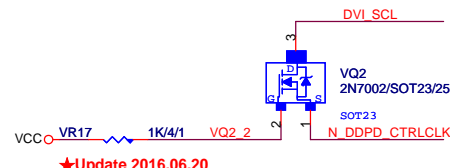
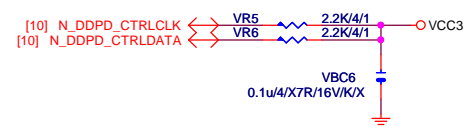
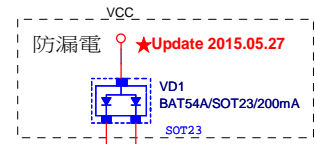
**DVI** Rev: 0.82

DVI: 20/4/6/4/20  
Impedance=85 +/- 17.5%

NET 可變



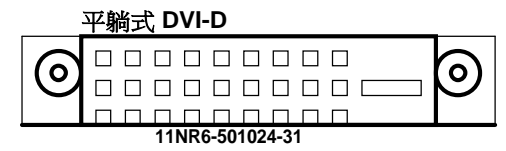
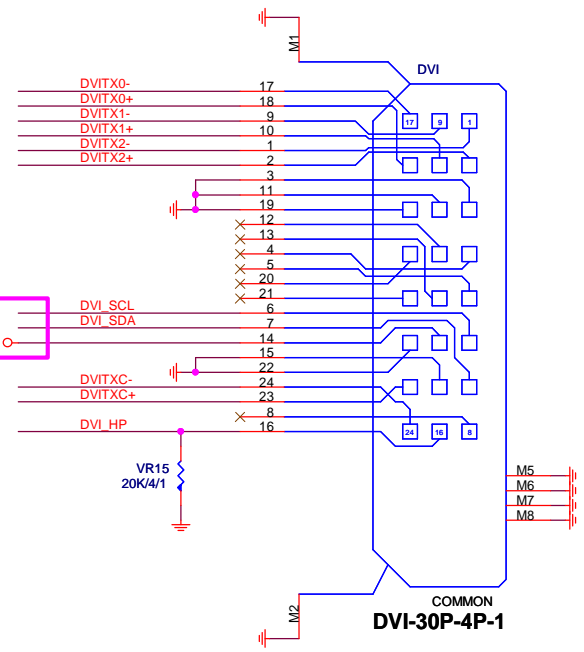
**DVI PU**



**DVI CONN**

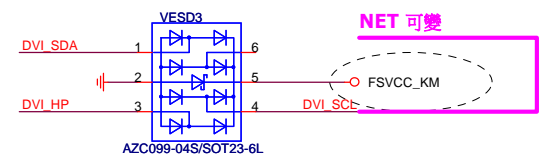
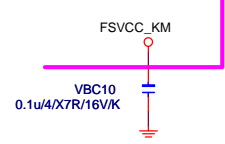
NET 可變

\* FSVCC\_KM

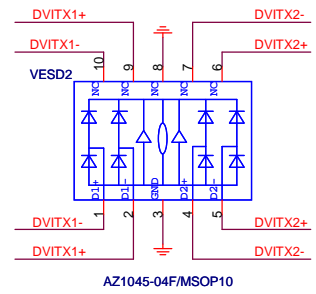


**ESD**

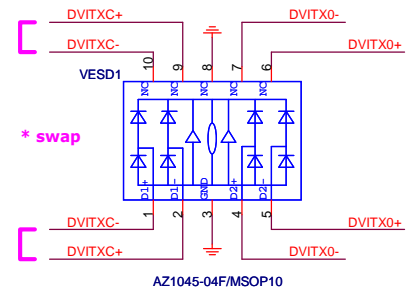
NET 可變



Close to connector

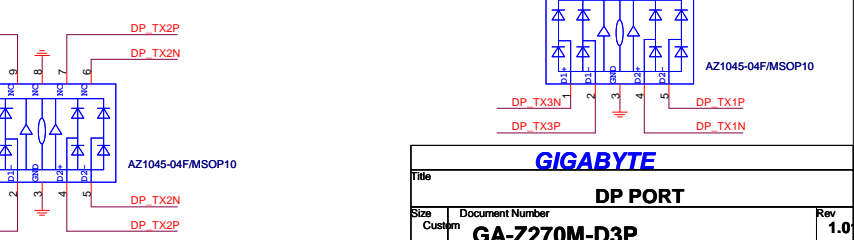
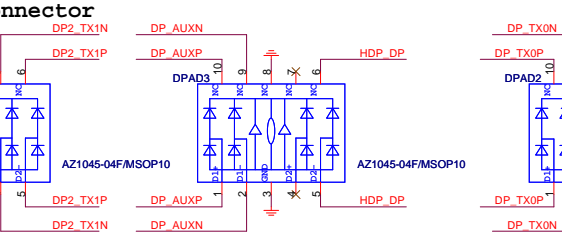
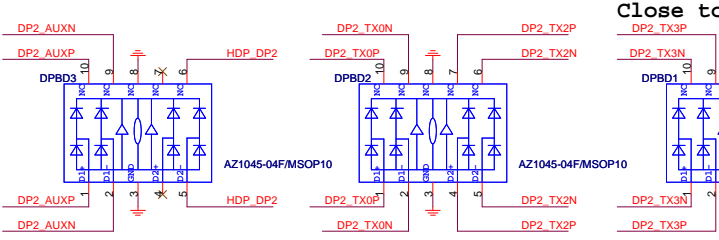
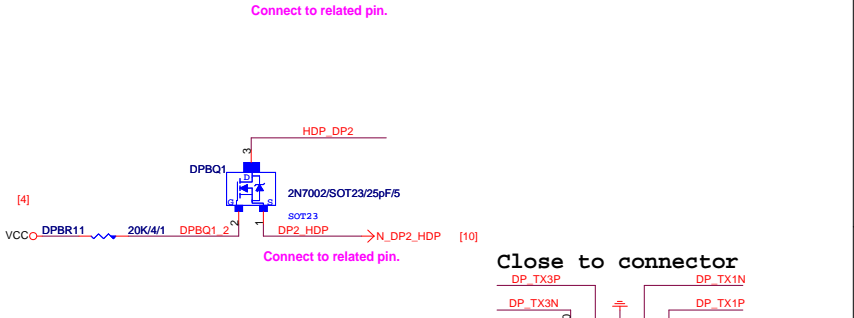
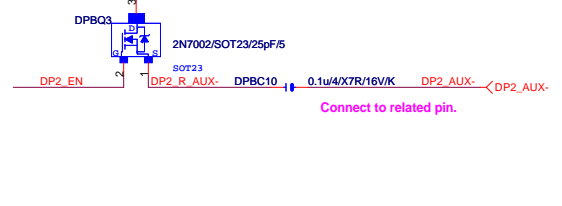
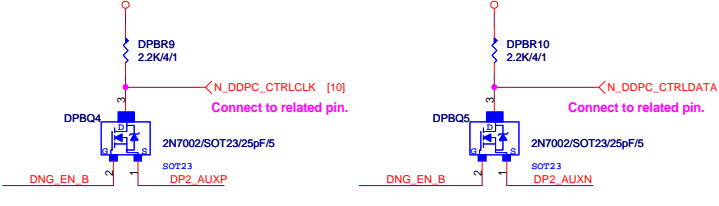
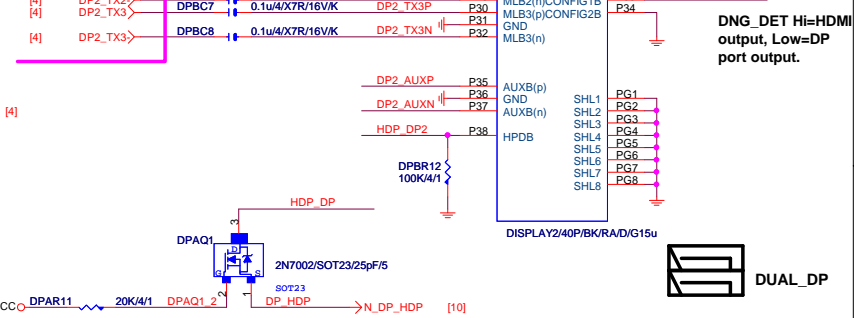
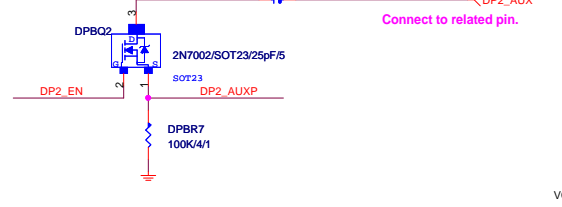
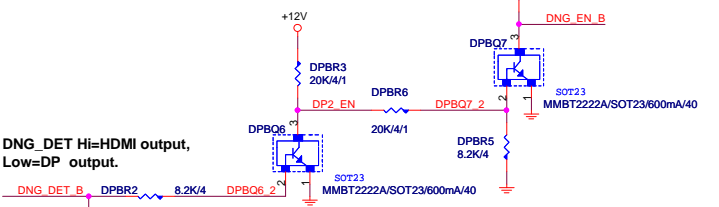
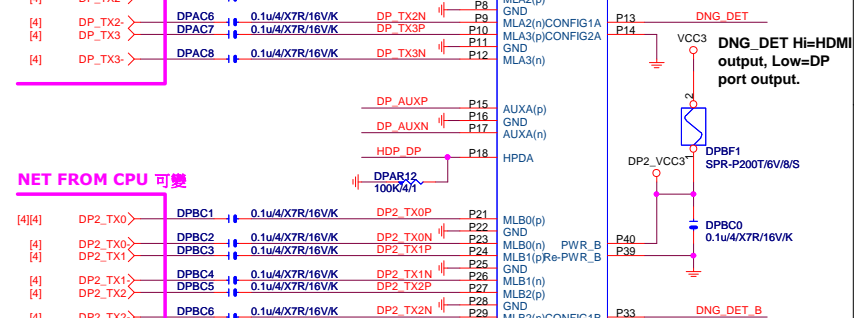
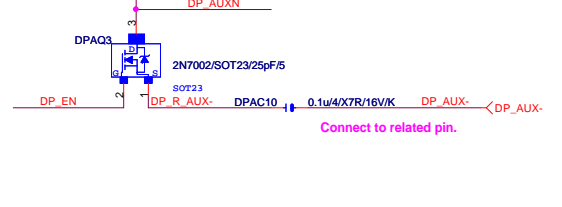
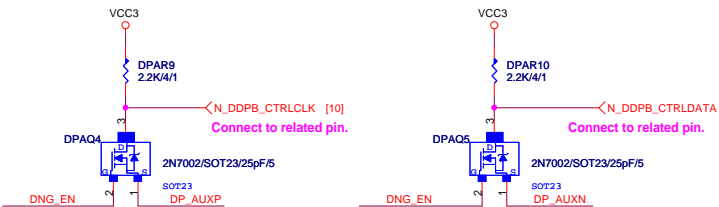
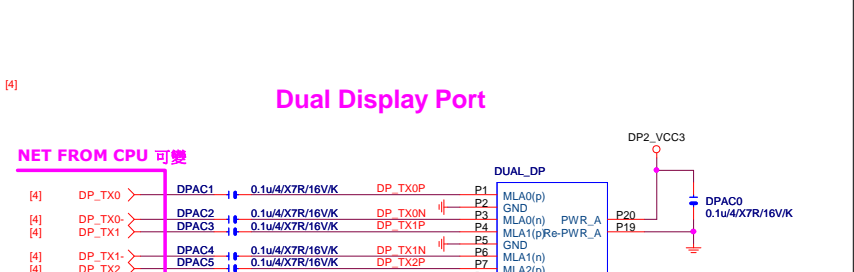
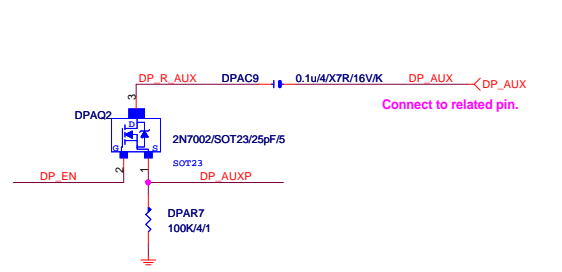
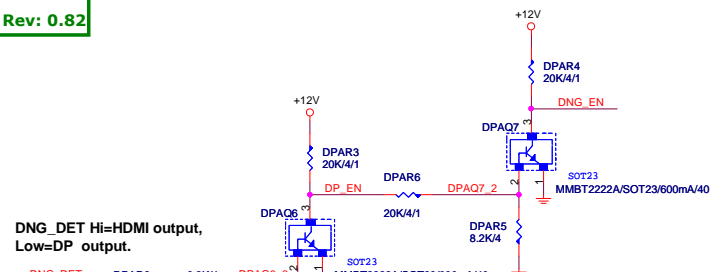


Close to connector



Close to connector

<b>Gigabyte Technology</b>			
Title			
<b>DVI</b>			
Size Custom	Document Number	<b>GA-Z270M-D3P</b>	Rev <b>1.01</b>
Date:	Monday, December 19, 2016	Sheet 39	of 55

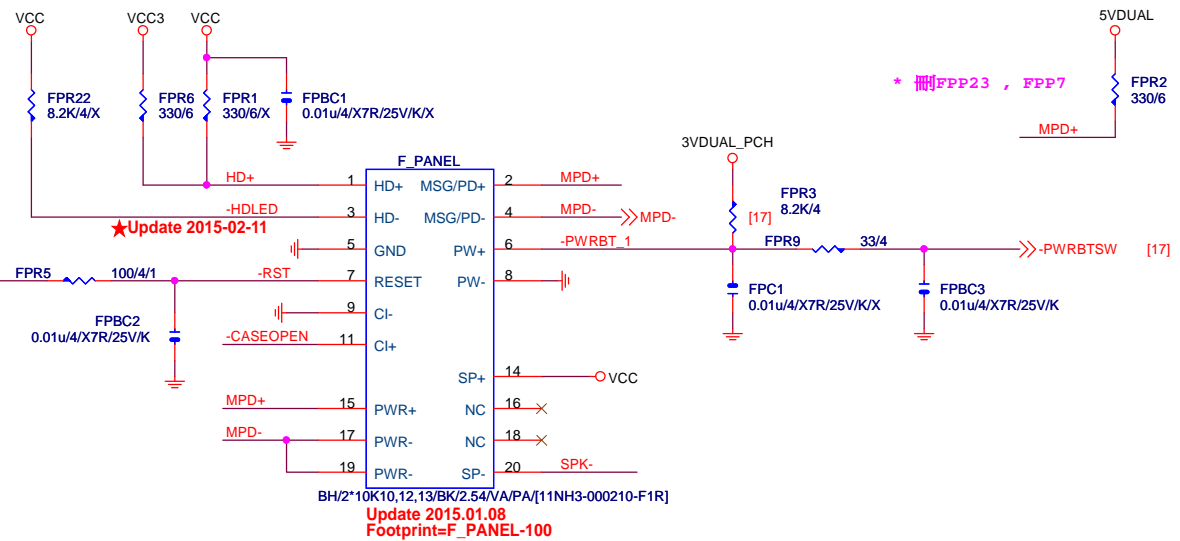




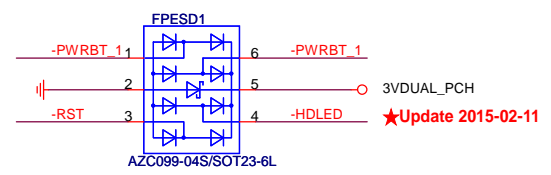
**FRONT PANEL**

**Rev: 0.82**

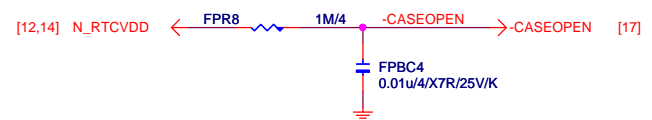
★Update 2016.06.15



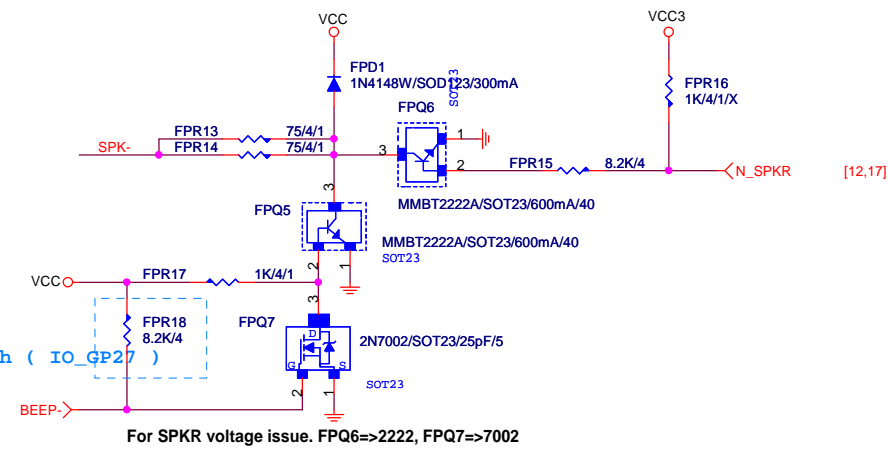
**ESD**



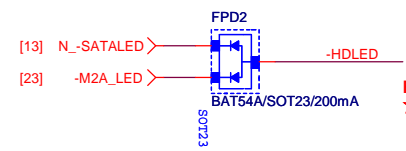
**CASE OPEN**



**SPKR W/O BC**



**SATA/M.2 LED**

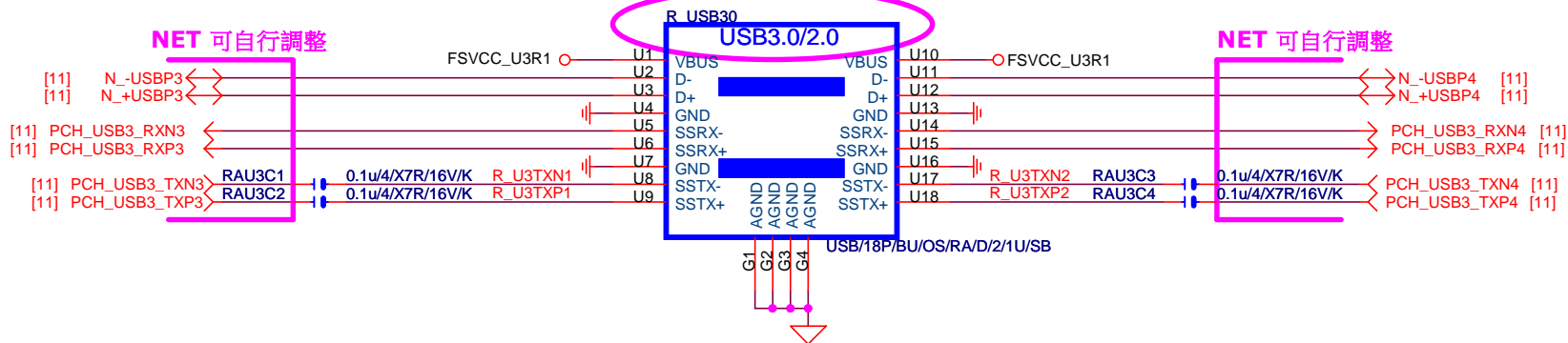


Fix some M.2 cause HD\_LED always on.  
★Update 2016.06.15

Now, import, Pull High ( IO\_GP27 ), IO\_GP26 ouport

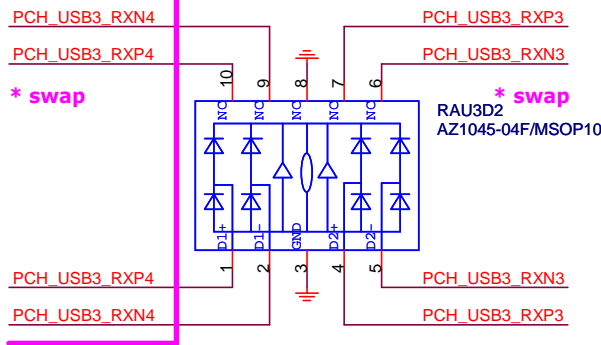
**Gigabyte Technology**

Title		
<b>FRONT PANEL</b>		
Size Custom	Document Number	Rev
	<b>GA-Z270M-D3P</b>	<b>1.01</b>
Date:	Monday, December 19, 2016	Sheet 41 of 55

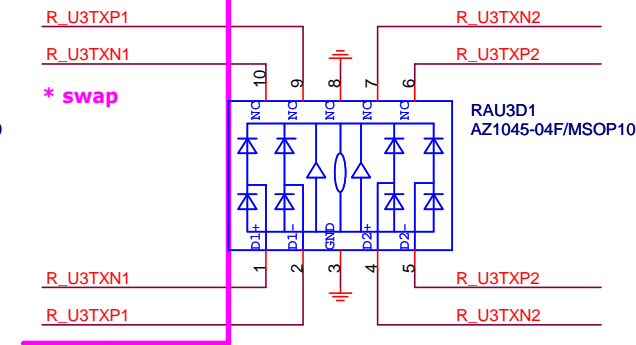


**ESD**

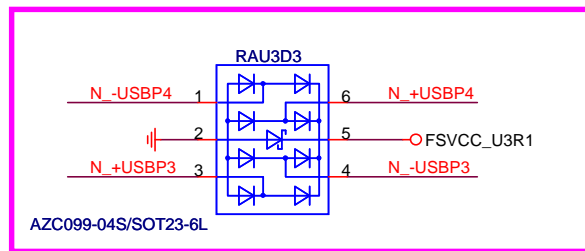
**NET 可自行調整**



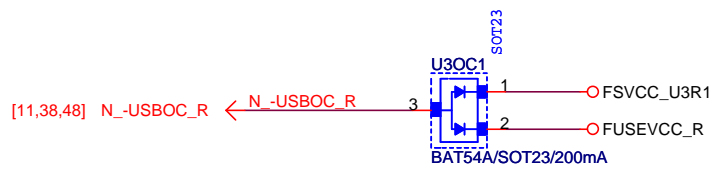
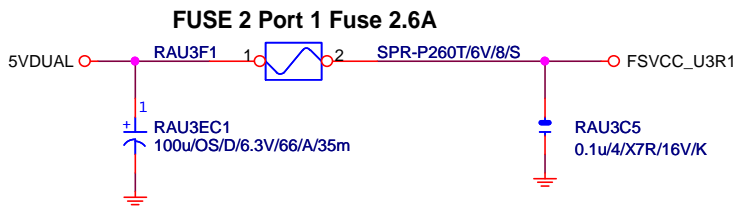
**NET 可自行調整**



**NET 可自行調整**

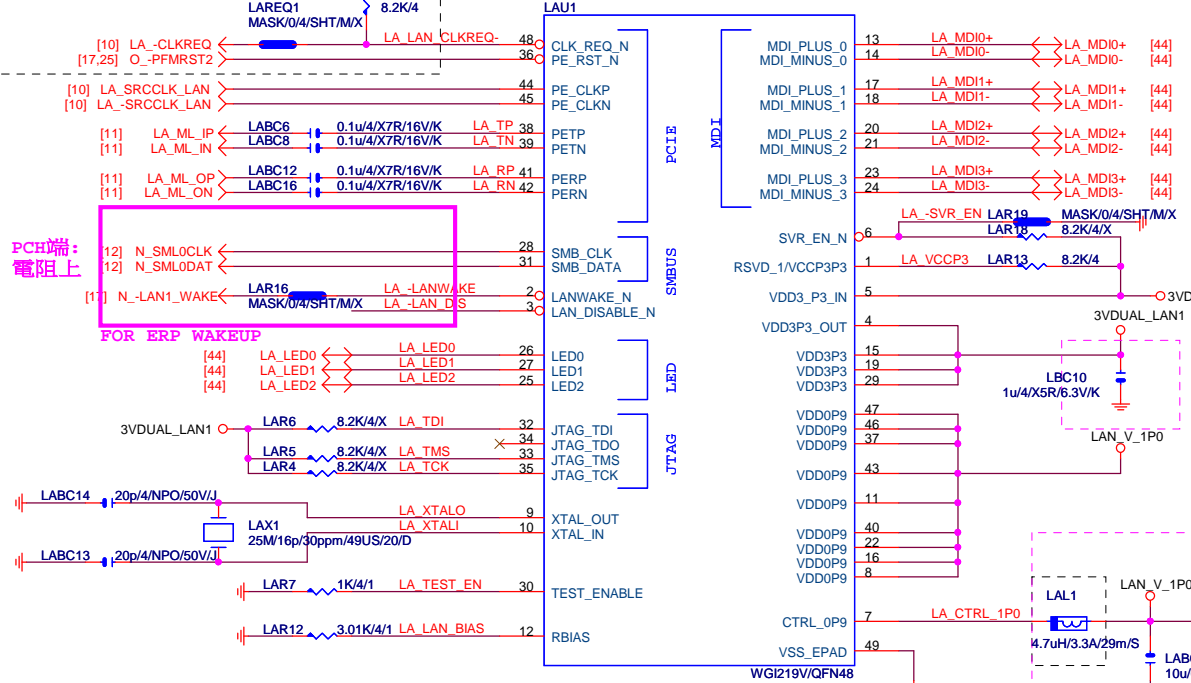


**FUSE**

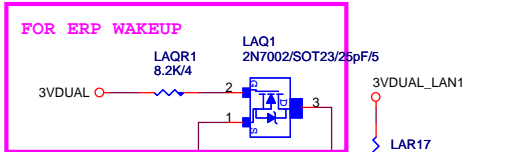
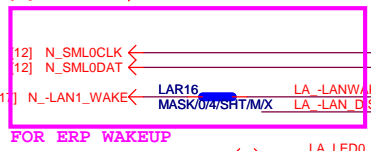


<b>Gigabyte Technology</b>		
<b>R_USB30,USB_OC</b>		
Size Custom	Document Number <b>GA-Z270M-D3P</b>	Rev <b>1.01</b>
Date:	Monday, December 19, 2016	Sheet 42 of 55

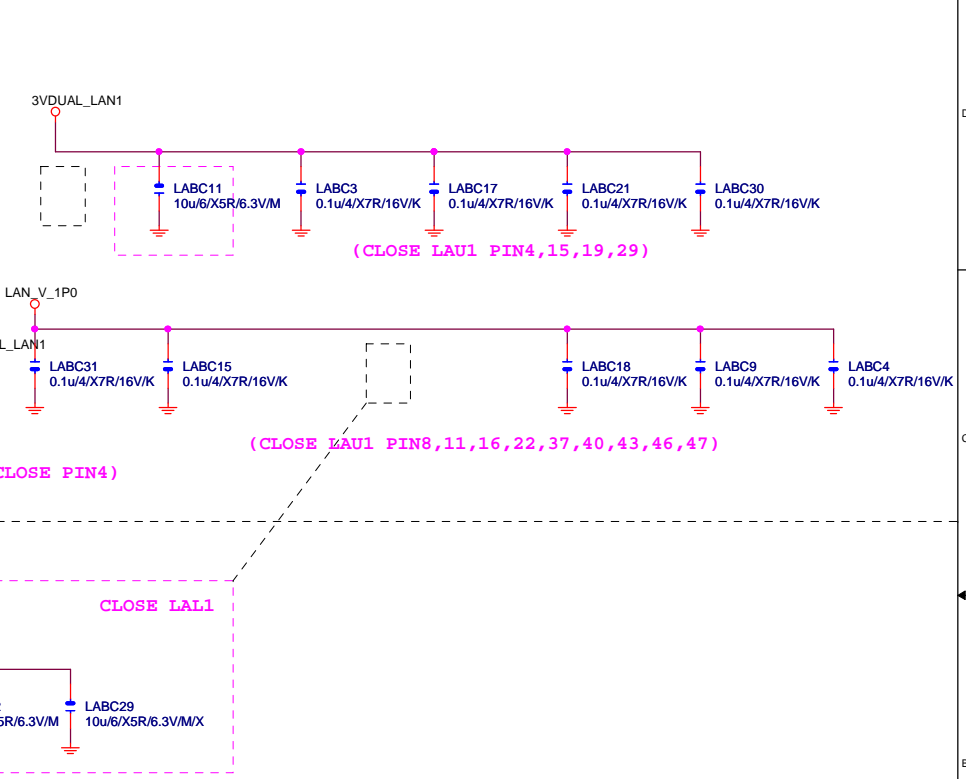
L1+CLK REQ# 節能:  
需對應LA\_SRCLK\_LAN之CLKREQ#



PCH端:  
電阻上

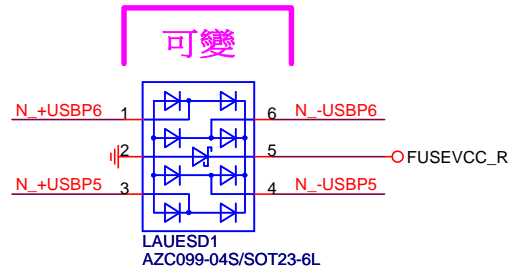


For當ErP enable後，挑PSU會無法LAN Wake-up



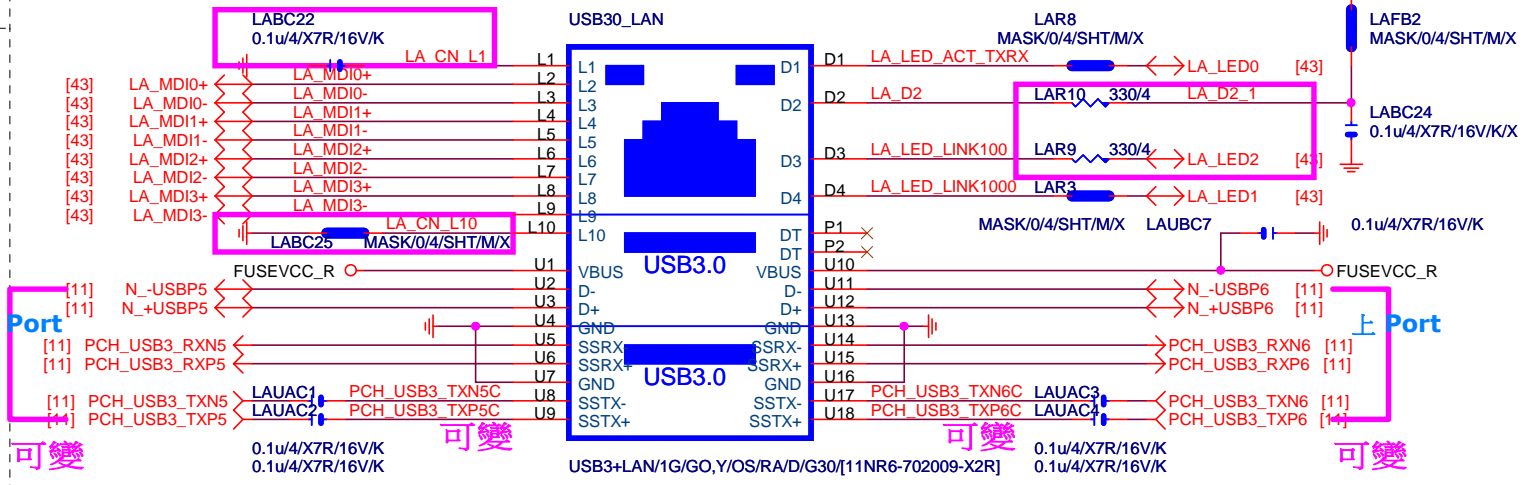
**USB\_LAN CONNECTOR** R1.11

**RMA ESD PROTECT** note:可變更USB NAME



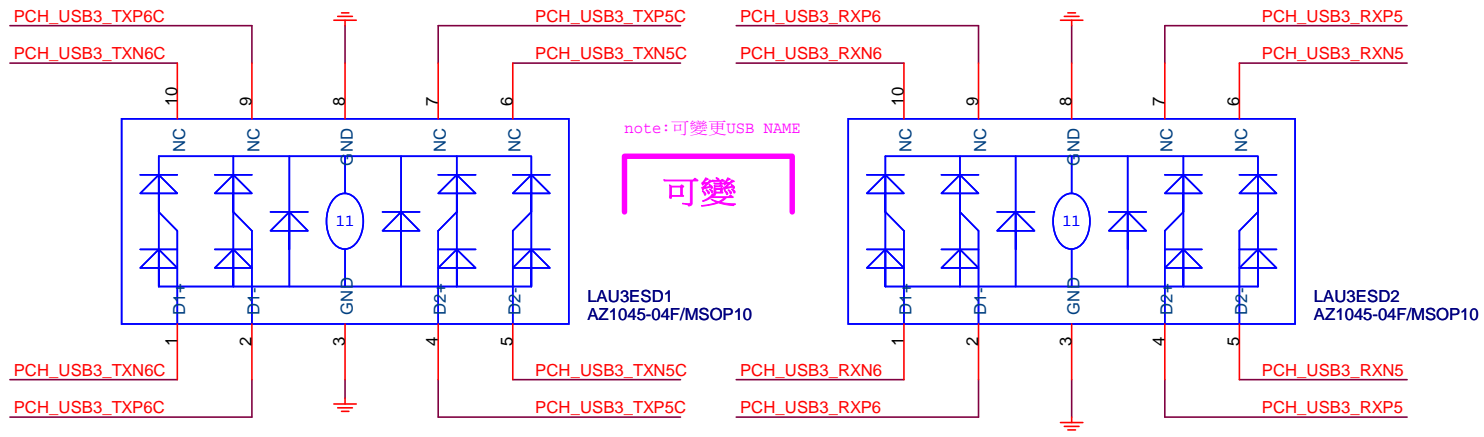
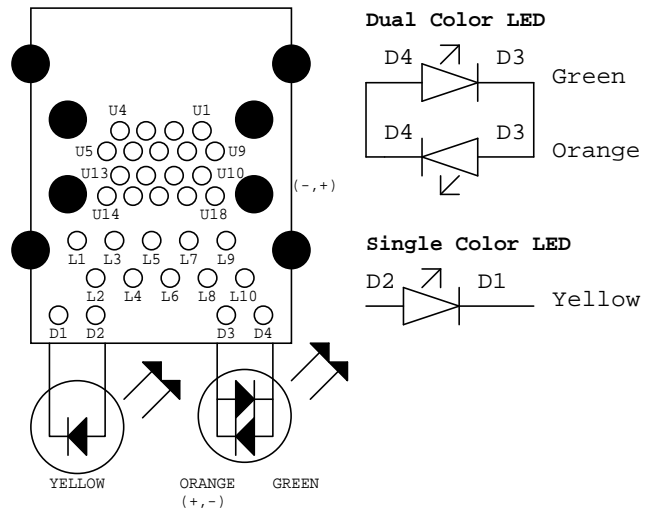
**USB\_LAN CONNECTOR** note:可變更USB NAME

**[I219]**



**LA\_MDI-->100歐姆:[20/4/8/4/20]**

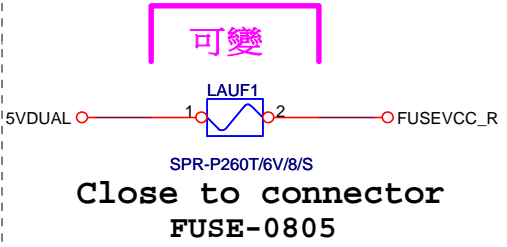
**USB30 LAN LAYOUT示意圖**



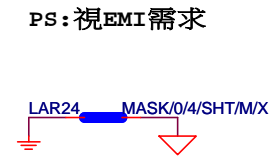
**LAN\_COVER** FOOT PRINT:LAN\_COVER

可變 \*Del USB\_LAN\_HS [視SPEC需求]

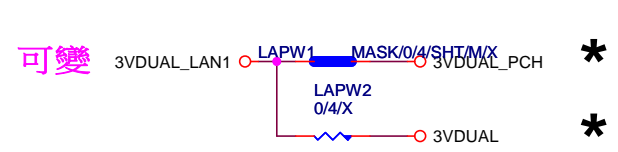
**USB POWER** note:可變更FUSE



**EMI SHORT PAD**

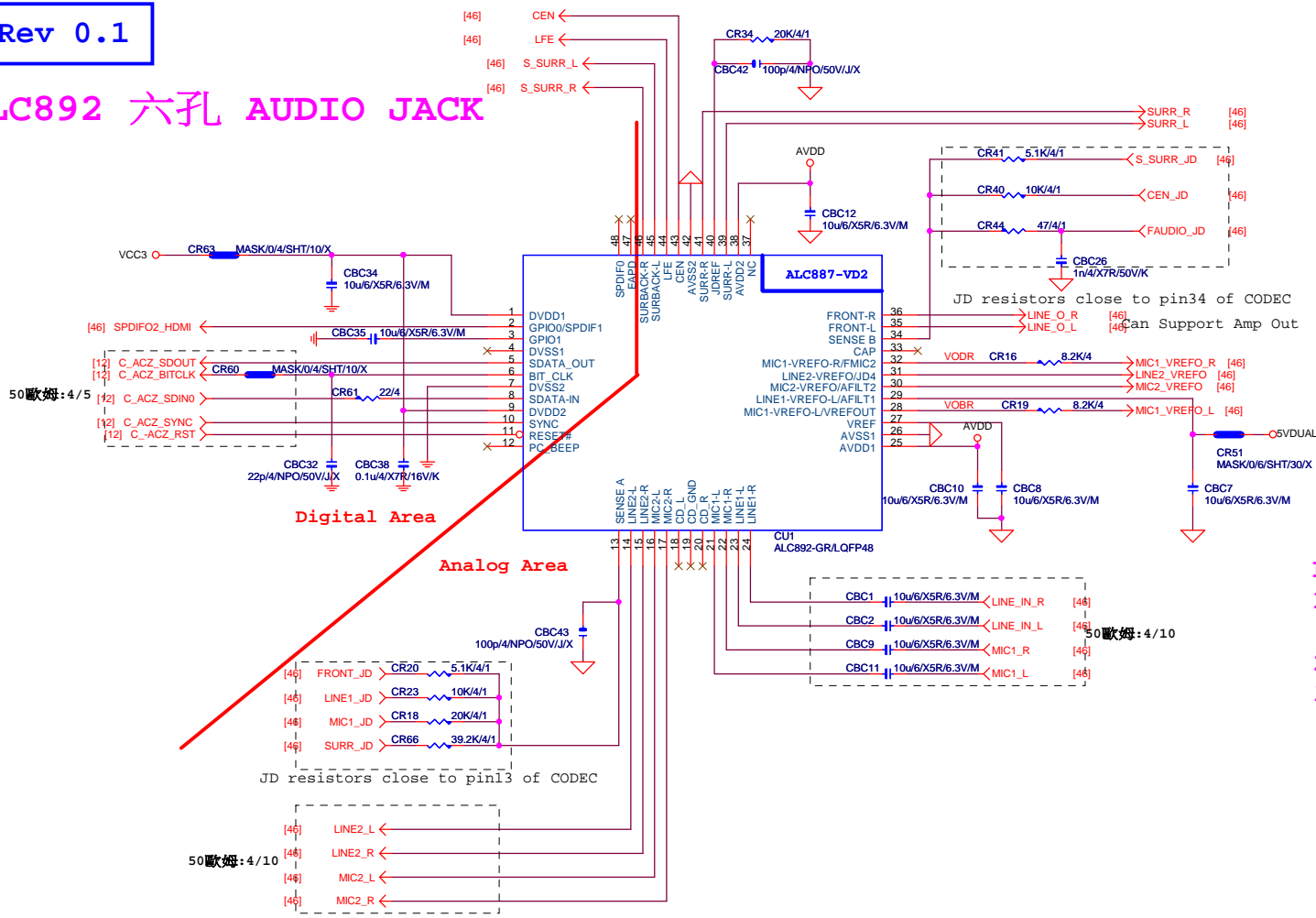


**LAN POWER** note: lan power連接及電流



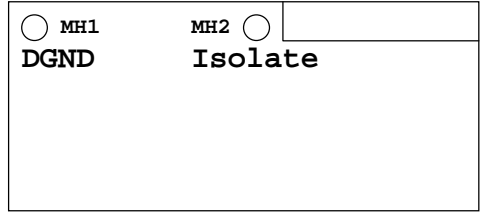
**Gigabyte Technology**  
**LAN CONNECTOR-I219**  
 Title  
 Size Custom Document Number  
**GA-Z270M-D3P**  
 Date: Monday, December 19, 2016 Sheet 44 of 55  
 Rev 1.01

# ALC892 六孔 AUDIO JACK



**LAYOUT注意: 螺絲孔下GND方式**

- MH1空間夠, 下DGND  
空間不夠, 才改為Isolate
- MH2一律改為Isolate
- Codec下方, 第二層必須參考GND



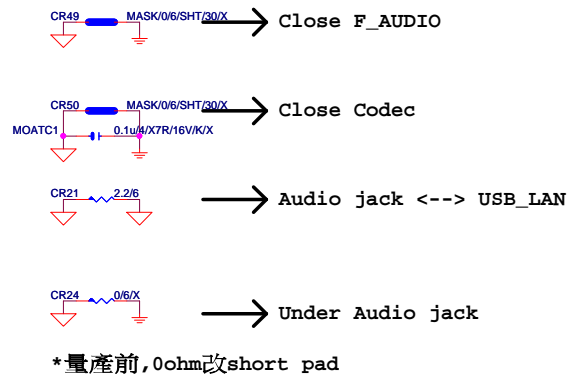
\*Del AUDIO\_HS

\*料號後補

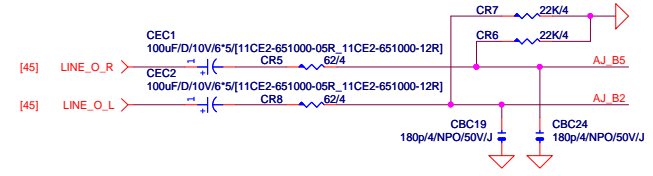
**BOM OPTION :**

- Chemicon 音效電容
- 金屬外罩 Reserve (LAYOUT上件與否, 依照各Model spec)
- LED Reserve (上件與否和LED顏色, 依照各Model spec)

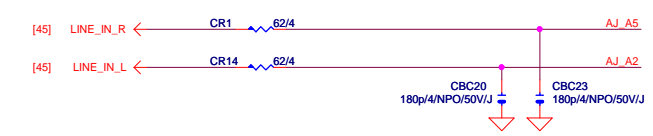
<b>Gigabyte Technology</b>		
<b>HD AUDIO ALC892</b>		
Size Custom	Document Number <b>GA-Z270M-D3P</b>	Rev <b>1.01</b>
Date: Monday, December 19, 2016	Sheet 45 of 55	



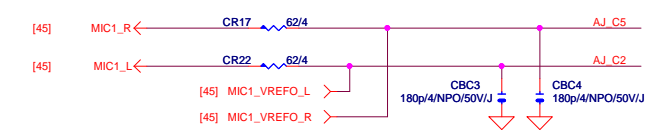
LINE-OUT



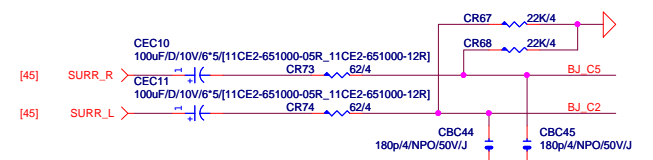
LINE-IN



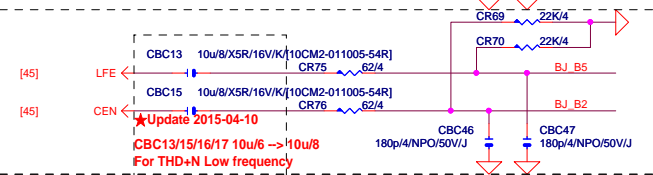
MIC-IN



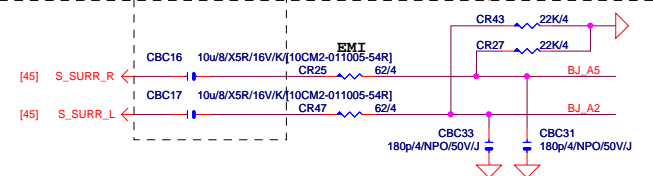
SURROUND



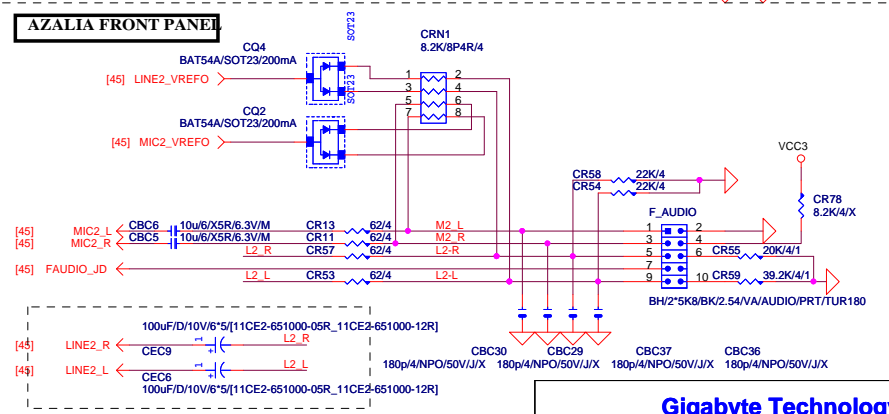
CEN/LFE



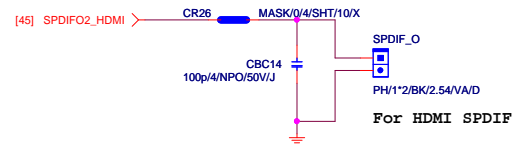
SURR BACK



AZALIA FRONT PANEL

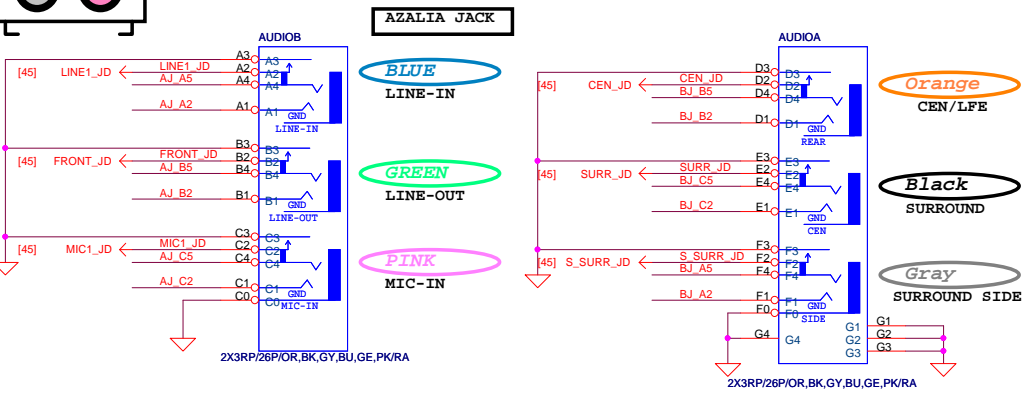
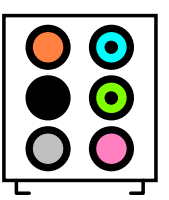


SPDIF\_OUT

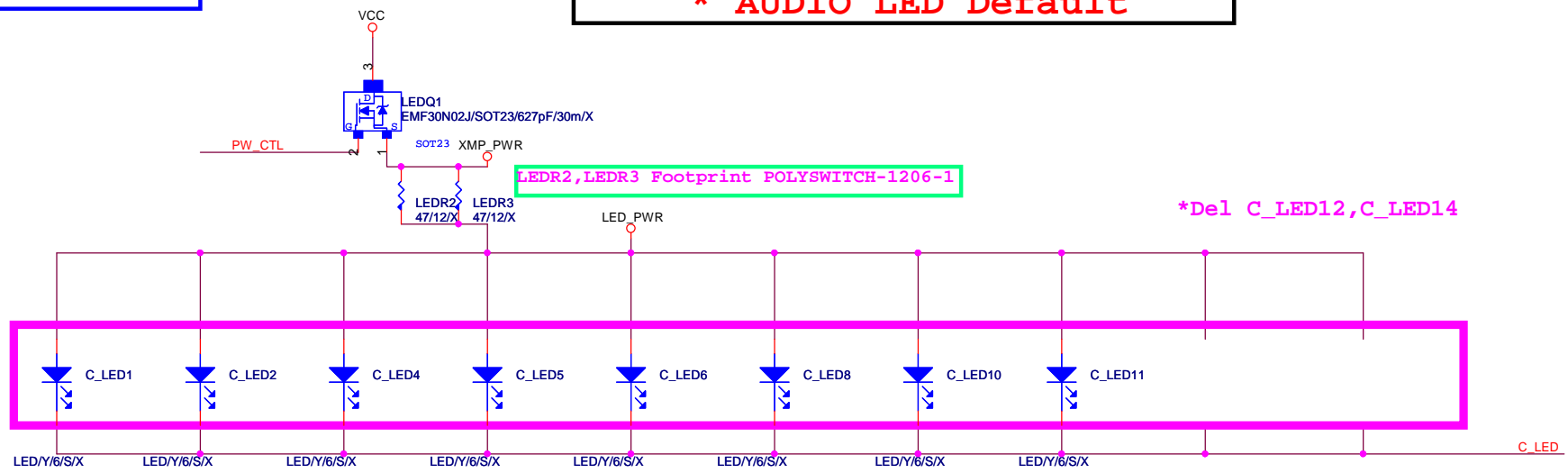


SPDIF\_IN

AZALIA JACK



**\* AUDIO LED Default**



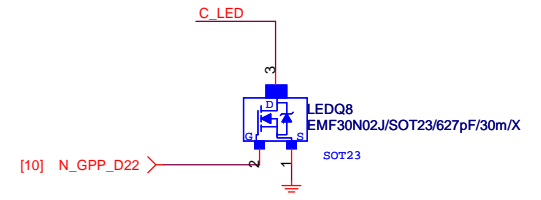
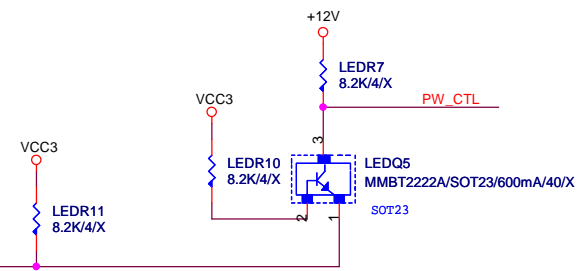
LEDR2,LEDR3 Footprint POLYSWITCH-1206-1

\*Del C\_LED12,C\_LED14

**Ambient LED Control**

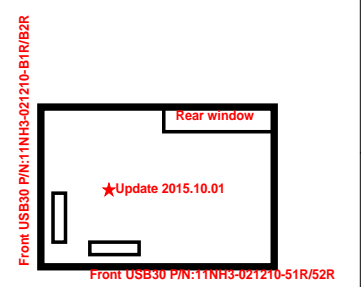
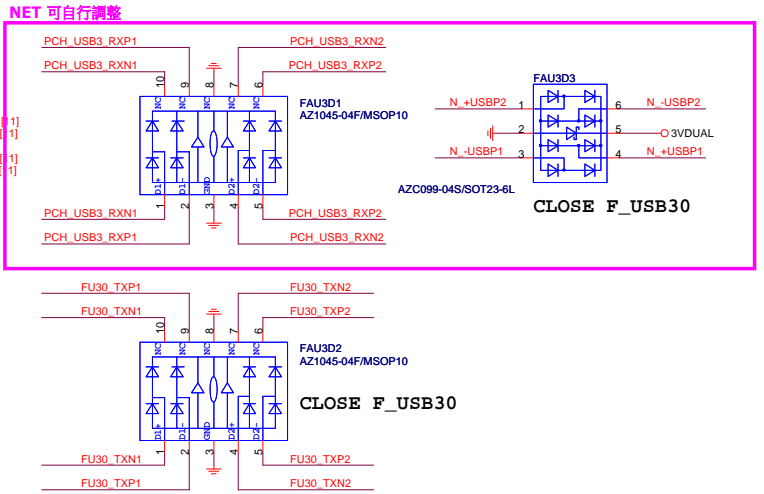
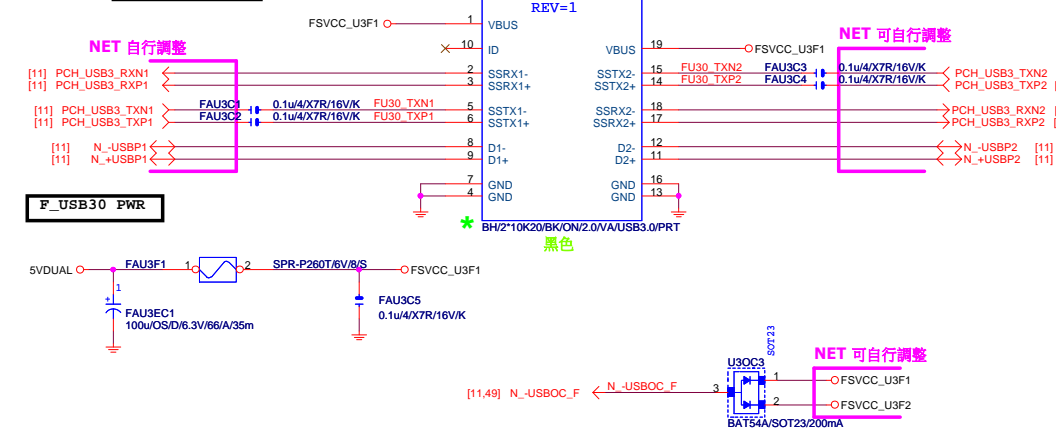
	N_GPP_D22
Full Mode	H
OFF Mode	L

[10] N\_GPP\_D22  
ON/OFF



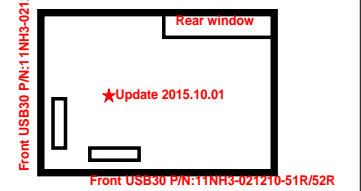
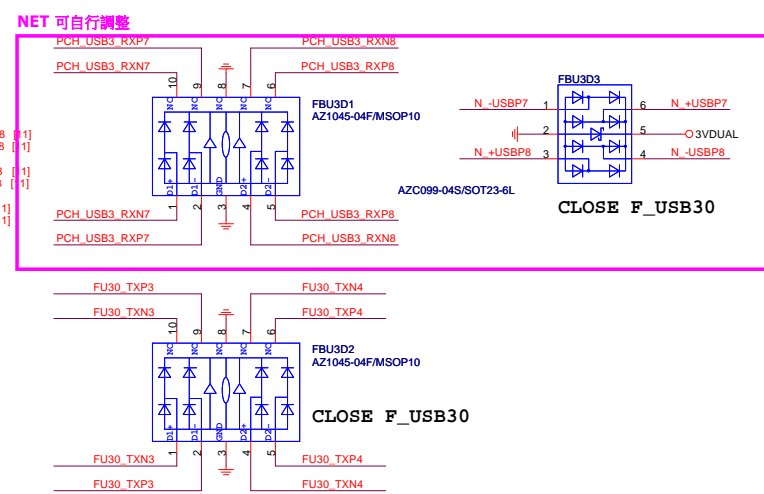
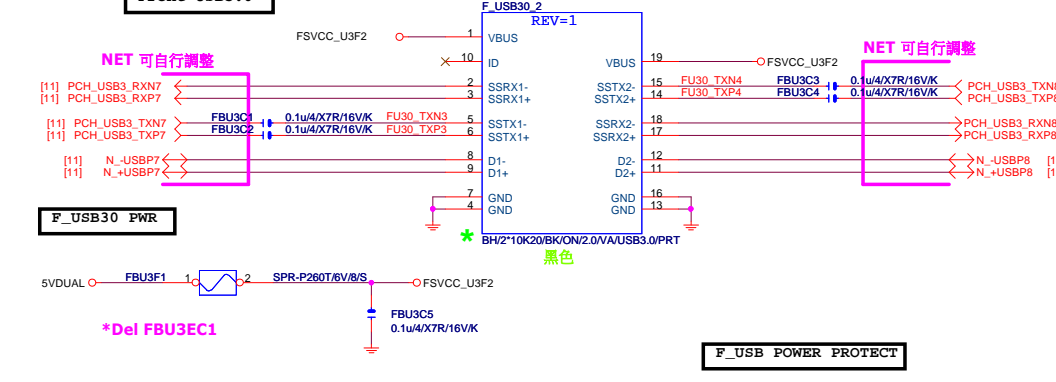


Front USB3.0



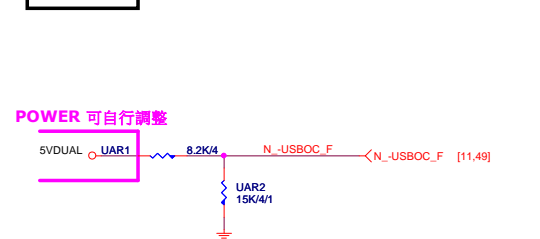
Front USB30 P/N:11NH3-021210-51R/B2R

Front USB3.0

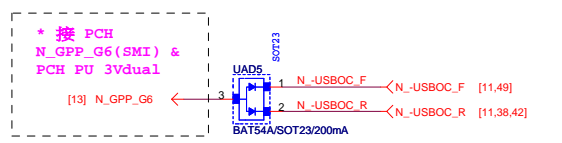
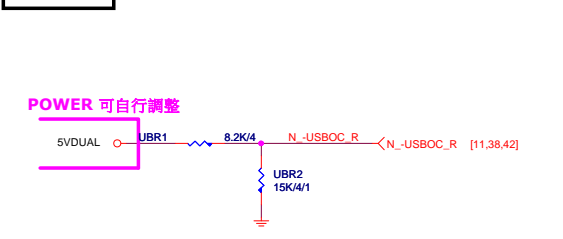


Front USB30 P/N:11NH3-021210-51R/B2R

-USBOC\_F



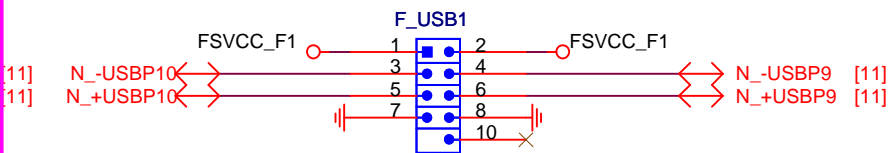
-USBOC\_R



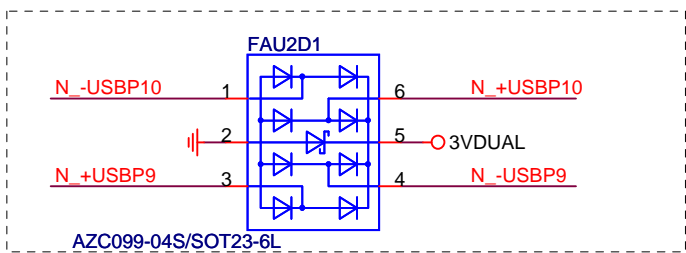
<b>Gigabyte Technology</b>		
Title <b>R_USB30,F_USB30, USB_OC</b>		
Size Custom	Document Number <b>GA-Z270M-D3P</b>	Rev <b>1.01</b>
Date: Monday, December 19, 2016	Sheet 48	of 55

NET 可變

FUSB2X5-HS

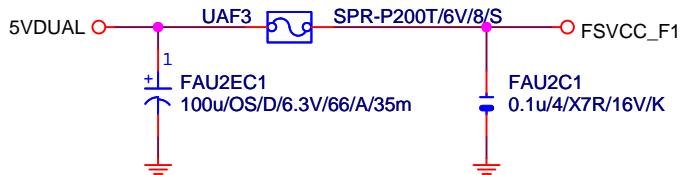


BH/2\*5K9/BK/ON/2.54/VA/USB/PRT/TUR180



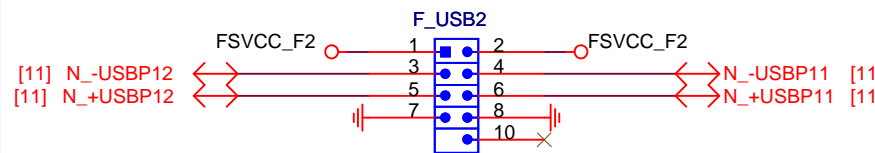
Close to connector

FUSE 2 Port 1 Fuse 2A

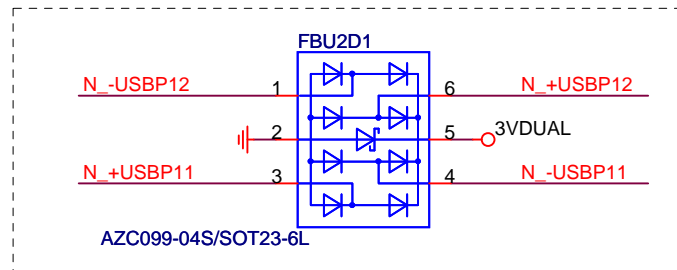


NET 可變

FUSB2X5-HS

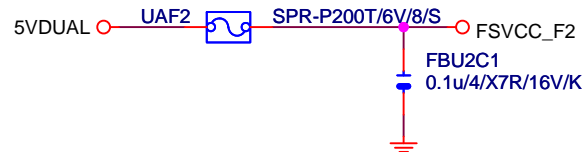


BH/2\*5K9/BK/ON/2.54/VA/USB/PRT/TUR180

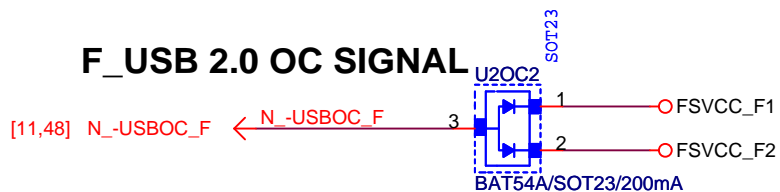


Close to connector

FUSE 2 Port 1 Fuse 2A



F\_USB 2.0 OC SIGNAL

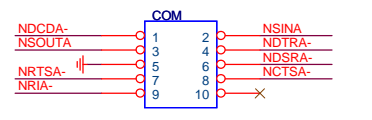
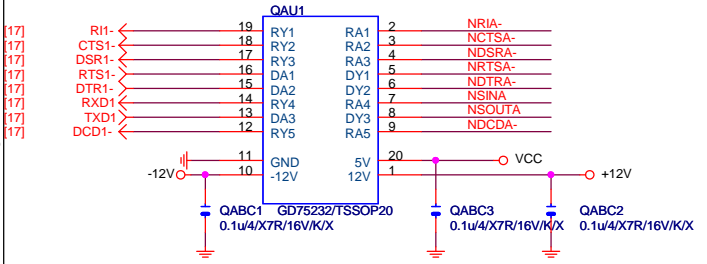


Gigabyte Technology

Title		
<b>USB2.0</b>		
Size A	Document Number	Rev
	<b>GA-Z270M-D3P</b>	<b>1.01</b>
Date:	Monday, December 19, 2016	Sheet 49 of 55

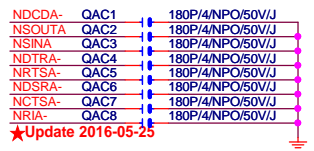
COM PORT **Rev: 0.82**

COM RI N/A

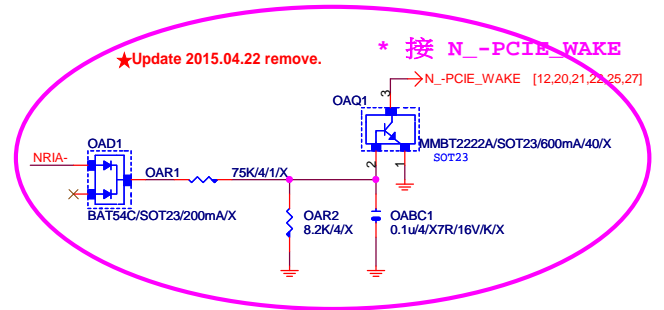


BH/2\*5K10/BK/2.54/VA/COMPRT/TUR180

F\_COM-HS



★Update 2016-05-25



★Update 2015.04.22 remove.

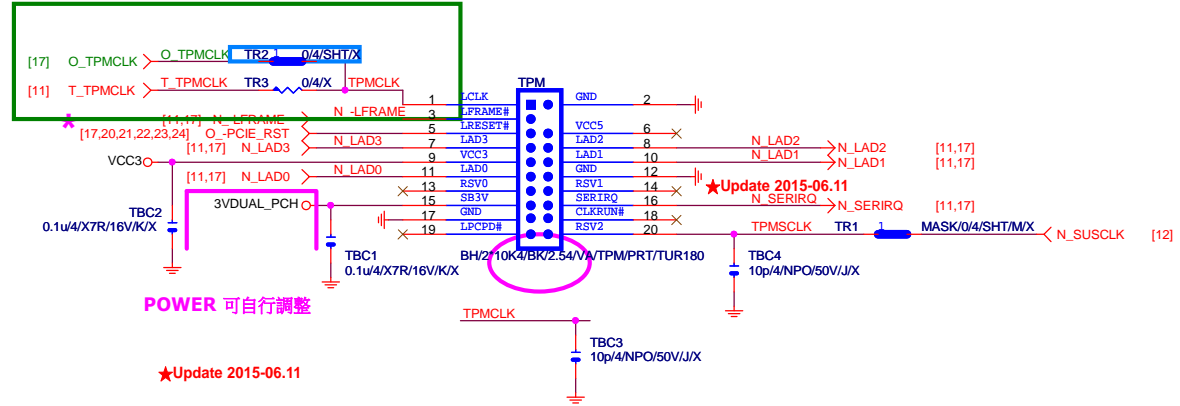
\* 接 N-PCIE\_WAKE

LPT PORT

TPM CONNECT

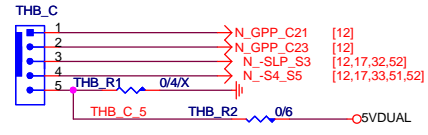
Thunderbolt

★Update 2015-12-29



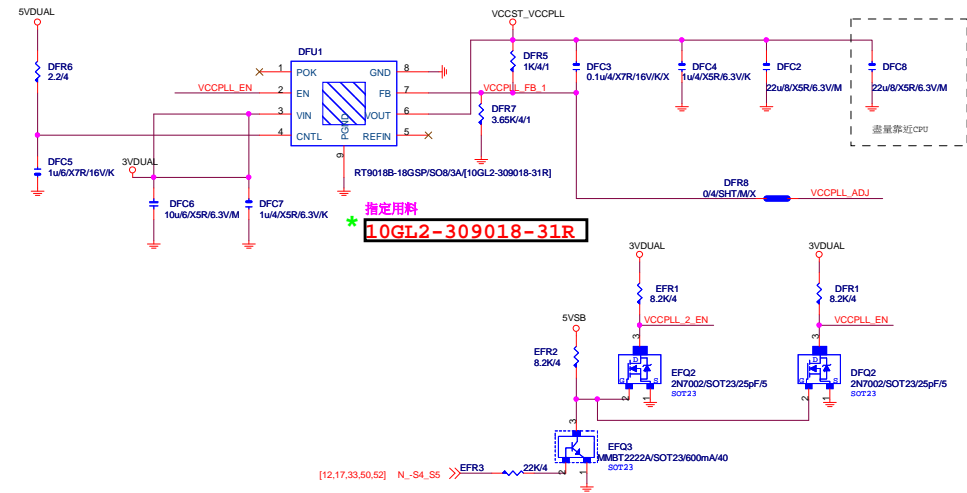
POWER 可自行調整

★Update 2015-06-11

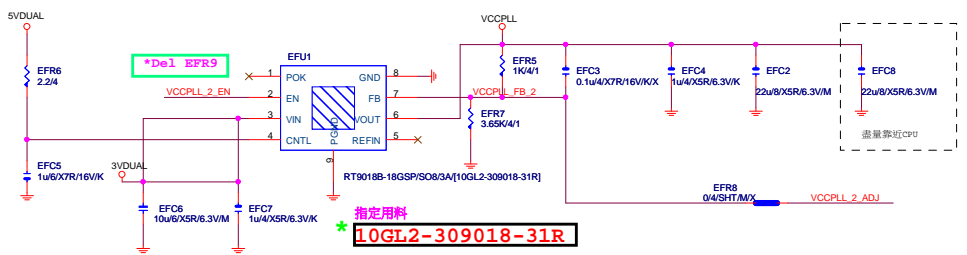


PH/1\*5/BK/2.54/VA/D/[11NH5-040105-41R]  
Footprint update "WAFER-1X5P"

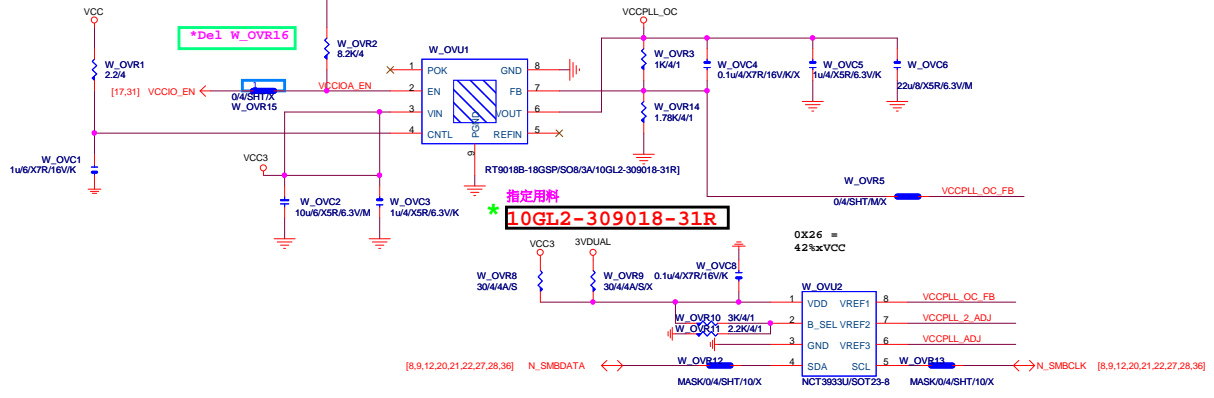
VCCST\_VCCPLL 替換原先MOS開關線路



VCCPLL



VCCPLL\_OC



### CLOSE SIO

EMIC1  
100p/4/NPO/50V/J/X

[12,17,32,50] N\_SLP\_S3 ←

EMIC2  
100p/4/NPO/50V/J/X

[12,17,33,50,51] N\_S4\_S5 ←

**\*Del EMIC3**

### CLOSE PCH

EMIC4  
100p/4/NPO/50V/J/X

[4,12] N\_CPUPWROK ←

VCC3

EMIC5

1n/4/X7R/50V/K

# GIGABYTE™

Title

**EMI/ESD**

Size  
A

Document Number

**GA-Z270M-D3P**

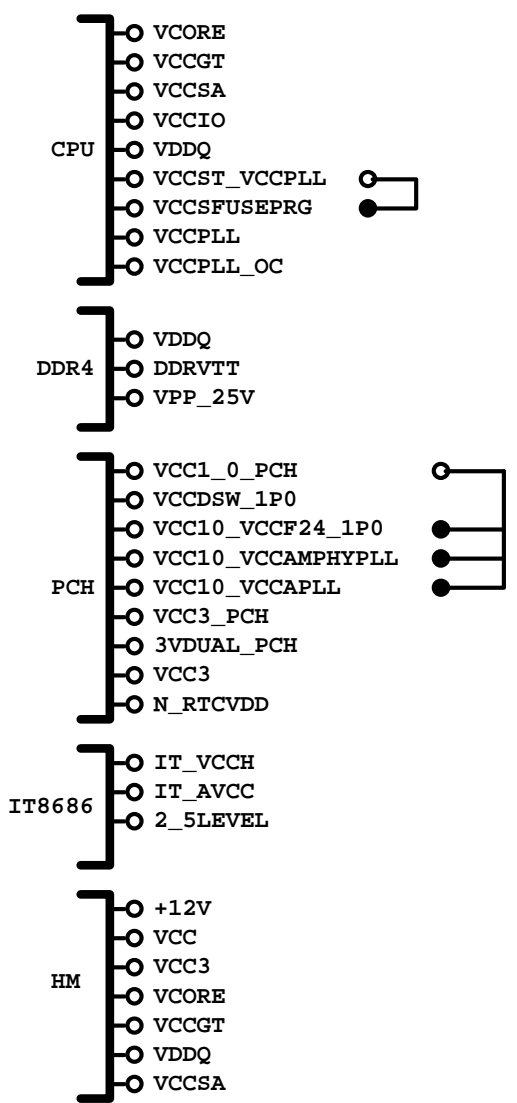
Rev

**1.01**

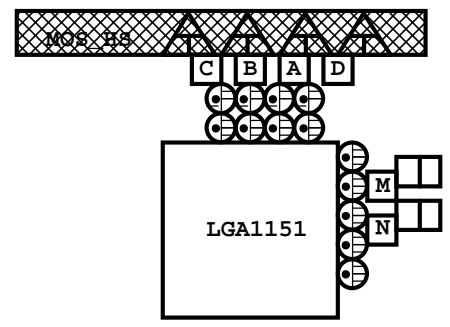
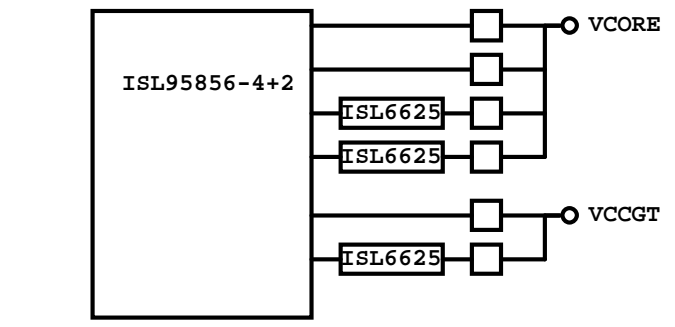
Date: **Monday, December 19, 2016**

Sheet **52** of **55**

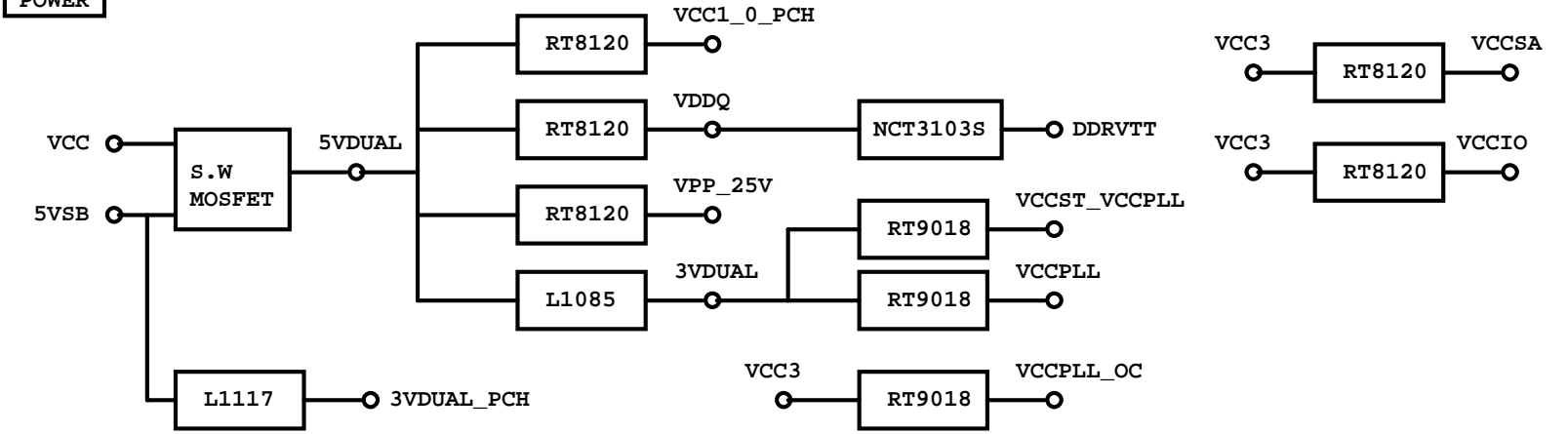
**POWER BLOCK MAP**



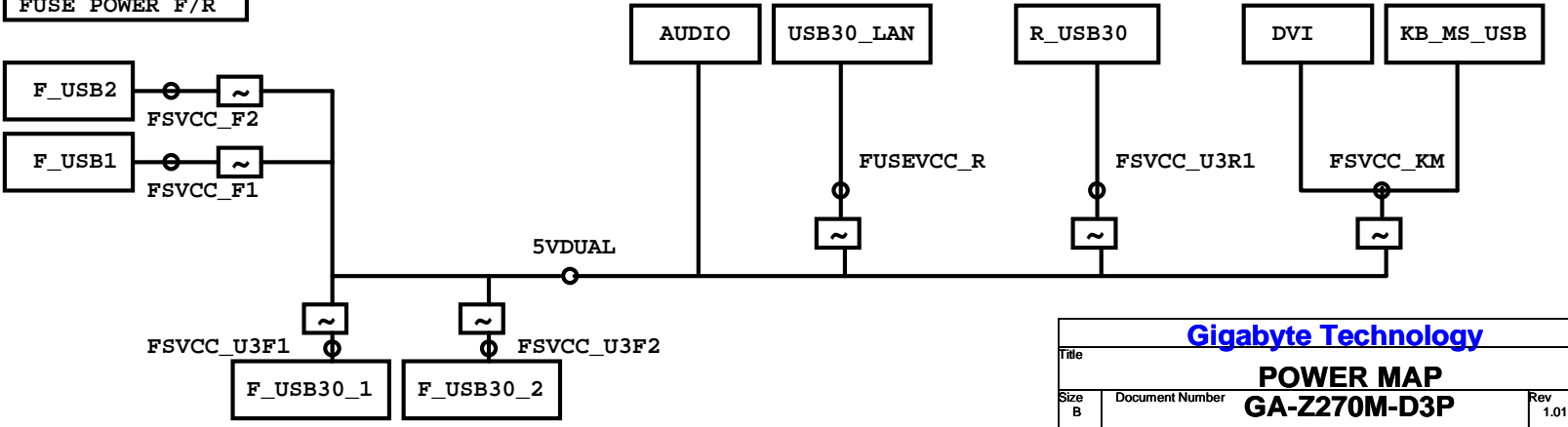
**VCORE/VCCGT**



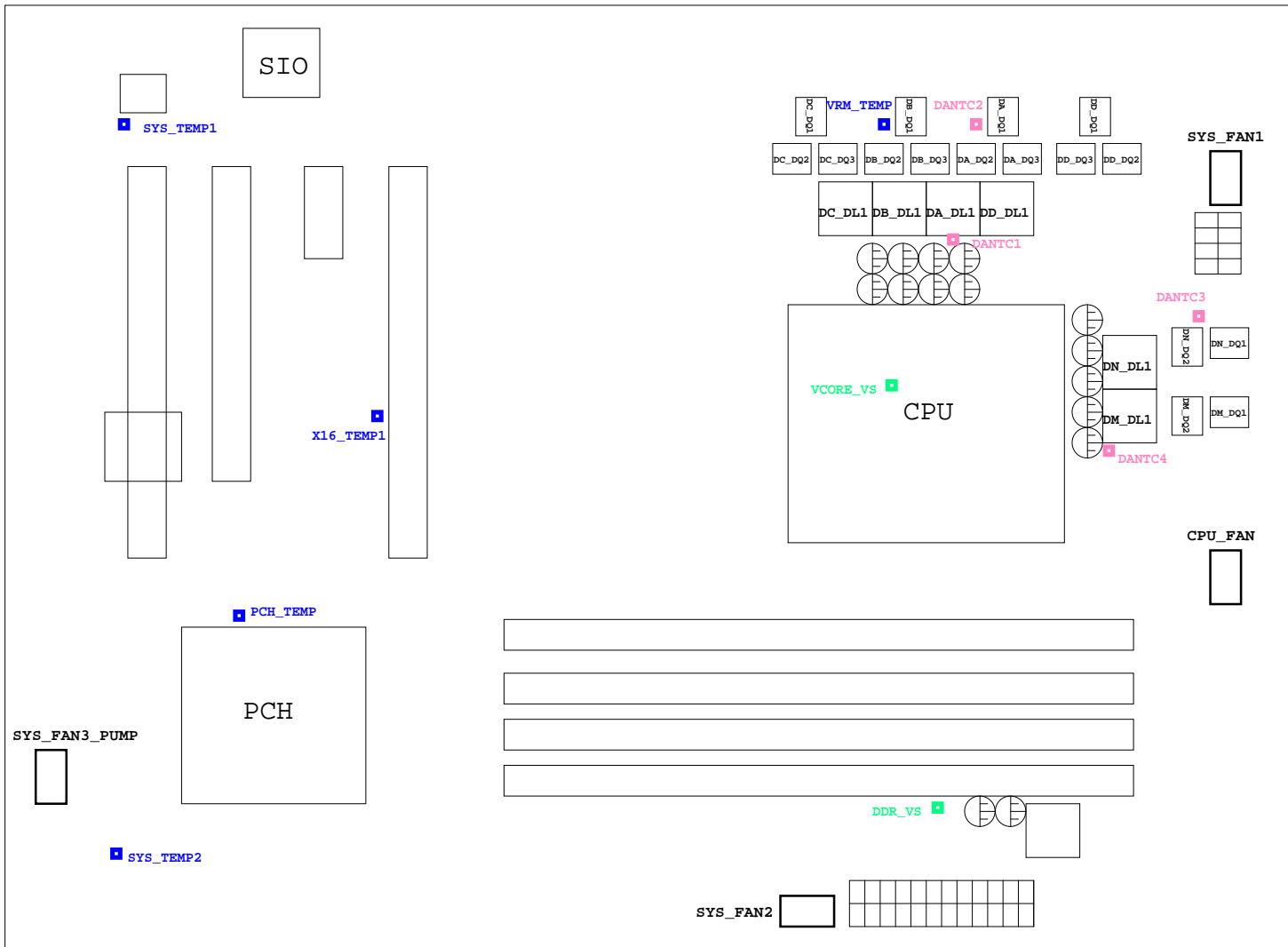
**POWER**



**FUSE POWER F/R**



<b>Gigabyte Technology</b>		
Title		
<b>POWER MAP</b>		
Size	Document Number	Rev
B	<b>GA-Z270M-D3P</b>	1.01
Date:	Monday, December 19, 2016	Sheet 53 of 55



熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL1	N/A
DANTC2	DA_DQ1	Differential
DANTC3	DM_DQ2	N/A
DANTC4	DM_DL1	Differential
VCORE_TEMP	DB_DQ1	N/A
X16_TEMP1	PCIEX16	N/A
PCH_TEMP	PCH	N/A
SYS_TEMP1	CU1	N/A
SYS_TEMP2	N/A	N/A





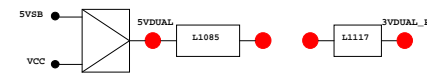
**PCH GPIO LIST TABLE**

PIN NAME	FWR	Default	USAGS	NOTE
GFP_A0	MAIN	H-Z	N_KBRST	F/U 8.2K VCC3
GFP_A1	MAIN	H-Z	N_LAD0	N/A
GFP_A2	MAIN	H-Z	N_LAD1	N/A
GFP_A3	MAIN	H-Z	N_LAD2	N/A
GFP_A4	MAIN	H-Z	N_LAD3	N/A
GFP_A5	MAIN	H-Z	N_LFRAME	N/A
GFP_A6	MAIN	H-Z	N_SERIRQ	F/U 8.2K VCC3
GFP_A7	MAIN	H-Z	N_LDRQ0	F/U 8.2K VCC3
GFP_A8	MAIN	H-Z	N_GFP_A8	F/U 8.2K VCC3
GFP_A9	MAIN	H-Z	N_TFMCCLK/N_LPC24M	N/A
GFP_A11	MAIN	H-Z	N_P_PME	F/U 8.2K 3VDUAL_PCH
GFP_A12	MAIN	H-Z	N_GFP_A12	F/U 8.2K VCC3
GFP_A13	MAIN	H-Z	N_S_WARN	N/A
GFP_A14	MAIN	H-Z	N_GFP_A14	F/U 8.2K 3VDUAL
GFP_A15	MAIN	H-Z	N_S_ACK	N/A
GFP_B0	MAIN	H-Z	N_DDR_V_SEL	F/U 8.2K VCC3
GFP_B2	MAIN	H-Z	N_VHALERT	F/U 8.2K 3VDUAL
GFP_B3	MAIN	H-Z	N_GFP_B3	N/A
GFP_B4	MAIN	H-Z	N_GFP_B4	N/A
GFP_B5	MAIN	H-Z	N_PCIE16_PR	F/U 8.2K VCC3
GFP_B6	MAIN	H-Z	N_PCIEK1_PK1	F/U 8.2K VCC3
GFP_B8	MAIN	H-Z	N_PCIEK4_PK	F/U 8.2K VCC3
GFP_B9	MAIN	H-Z	N_GFP_B9	F/D GND
GFP_B10	MAIN	H-Z	N_LA_CLKREQ	F/U 8.2K 3VDUAL LAN1
GFP_B12	MAIN	H-Z	N_SLP_S0	N/A
GFP_B13	MAIN	H-Z	N_PMRST	N/A
GFP_B14	MAIN	H-Z	N_SPKR	N/A
GFP_B15	MAIN	H-Z	N_GFP_B15	N/A
GFP_B16	MAIN	H-Z	N_GFP_B16	N/A
GFP_B22	MAIN	H-Z	N_GFP_B22	F/D 1K GND
GFP_B43	MAIN	H-Z	N_PCH_HOT	N/A
GFP_C0	MAIN	H-Z	N_SMBCLK	F/U 1K 3VDUAL
GFP_C1	MAIN	H-Z	N_SMBDATA	F/U 1K 3VDUAL
GFP_C2	MAIN	H-Z	N_LPCPME	N/A
GFP_C3	MAIN	H-Z	N_SMLCLK	F/U 499 3VDUAL
GFP_C4	MAIN	H-Z	N_SMLDAT	F/U 499 3VDUAL
GFP_C5	MAIN	H-Z	N_GFP_C5	N/A
GFP_C6	MAIN	H-Z	N_SMLCLK	F/U 8.2K 3VDUAL
GFP_C7	MAIN	H-Z	N_SMLDAT	F/U 8.2K 3VDUAL
GFP_C22	MAIN	H-Z	N/A	N/A
GFP_C33	MAIN	H-Z	N_GFP_C33	N/A
GFP_D4	MAIN	H-Z	N_GFP_D4	F/U 8.2K 3VDUAL
GFP_D7	MAIN	H-Z	N_GFP_D7	N/A
GFP_D8	MAIN	H-Z	N_GFP_D8	N/A
GFP_D9	MAIN	H-Z	N_GFP_D9	F/U 1K VCC3
GFP_D10	MAIN	H-Z	N_GFP_D10	N/A
GFP_D13	MAIN	H-Z	N_GFP_D13	N/A
GFP_D33	MAIN	H-Z	N/A	N/A
GFP_E0	MAIN	H-Z	N_GFP_E0	F/U 8.2K 3VDUAL
GFP_E1	MAIN	H-Z	N_GFP_E1	F/U 8.2K 3VDUAL
GFP_E2	MAIN	H-Z	N_GFP_E2	F/U 8.2K 3VDUAL
GFP_E3	MAIN	H-Z	N/A	N/A
GFP_E4	MAIN	H-Z	N_DEVSLP0	N/A
GFP_E6	MAIN	H-Z	N_GFP_E6	N/A
GFP_E8	MAIN	H-Z	N_SATALED	N/A
GFP_E9	MAIN	H-Z	N_USBOC_F	N/A
GFP_E10	MAIN	H-Z	N_USBOC_R	N/A
GFP_E11	MAIN	H-Z	N_USBOC_R	N/A
GFP_E12	MAIN	H-Z	N_USBOC_F	N/A
GFP_F0	MAIN	H-Z	N_GFP_F0	F/U 8.2K 3VDUAL
GFP_F1	MAIN	H-Z	N_GFP_F1	F/U 8.2K 3VDUAL
GFP_F2	MAIN	H-Z	N_GFP_F2	F/U 8.2K 3VDUAL
GFP_F3	MAIN	H-Z	N_GFP_F3	F/U 8.2K 3VDUAL
GFP_F4	MAIN	H-Z	N_GFP_F4	F/U 8.2K 3VDUAL
GFP_F5	MAIN	H-Z	N_GFP_F5	F/U 8.2K VCC3
GFP_F6	MAIN	H-Z	N_DEVSLP4	N/A
GFP_F10	MAIN	H-Z	N_GFP_F10	F/U 8.2K VCC3
GFP_F11	MAIN	H-Z	N_GFP_F11	F/U 8.2K VCC3
GFP_F12	MAIN	H-Z	N_GFP_F12	F/U 8.2K VCC3
GFP_F13	MAIN	H-Z	N_GFP_F13	F/U 8.2K VCC3
GFP_F14	MAIN	H-Z	N_SKT0CC	F/U 8.2K VCC3
GFP_F15	MAIN	H-Z	N_USBOC_F	N/A
GFP_F16	MAIN	H-Z	N_USBOC_F	N/A
GFP_F17	MAIN	H-Z	N_USBOC_R	N/A
GFP_F18	MAIN	H-Z	N_USBOC_7	F/U 8.2K 3VDUAL
GFP_F22	MAIN	H-Z	N_GFP_F22	F/U 8.2K VCC3
GFP_F23	MAIN	H-Z	N_GFP_F23	F/U 8.2K VCC3
GFP_G11	MAIN	H-Z	N_GFP_G11	N/A
GFP_G12	MAIN	H-Z	N_GFP_G12	N/A
GFP_G13	MAIN	H-Z	N_CPU_S1	N/A
GFP_G14	MAIN	H-Z	N_GT_S	N/A
GFP_G15	MAIN	H-Z	N_CPU_S	N/A
GFP_G18	MAIN	H-Z	N_GFP_G18	F/U 8.2K VCC3
GFP_G19	MAIN	H-Z	N_GFP_G19	F/U 8.2K VCC3
GFP_G20	MAIN	H-Z	N_GFP_G20	F/U 8.2K VCC3
GFP_G21	MAIN	H-Z	N_GFP_G21	F/U 8.2K VCC3
GFP_G22	MAIN	H-Z	N_GFP_G22	F/U 8.2K VCC3
GFP_H0	MAIN	H-Z	N2A_CLKREQ	F/U 8.2K VCC3
GFP_H12	MAIN	H-Z	N_GFP_H12	N/A
GFP_H19	MAIN	H-Z	N_GFP_H19	F/U 8.2K 3VDUAL
GFP_H20	MAIN	H-Z	N_GFP_H20	F/U 8.2K 3VDUAL
GFP_H21	MAIN	H-Z	N_GFP_H21	F/U 8.2K 3VDUAL
GFP_H22	MAIN	H-Z	N_GFP_H22	F/U 8.2K 3VDUAL
GFP_I0	MAIN	H-Z	N_DP_HDP	N/A
GFP_I1	MAIN	H-Z	N_DP2_HDP	N/A
GFP_I2	MAIN	H-Z	N_DVI_HDP_F	F/U 1M VCC3

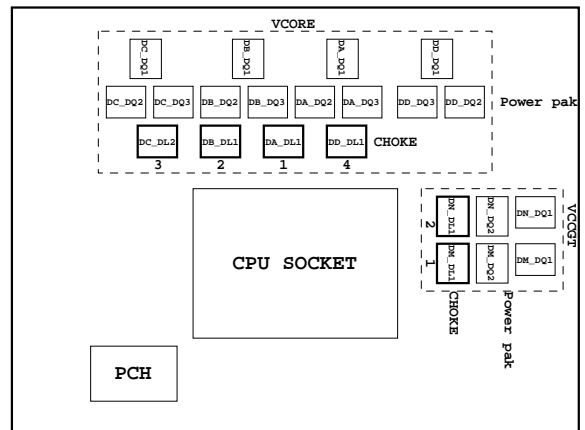
PIN NAME	FWR	Default	USAGS	NOTE
GFP_I3	MAIN	H-Z	N_GFP_I3	F/U 8.2K VCC3
GFP_I4	MAIN	H-Z	N_GFP_I4	F/U 100K GND
GFP_I5	MAIN	H-Z	N_DDBP_CTRLCLK	F/U 2.2K VCC3
GFP_I6	MAIN	H-Z	N_DDBP_CTRLDATA	F/U 2.2K VCC3
GFP_I7	MAIN	H-Z	N_DDBP_CTRLCLK	F/U 2.2K VCC3
GFP_I8	MAIN	H-Z	N_DDBP_CTRLDATA	F/U 2.2K VCC3
GFP_I9	MAIN	H-Z	N_DDBP_CTRLCLK	F/U 2.2K VCC3
GFP_I10	MAIN	H-Z	N_DDBP_CTRLDATA	F/U 2.2K VCC3
GPD0	STBY	BATLOW	N_BATLOW	F/U 8.2K 3VDUAL_PCH
GPD1	STBY	ADPRESSET	N_GP_D1	F/U 8.2K 3VDUAL_PCH
GPD2	STBY	LAN_WAKE	N_LAN_WAKE	F/U 8.2K 3VDUAL_PCH
GPD3	STBY	PWRBTN	O_PWRBTN	F/U 8.2K 3VDUAL_PCH
GPD4	STBY	SLP_S3	N_SLP_S3	N/A
GPD5	STBY	SLP_S4	N_S4_S5	N/A
GPD6	STBY	SLP_A	N_SLP_A	N/A
GPD8	STBY	SUSCLK	N_SUSCLK	F/D 1.5K GND
GPD10	STBY	SLP_S5	N_SLP_S5	N/A
GPD11	STBY	LAMPHYPC	N_LAN_DIS	N/A

**Super I/O ITR8686 GPIO Table**

PIN NAME	USAGS	NOTE
PCIRST3#/GP10/VDIMM_STR_EN	N/A	
PCIRST2#/GP11	O_PCIE_RST	
PCIRST1#/GP12	O_PPWRST2	
SVC/PECI_RQT/GP14	N_THERMTRIP	
SLP_SUS#/PCIRSTIN#/CIRT2/GP15	-PCIRSTIN	
PS1_L/FAN_CLT5/CIRK2/GP16	PCIN	
RI2#/GP17	IO_GP17	
THR_PWM_CTS2#/GP20	PCIN	
IO_SMI#DCD2#/GP21	PCIN	
SP1_S1/GP22	PCIN	
DPWROR/GPU_PG/GP23	N_PCH_DPWROR	
FAN_TAC5/RTS2#/GP24	PCIN	
FAN_TAC4/DSR2#/GP25	FANIO4	
MB_ID2	MB_ID2	
INV_IN1/SIN2/GP27	BEEP-	
ATXPG/GP30	PWOK	
CTS1	CTS1-	
OCMDT3/RI1#/GP32	RI1-	
OCMDT2/DCD1#/GP33	DCD1-	
VTT_PWRGD/GP34	VTT_PWRGD	
VCC18_EN/GP35	VCCIO_EN	
FAN_CTL3/GP36	FANPWM3	
FAN_TAC3/GP37	FANIO3	
3VSB5W#/GP40	PCIN	
OCMDT1/SIN1/GP41	RXD1	
GP42/SCK/FAN_CTL4	FANPWM4	
FAN5W#/GP43	-PPWRSTW	
PWRON#/GP44	O_PPWRSTW	
OCMDT0/DSR1#/GP45	DSR1-	
CE2_N/GP47/JP6	CEB_N	
GP50/JP1	O_TFMCCLK	
FAN_CTL2/GP51	FANPWM2	
FAN_TAC2/GP52	FANIO2	
SUSCH#/GP53	N_S4_S5	
PME#/GP54	N_LPCPME	
RSRST#/CIRKX1/GP55	O_RSRST	
MCLK/FAN_TAC6/GP56	MCLK	
MDAT/FAN_CTL6/GP57	MDAT	
KCLK/GP60	KCLK	
KDAT/GP61	KDAT	
KRST#/GP62	N_KBRST	
HOLD_B#/GP63	PCIN	
HOLD_S#/GP64	-SPI_HOLD_N	
VLDI_EN/PCH_D0/GP65	PCIN	
VCC1_05_EN/GP66	VCC1_0_EN	
GP67	N_RTCRST	
USB_F81/PD0/GP70	PCIN	
USB_F82/PD1/GP71	PCIN	
USB_F83/PD2/GP72	PCIN	
USB_F83/PD3/GP73	PCIN	
USB_F85/PD4/GP74	PCIN	
USB_F86/PD5/GP75	PCIN	
USB_F87/PD7/GP76	PCIN	
USB_F88/PD8/GP77	PCIN	
LS_IN1/SLCT/GP80	VDDQ	
LS_OUT1/PE/GP81	PCIN	
LS_IN2/BSUY/GP82	VCCIO	
LS_OUT2/ACK#/GP83	VCCIO	
IPHONE_CHARGE#/SLIN#/GP84	PCIN	
OC_IN/INIT#/GP85	PCIN	
OC_OUT/AFD#/GP86	PCIN	
USB_OC2/STB#/GP87	PCIN	
DDR_EN/GP90	MA_EN	
PWRLED/GP91	MFD-	
HOLD_OUT/GP92	PCIN	
HDLED_IN/GP93	IO_GP93	
PROCHOT#/GP94	A_PROCHOT	
CPUPWRGD/GP95	PCIN	
PCH_VRMPWRGD/GP96	N_PCH_VRMPWRGD	
VR_RDY/GP97	VR_RDY	



PWM各相位的擺法如下:



BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
VCCGT	CPU Graphic Voltage
VCCSA	CPU System Agent Voltage
VCCIO	CPU I/O Voltage
VCC1_0_PCH	PCH core
VDDQ	DRAM voltage
VPP_25V	DRAM VPP voltage
DDRVT	DRAM Terminatio
VREF_DO_AVREF_DQ_B	DRAM Data Ref

散熱模組料號:

Z270M-D3P :  
PCH : 12SP2-S04407-01R/02R/03R  
MOS : 12SP2-S09425-N1R/N2R/N3R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	VCC	FANIO1	IT8686
	FANCVOUT	N/A	N/A	NCT3947
SYS FAN1	FANPWM2	VCC	FANIO2	IT8686
	FAN1_VOUT	N/A	N/A	NCT3947
SYS FAN2	FANPWM3	VCC	FANIO3	IT8686
	FAN2_VOUT	N/A	N/A	NCT3947
SYS FAN3	FANPWM4	VCC	FANIO4	IT8686
	FAN3_VOUT	N/A	N/A	NCT3947