ANALOG DEVICES

*i*Coupler®

Isolated RS-485 Transceiver

Preliminary Technical Data

ADM2483

FEATURES

RS-485 Transceiver with Electrical Data Isolation
2500V_{RMS} for 1 min (UL 1577 Certification)
Complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482:1987(E)
250kbps Data Rate
Slew Rate Limited Driver Outputs
Low power operation:
4.5mA max
Suitable for 5 V or 3 V operation (V_{DD}1)
High common mode transient immunity: >25 KV/ µs
Receiver open-circuit fail-safe design
Glitch-free power-up/down protection
Thermal shutdown protection
Safety and regulatory approvals (pending)
CSA Component Acceptance Notice #5A
VDE Certificate of Conformity
DIN EN 60747-5-2 (VDE 0884 Rev. 2):2003-01
DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000
VIORM = 560 V PEAK
Operating Temperature Range: -40° to 85°C
Wide body 16-lead SOIC package

APPLICATIONS

Low Power RS-485/RS-422 Networks
Isolated Interfaces
Building Control Networks
Multipoint Data Transmission Systems

FUNCTIONAL BLOCK DIAGRAM

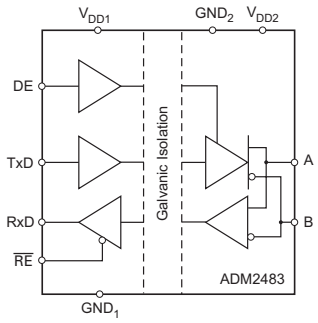

Figure 1.

GENERAL DESCRIPTION

The ADM2483[1] differential bus transceiver is an integrated, galvanically isolated component designed for bi-directional data communication on multi-point bus transmission lines. It is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A and ISO 8482:1987(E). The ADM2483 employs Analog Devices' *i*Coupler technology to combine a 3-channel isolator, a 3-state differential line driver and a differential input receiver into a single package. The logic side of the device can be powered with either a 5V or a 3V supply while the bus-side is powered with a 5V supply.

The ADM2483 is slew limited to reduce reflections with improperly terminated transmission lines. The controlled slew rate limits the data rate to 250 kbps. The input impedance of the ADM2483 is 12 kΩ allowing up to 32 transceivers on the bus. The ADM2483 driver has an active-high enable. The driver differential outputs and the receiver differential inputs are connected internally to form a differential I/O port that imposes minimal loading on the bus when the driver is disabled or when V_{DD1} or V_{DD2} =0. Also provided is an active-high receive disable which causes the receive output to enter a high impedance state.

The AM2483 has current limiting and thermal shutdown features to protect against output short circuits and bus contention situations where these might cause excessive power dissipation.

[1] Protected by U.S. patent 5,952,849. Additional patents are pending.

Rev. PrA

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ELECTRICAL SPECIFICATIONS

Table 1. All voltages are relative to their respective ground; 2.7 ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V. All min/max specifications apply over the entire recommended operation range unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V unless otherwise noted.

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Supply Currents:						
Supply Current, Logic Side, 5V Operation	I_{DD1}			2.5	mA	4.5V ••V_{DD1} ••5.5V, outputs unloaded, receiver enabled
Supply Current, Logic Side, 3V Operation	I_{DD1}			1.3	mA	2.7V ••V_{DD1} ••3.3V, outputs unloaded, receiver enabled
Supply Current, Bus Side						
Driver Enabled	I_{DD2}			2.0	mA	V_{DE} = 0, outputs unloaded, V_{DE} = 5V
Driver Disabled	I_{DD0}			1.7	mA	V_{DE} = 0, outputs unloaded, V_{DE} = 0
Transmit Data Input Current	I_{TXD}	-10	0.01	10	•A	V_{RxD} = V_{DD1} or 0
Driver Enable Input Current	I_{DE}	-10	0.01	10	•A	V_{DE} = V_{DD1} or 0
Receiver Enable Input Current	$I_{\overline{RE}}$	-10	0.01	10	•A	$V_{\overline{RE}}$ = V_{DD1} or 0
Receiver Data:						
Logic High Output Voltage	V_{OHRXD}	V_{DD1} - 0.1	V_{DD1}		V	I_{ORXD} = -20 •A, V_A-V_B = 0.2V
		V_{DD1} - 0.4	V_{DD1}-0.2		V	I_{ORXD} = -4 mA, V_A-V_B = 0.2V
Logic Low Output Voltage	V_{OLRXD}		0.0	0.1	V	I_{ORXD} = 20 •A, V_A-V_B = -0.2V
			0.2	0.4	V	I_{ORXD} = 4 mA, V_A-V_B = -0.2V
Driver Enable:						
Logic High Output Voltage, Bus Enable	V_{OHDE}	V_{DD2} - 0.1	V_{DD2}		V	I_{ODE} = -20 •A
		V_{DD2} - 0.3	V_{DD2}-0.1		V	I_{ODE} = -1.6 mA
		V_{DD2} - 0.4	V_{DD2}-0.2		V	I_{ODE} = -4 mA
Logic Low Output Voltage, Bus Enable	V_{OLDE}		0.0	0.1	V	I_{ODE} = 20 •A
			0.1	0.3	V	I_{ODE} = 1.6 mA
			0.2	0.4	V	I_{ODE} = 4 mA
Receiver Enable:						
Logic High Output Voltage, Receive Enable	$V_{OH\overline{RE}}$	V_{DD2} - 0.1	V_{DD2}		V	$I_{O\overline{RE}}$ = -20 •A
		V_{DD2} - 0.3	V_{DD2}-0.1		V	$I_{O\overline{RE}}$ = -1.6 mA
		V_{DD2} - 0.4	V_{DD2}-0.2		V	$I_{O\overline{RE}}$ = -4 mA
Logic Low Output Voltage, Receive Enable	$V_{OL\overline{RE}}$		0.0	0.1	V	$I_{O\overline{RE}}$ = 20 •A
			0.1	0.3	V	$I_{O\overline{RE}}$ = 1.6 mA

			0.2	0.4	V	$I_{O\overline{RE}}$ = 4 mA
Driver Outputs:						
Differential Output Voltage, Unloaded	$\|V_{OD1}\|$			5.0	V	$R_L = \infty$, Fig. 2
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.0		5.0	V	V_{OC} = 5V, R_L = 100 Ω, Fig. 2
	$\|V_{OD3}\|$	1.5		5.0	V	R_L = 54 Ω, Fig. 2
	$\|V_{OD4}\|$	1.5		5.0	V	-7V ≤ V_{test1} ≤ 12V, $V_{DD1} \geq$ 4.75V, Fig. 3
Change in Differential Output Voltage Magnitude for Complementary Output States	$\Delta\|V_{OD}\|$			0.2	V	R_L = 54 Ω or 100 Ω, Fig. 2
Common Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, Fig. 2
Change in Common Mode Output Voltage Magnitude for Complementary Output States	$\Delta\|V_{OC}\|$			0.2	V	R_L = 54 Ω or 100 Ω, Fig. 2
Short Circuit Output Current	I_{OS}			250	mA	
Receiver Inputs:						
Differential Input Threshold Voltage	V_{TH}	-0.2		0.2	V	
Input Voltage Hysteresis	V_{HYS}		70		mV	V_{OC} = 0V
Input Current (A, B)	I_I			1.0	mA	V_{OC} = 12V
		-0.8			mA	V_{OC} = -7V
Line Input Resistance	R_{IN}	12			kΩ	
AC SPECIFICATIONS						
Transmit Data/Driver Outputs:						
Propagation Delay[2]	t_{TALH}, t_{TAHL}, t_{TBLH}, t_{TBHL}	250		2000	ns	R_L=54 Ω, C_{L1}=C_{L2}=100 pF, Figs. 4 and 8
Driver Skew, $t_{MLH} = \|t_{TALH}-t_{TBLH}\|$, $t_{MHL} = \|t_{TAHL}-t_{TBHL}\|$	t_{MLH}, t_{MHL}		100	800	ns	R_L=54 Ω, C_{L1}=C_{L2}=100 pF, Figs. 4 and 8
Differential Output Rise/Fall Time[6]	t_R, t_F	250		2000	ns	R_L=54 Ω, C_{L1}=C_{L2}=100 pF, Figs. 4 and 8
Driver Enable Time, High Impedance Low/High[6]	t_{AZL}, t_{BZL}, t_{AZH}, t_{BZH}	250		2000	ns	V_{TXD} = V_{DD1} or 0, R_L=500 Ω, C_{L1}= 100 pF, Figs. 5 and 9
Driver Disable Time, Low/High to High Impedance[6]	t_{ALZ}, t_{BLZ}, t_{AHZ}, t_{BHZ}	300		3000	ns	V_{TXD} = V_{DD1} or 0, R_L=500 Ω, C_{L1}= 15 pF, Figs. 5 and 9
Receive Data/Receiver Inputs:						
Propagation Delay[2]	t_{RALH}, t_{RAHL}, t_{RBLH}, t_{RBHL}	250		2000	ns	C_L= 15pF, Figs. 6 and 10
Receiver Skew, $t_{MRLH} = \|t_{RALH}-t_{RBLH}\|$, t_{MRHL} $\|t_{RAHL}-t_{RBHL}\|$	t_{MRLH}, t_{MRHL}		200			
Receive Enable/Disable Time	t_{RE}			10	ns	C_L= 15pF, Figs. 6
Common Mode Transient Immunity[3]	CM	25			KV/µs	V_{TXD} = V_{DD} or 0, V_{CM} = 1000V, transient magnitude = 800V

NOTES:
[1] All voltages are relative to their respective ground.
[2] t_{RALH} and t_{RBLH} propagation delays are measured from the 50% level of the falling edge of the DE signal to the 50% level of the falling edge of the DE signal. t_{DELH} propagation delay is measured from the 50% level of the rising edge of the DE signal to the 50% level of the rising edge of the DE signal.
[3] CM is the maximum common mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

PACKAGE CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		•	
Capacitance (Input-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	
Package Power Dissipation	P_{PD}			600	mW	

NOTE:
[1] Device considered a two-terminal device: pins 1, 2, 3,4,5,6,7, and 8 shorted together and pins 9,10,11,12,13,14,15, and 16 shorted together.

REGULATORY INFORMATION

The ADM2483 will be approved by the following organizations upon product release:

UL[1]	CSA	VDE[2]
To be recognized under 1577 component recognition program	To be approved under CSA Component Acceptance Notice #5A	To be approved according to: DIN EN 60747-5-2 (VDE 0884 Rev. 2):2002-04 DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000

NOTES:
[1] In accordance with UL1577, each ADM2483 is proof tested by applying an insulation test voltage ≥3000 Vrms for 1 second (current leakage detection limit = 5 μA)
[2] In accordance with VDE 0884, each ADM2483 is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 2.

Parameter	Symbol	Value	Unit	Conditions
Rated dielectric insulation voltage		2500	V_{RMS}	1-minute duration.
Minimum external air gap (clearance)	L(I01)	7.40 min.	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum external tracking (creepage)	L(I02)	8.51 min.	mm	Measured from input terminals to output terminals, shortest distance path along body.
.				
Minimum internal gap (internal clearance)		0.02 min.	mm	Insulation distance through insulation.
Tracking resistance (comparative tracking index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation group		IIIa		Material Group (DIN VDE 0110,1/89,Table 1)

VDE 0884 INSULATION CHARACTERISTICS

Table 3. This isolator is suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety date shall be ensured by means of protective circuits.
"*" marking on packages denotes VDE 0884 approval for 560 VPEAK working voltage.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, for rated mains voltage			
≤ 150 Vrms		I to IV	
≤ 300 Vrms		I to III	
≤ 400 Vrms		I to II	
Climatic classification		40/85/21	
Pollution degree (DIN VDE 0110, Table 1)		2	
Maximum working insulation voltage	V_{IORM}	400	V_{PEAK}
Input to output test voltage, Method b1	V_{PR}	1050	V_{PEAK}
$V_{IORM} \times 1.875 = V_{PR}$, 100% production test,			
t_m = 1sec, partial discharge < 5 pC			
Input to output test voltage, Method a			
(After environmental tests Subgroup 1)			
V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC		896	Vpeak
(After input and/or safety test Subgroup 2/3)			
V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	Vpeak
Highest allowable over-voltage			
(Transient over-voltage, t_{TR} =10 sec)	V_{TR}	4000	V_{PEAK}
Safety-limiting values (maximum value allowed in the event of a failure. See thermal derating curve, Figure 1)			
Case temperature	TS		°C
Input current	$I_{S, INPUT}$		mA
Output current	$I_{S,OUTPUT}$		mA
Insulation resistance at Ts, V_{IO} = 500 V	Rs	$>10^9$	Ω

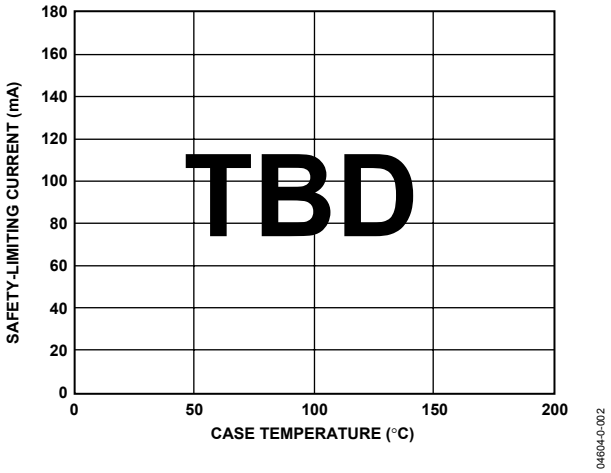

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884.

RECOMMENDED OPERATING CONDITIONS

Table 4.All voltages are relative to their respective ground.

Parameter	Symbol	Min.	Max.	Unit
Operating temperature	T_A	-40	85	°C
Supply voltages	V_{DD1}	2.7	5.5	V
	V_{DD1}	4.5	5. 5	V
Input bus voltage (separately or common mode)	V_{IB}	-7	12	V
Differential input bus magnitude	$\|V_{ID}\|$		12	V
Logic high input voltages, 5 V operation1	V_{TxDH}, V_{RTSH}, $V_{\overline{REH}}$	0.7 V_{DD1}	V_{DD1}	V
Logic low input voltages, 5 V operation1	V_{TxDL}, V_{RTSL}, $V_{\overline{REL}}$	0.0	0.3 V_{DD1}	V
Logic high input voltages, 3 V operation1	V_{TxDH}, V_{RTSH}, $V_{\overline{REH}}$	0.7 V_{DD1}	V_{DD1}	V
Logic low input voltage, 3 V operation1	V_{TxDL}, V_{RTSL}, $V_{\overline{REL}}$	0.0	0.25 V_{DD1}	V
Input signal rise and fall times			1.0	ms
Data rate (NRZ)	r_{BIT}	0	250	kBd

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination.

Table 5. Ambient temperature = 25 °C unless otherwise noted. All voltages are relative to their respective ground.

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	T_S	-55	150	°C
Ambient operating temperature	T_A	-40	100	°C
Supply voltages	V_{DD1},V_{DD2}	-0.5	6.5	V
Logic input voltages	V_{TxD}, V_{RTS}, $V_{\overline{RE}}$	-0.5	V_{DD1} + 0.5	V
Bus terminal voltages	A, B	-9	14	V
Logic output voltages	RxD, DE	-0.5	V_{DDO} + 0.5	V
Average output current, per pin	I_O	-35	35	mA
ESD (human body model)		-2.0	2.0	KV
Thermal impedance	Θ_{JC}		TBD	°C/W
	Θ_{JA}		105	°C/W
Lead solder temperature (hand soldering) Heating at lead tip 275°C ±10° for 20 seconds				
Solder reflow temperature profile JEDEC Standard 20A				

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TRUTH TABLES

The truth tables in this section use these abbreviations:

Letter	Description
H	High level
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

See the Power Up/Power-Down Characteristics section for additional information.

Table 6.Transmitting

	INPUTS		OUTPUTS	
SUPPLIES	**DE**	**T×D**	**A**	**B**
V_{DD1} and V_{DD2} On	H	H	H	L
V_{DD1} and V_{DD2} On	H	L	L	H
V_{DD1} and V_{DD2} On	L	X	Z	Z
V_{DD1} and/or V_{DD2} Off	X	X	Z	Z

Table 7. Receiving

	INPUTS		OUTPUT
SUPPLIES	**A-B**	$\overline{\text{RE}}$	**R×D**
VDD1 and VDD2 On	> 0.2V	L or NC	H
VDD1 and VDD2 On	< -0.2V	L or NC	L
VDD1 and VDD2 On	-0.2 <A-B< 0.2	L or NC	Indeterminate
VDD1 and VDD2 On	Inputs Open	L or NC	H
VDD1 and VDD2 On	X	H	Z
VDD1 and/or VDD2 Off	X	L or NC	H

PIN CONFIGURATION

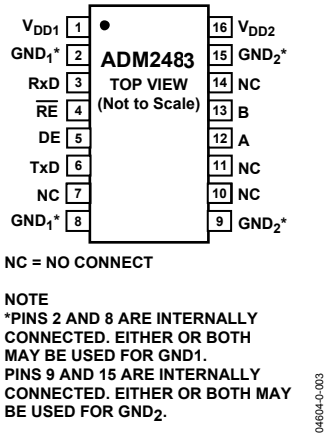

Figure 3.

Table 8.Pin Function Description

Pin(s)	Mnemonic	Function
1	V_{DD1}	Power supply, logic side
2, 8	GND_1	Ground, logic side
3	R × D	Receiver output.
4	$\overline{\text{RE}}$	Receiver enable
5	DE	Request to send
6	TxD	Transmit data
9, 15	GND2	Ground, bus side
12	A	Noninverting receiver input/driver output
13	B	Inverting receiver input/driver output
16	V_{DD2}	Power supply, bus side

TEST CIRCUITS

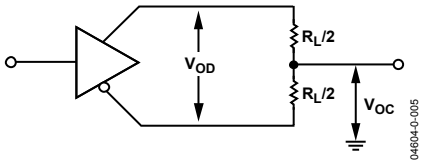

Figure 4. Driver Voltage Measurement Test Circuit

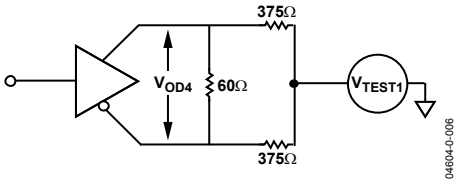

Figure 5. Driver Voltage Measurement Test Circuit

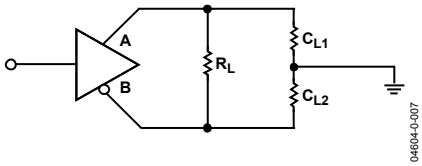

Figure 6. Driver Propagation Delay Test Circuit

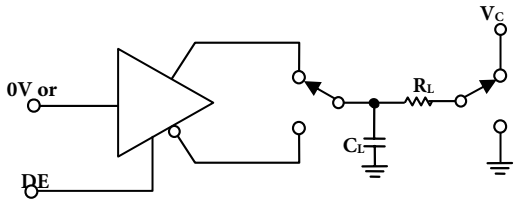

Figure 7. Driver Enable Test Circuit

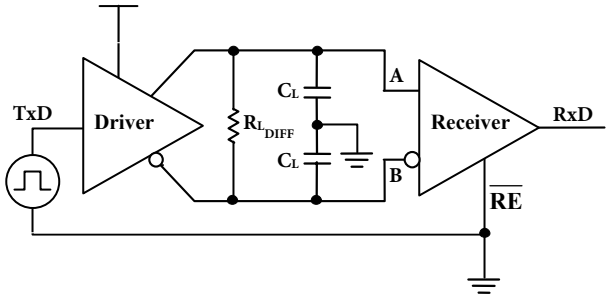

Figure 8. Receiver Propagation Delay Test Circuit

SWITCHING CHARACTERISTICS

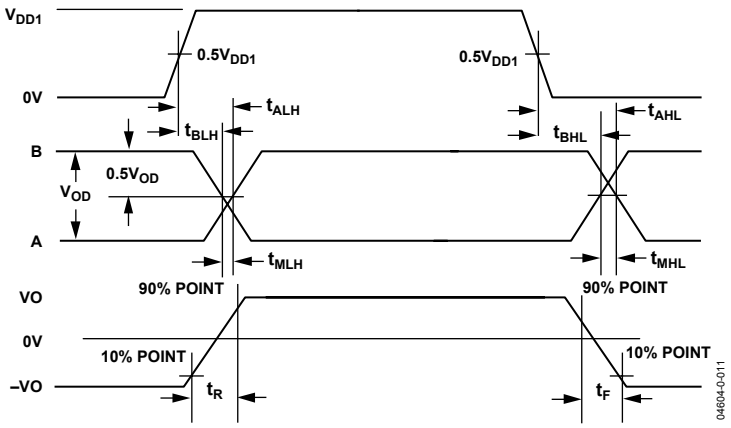

Figure 9. Driver Propagation Delay, Rise/Fall Timing

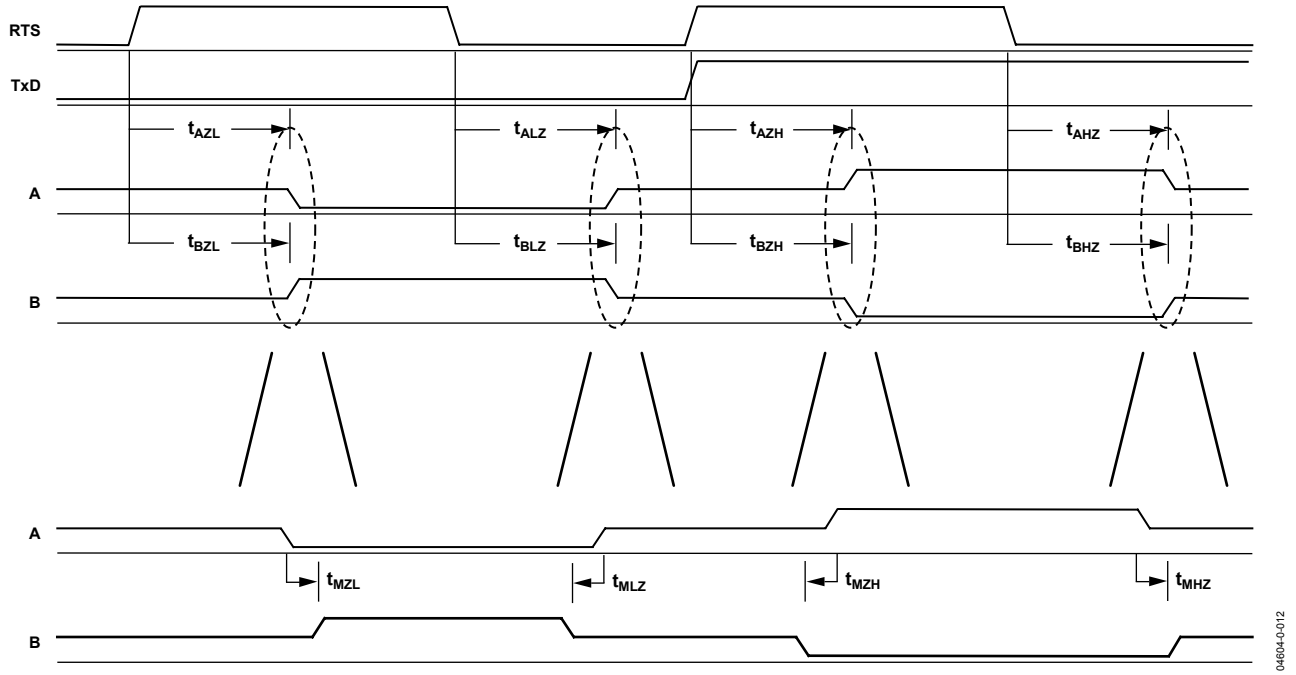

Figure 10 Driver Enable/Disable Timing

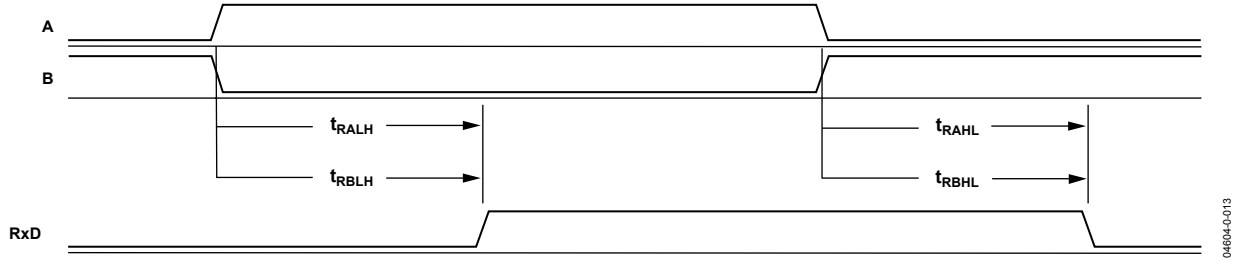

Figure 11. Receiver Propagation Delay

APPLICATION INFORMATION

POWER-UP/POWER-DOWN CHARACTERISTICS

The power-up/power-down characteristics of the ADM2483 are in accordance with the supply thresholds shown in **Table 9**. Upon power-up, the ADM2483 output signals (A, B, RxD and DE) reach their correct state once both supplies have exceeded their thresholds. Upon power-down, the ADM2483 output signals retain their correct state until at least one of the supplies drops below its power down threshold. When the VDD1 power-down threshold is crossed, the ADM2483 output signals reach their unpowered states within 4 µs.

Table 9.Power Up/Power-Down Thresholds

			Unpowered States			
Supply	**Transition**	**Threshold**	**A**	**B**	**RxD**	**DE**
VDD1	Power Up	2.0V	Z	Z	H	L
VDD1	Power Down	1.0V				
VDD2	Power Up	3.3V				
VDD2	Power Down	2.4V				

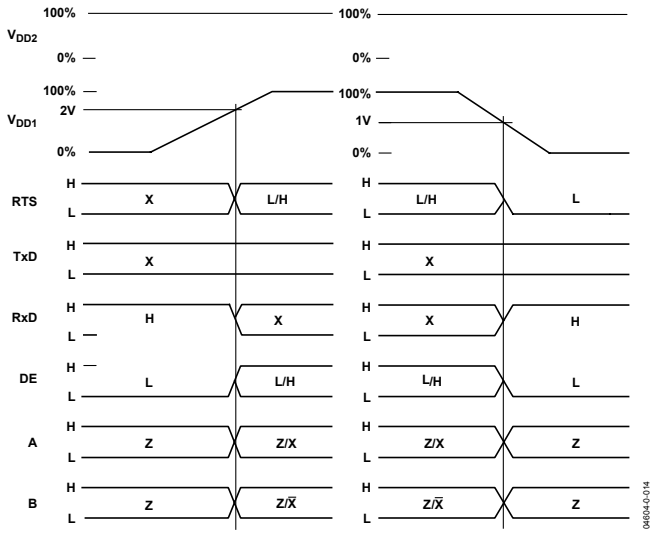

Figure 12. VDD1 Power Up/Down

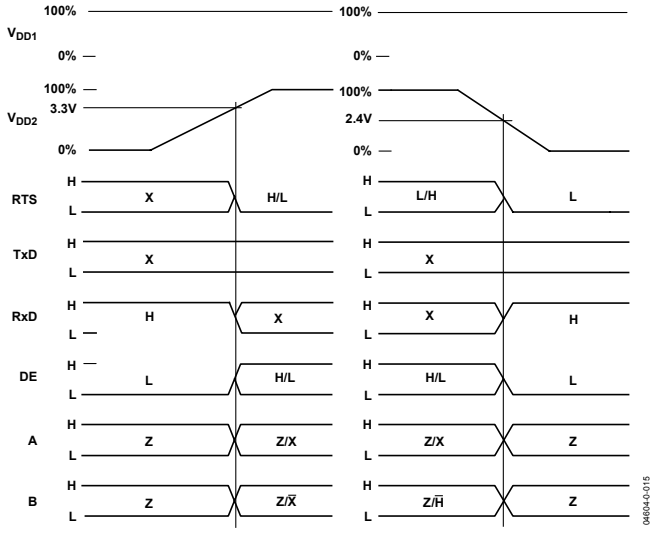

Figure 13. VDD2 Power Up/Down

THERMAL SHUTDOWN

The ADM2483 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER OPEN-CIRCUIT FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating or open circuited.

MAGNETIC FIELD IMMUNITY

The ADM2483 is immune to external magnetic fields. The ADM2483's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the Decoder. The analysis below defines the conditions under which this may occur. The ADM2483's 3 V operating condition is examined as it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0 V in amplitude. The Decoder has sensing thresholds at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The induced voltage induced across the receiving coil is given by $V = (-d/dt)\, rn2;\ n = 1,2,\ldots,N$ where:

β = magnetic flux density (Gauss)

N = number of turns in receiving coil

r_n = radius of nth turn in receiving coil (cm)

Given the geometry of the receiving coil and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the Decoder, a maximum allowable magnetic field is calculated as shown in Figure 14.

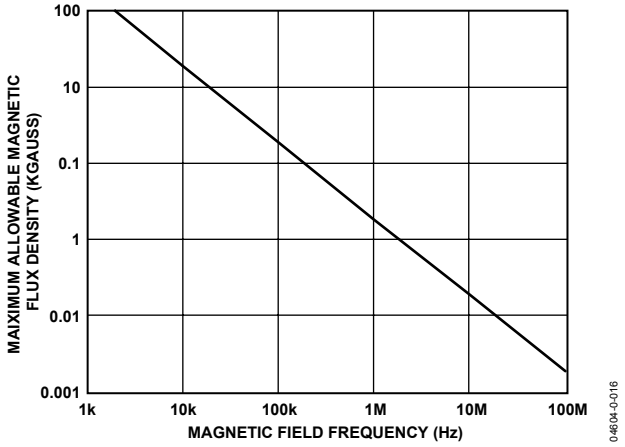

Figure 14. Maximum Allowable External Magnetic Flux Density.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 KGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and was of the worst-case polarity) it would reduce the received pulse from > 1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the Decoder.

As a convenience to the user, the above magnetic flux density values are shown below in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2483 transformers.

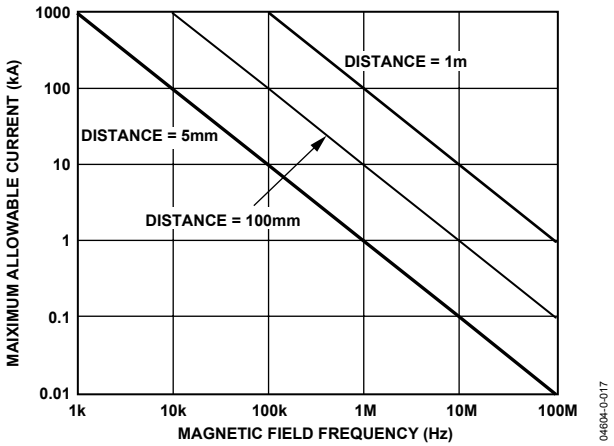

Figure 15. Maximum Allowable Current for Various Current-to-ADM2483 Spacings.

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

OUTLINE DIMENSIONS

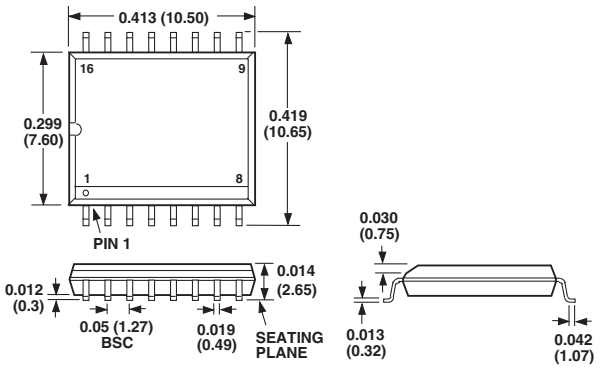

Figure 16. 16-Lead Wide-Body Small Outline Package [SOIC]

(RW-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Max. Data Rate (kbps)	Temperature Range	Package Description	Package Option
ADM2483BRW	250	−40°C to +85°C	16-Lead Wide Body SOIC	

The addition of an "-RL" suffix designates a 13" (1000 units) tape and reel option.

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