GOWIN

PROGRAMMING FOR THE FUTURE

GW2AN-18X and GW2AN-9X

Data Sheet

DS971-1.07E, 02/24/2023

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Revision History

Date	Version	Description
09/21/2020	1.0E	Initial version published.
07/16/2021	1.01E	The GW2AN-9X information improved.
10/28/2021	1.02E	The GW2AN-9X UG256, PG256, and UG324 packages added.
05/25/2022	1.03E	● Recommended Operating Conditions updated. ● Power Supply Ramp Rates updated.
08/26/2022	1.04E	● The maximum value of the differential input threshold V_{THD} updated. ● Note about DC current limit added. ● 3.9.1 I2C Timing Characteristics added.
09/07/2022	1.05E	● Table 4-3 Power Supply Ramp Rates updated. ● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Figure 3-1 Architecture Diagram updated.
11/11/2022	1.06E	● Table 4-2 Recommended Operating Conditions updated. ● Table 4-5 POR Specifications updated. ● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Table 4-9 Static Supply Current updated.
02/24/2023	1.07E	● Table 4-1 Absolute Max. Ratings updated. ● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Information on Slew Rate removed. ● Description of the on-chip differential termination resistor modified.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW2AN series of the FPGA products, which helps you to understand the GW2AN series of the FPGA products quickly and select and use devices appropriately.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at *www.gowinsemi.com*:

- *UG702*, GW2AN-18X & 9X Programming and Configuration User Guide
- *UG973, GW2AN series of FPGA Products Package and Pinout*
- *UG972, GW2AN-18X Pinout*
- *UG978, GW2AN-9X Pinout*

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
GPIO	Gowin Programable IO
IOB	Input/Output Block
LUT4	4-input Look-up Table
LUT5	5-input Look-up Table
LUT6	6-input Look-up Table
LUT7	7-input Look-up Table
LUT8	8-input Look-up Table
PG	PBGA
PLL	Phase-locked Loop
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing
UG	UBGA

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: *www.gowinsemi.com*

E-mail: *support@gowinsemi.com*

2 General Description

The GW2AN series of FPGA products are the first generation non-volatile FPGA products of the Arora family. They offer a range of comprehensive features and rich internal resources, a high-speed LVDS interface, abundant BSRAM memory resources, and NOR Flash resources. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2AN series of FPGA products suitable for high-speed, low-cost applications.

GOWINSEMI continually invests the development of next-generation FPGA hardware environment through the market-oriented independent research and developments that supports the GW2AN series of FPGA products, which can be used for FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- Lower power consumption
  - 55nm technology
  - LV version: Supports 1.0V core voltage;
  - EV version: Supports 1.2 V core voltage;
  - UV version: Supports 2.5V and 3.3 V core voltage;
  - Clock dynamically turns on and off
- Multiple I/O standards
  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, II, SSTL15; HSTL18 I, II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA, etc. drive options
  - Output drive strength option
  - Individual bus keeper, weak pull-up, weak pull-down, and open drain option

  - Hot socket
- Abundant slices
  - Four input LUT (LUT4)
  - Supports shift register and distributed register
- Integrate NOR Flash
- Block SRAM with multiple modes
  - Supports dual port, single port, and semi-dual port
  - Supports byte write enable
- Flexible PLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Configuration
  - Supoprts JTAG configuration
  - Five GowinCONFIG configuration modes: SSPI, Autoboot, CPU, I^2C, SERIAL
  - Supoprts I^2C and SSPI background update
  - Supports JTAG and SSPI programming SPI Flash directly and other modes programming SPI Flash via IP
  - Data stream file encryption and security bit settings

2.2 Product Resources

Table 2-1 Product Resources

Device	GW2AN-9X	GW2AN-18X
LUT4	10368	20,736
Registers/Latches	10368	20,736
SSRAM(bits)	41472	41,472
BSRAM(bits)	540K	540K
BSRAM quantity	30	30
NOR Flash	16M bit	16M bit
PLLs	2	2
Global Clock	8	8
High Speed Clock	8	8
LVDS (Mb/s)	1250	1250
MIPI (Mb/s)	1200	1200
Total number of I/O banks	9	9
Max. I/O	389	389
Core Voltage (LV)	1.0V	1.0V

Device	GW2AN-9X	GW2AN-18X
Core Voltage (EV)	1.2V	1.2V
Core Voltage (UV)	2.5V/3.3V	2.5V/3.3V

Table 2-2 GW2AN-18X PLL List

Package	Device	PLL
PG256	GW2AN-18X	PLLL/PLLR
UG256	GW2AN-18X	PLLL/PLLR
UG324	GW2AN-18X	PLLL/PLLR
UG332	GW2AN-18X	PLLL/PLLR
UG400	GW2AN-18X	PLLL/PLLR
UG484	GW2AN-18X	PLLL/PLLR

Table 2-3 Package Information, Max. User I/O, and LVDS Pairs

Package	Pitch(mm)	Size(mm)	E-pad Size (mm)	GW2AN-9X	GW2AN-18X
UG484	0.8	19 x 19	-	383（96）	383（96）
UG400	0.8	17 x 17	-	335（95）	335（95）
UG256	0.8	14 x 14	-	207（86）	207（86）
PG256	1.0	17 x 17	-	207（86）	207（86）
UG332	0.8	17 x 17	-	-	279（82）
UG324	0.8	15 x 15	-	279（74）	279（74）
PG484	1.0	23 x 23	-	-	381（96）

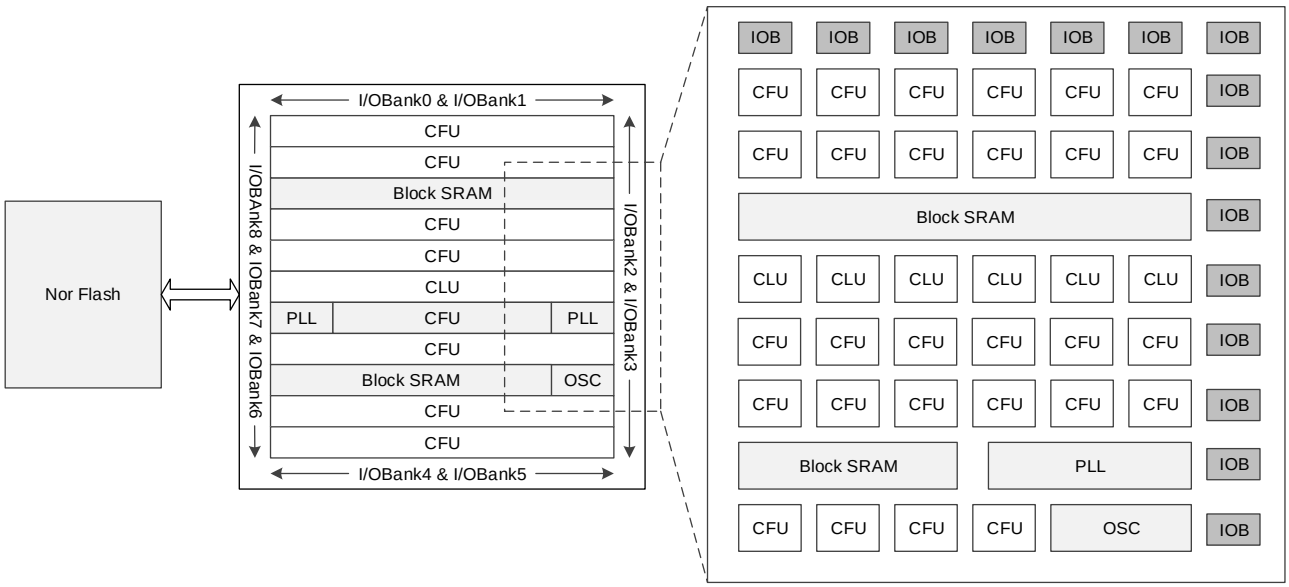
Note!

- The package types in this data sheet are written with abbreviations. See 5.1 Part Name for further information.
- JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max.User I/O noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. For further detailed information, pelase refer to *UG973, GW2AN series of FPGA Products Package and Pinout* .

3 Architecture

3.1 Architecture Overview

Figure 3-1 Architecture Diagram



See Figure 3-1 for an overview of the architecture of the GW2AN series of FPGA products. GW2AN series integrates the NOR Flash memory chip. For the NOR Flash features, please refer to 3.2 NOR FLASH.

Please refer to Table 2-1 for the GW2AN-18X device internal resources. The core of device is an array of Configurable Logic Unit (CFU) surrounded by IO blocks. Besides, GW2AN provides BSRAM, PLL, and on chip oscillator.

Configurable Function Unit (CFU) is the base cell for the array of GW2AN series FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see 3.3 Configurable Function Unit.

The I/O resources in the GW2AN series of FPGA products are arranged around the periphery of the devices in groups referred to as

banks, which are divided into nine Banks, including Bank0 ~ Bank8. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see 3.4 IOB.

The BSRAM is embedded as a row in the GW2AN series of FPGA products. Each BSRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. For more detailed information, see 3.5 Block SRAM (BSRAM).

GW2AN provides one PLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each GW2AN series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 1.5625 MHz to 100 MHz, providing the clock resource for the MSPI mode. It also provides a clock resource for user designs with the clock precision reaching ±5%. For more detailed information, please refer to 3.6 Clock, 3.10 On Chip Oscillator.

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW2AN series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see 3.7 Long Wire (LW)*, and* 3.8 Global Set/Reset (GSR).

3.2 NOR FLASH

GW2AN series of FPGA products integrate the NOR Flash memory chip.The features are as follows:

- Full voltage range: 1.65V - 3.465V
- 16Mb of storage, 256 bytes per page;
- Supports SPI;
- Clock frequency: 100MHz;
- Software/Hardware Write Protection
  - All/Partial write protection via software setting
  - Top/Bottom Block protection
- Minimum 100,000 Program/Erase cycles;
- Fast program/ Erase Speed
  - Page program time: 1ms;
  - Sector erase time: 100ms;
  - Block erase time: 0.3s/0.5s;
  - Chip erase time: 10s
- Data retention: 20 years

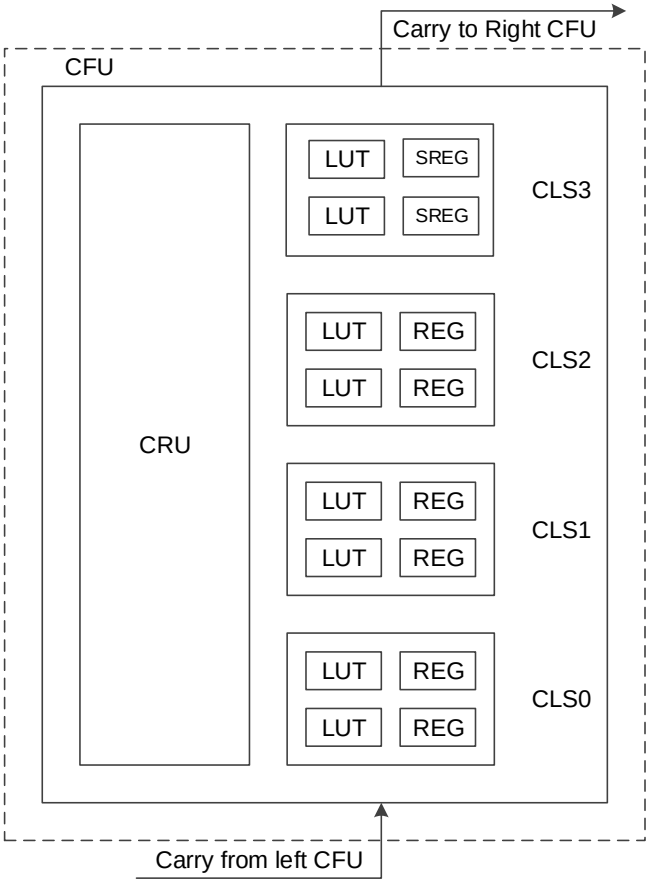
3.3 Configurable Function Unit

The configurable function unit(CFU) and the configurable logic unit(CLU) are two basic units for FPGA core of GOWINSEMI. As shown in Figure 3-2, each unit consists of four configurable logic sections and its configurable routing unit. Each of the three configurable logic sections contains two 4-input LUTs and two registers, and the other one only contians two 4-input LUTs.

Configurable logical sections in CLU cannot be configured as SRAM, but as basic logic, ALU, and ROM. The configurable logic sections in the CFU can be configured as basic logic, ALU, SRAM, and ROM depending on the applications.

For further more information about CFU, please refer to *UG288, Gowin Configurable Function Unit (CFU) User Guide*.

Figure 3-2 CFU Structure



Note!

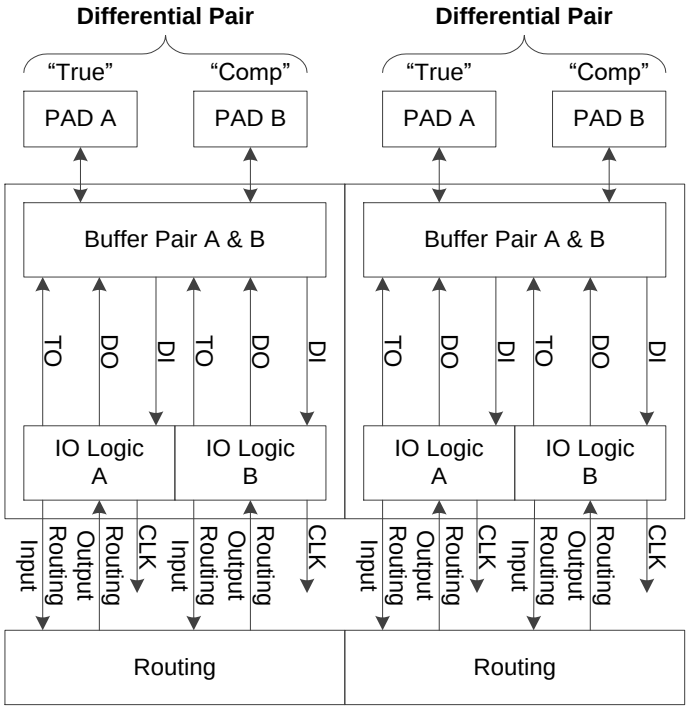
SREG needs special patch supporting. Please contact Gowin technical support or local O ffice for this patch.

3.4 IOB

The IOB in the GW2AN series of FPGA products includes IO Buffer, IO Logic, and its Routing Unit. As shown below, each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a

Single-ended input/output.

Figure 3-3 IOB Structure View



IOB Features:

- V_{CCO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode

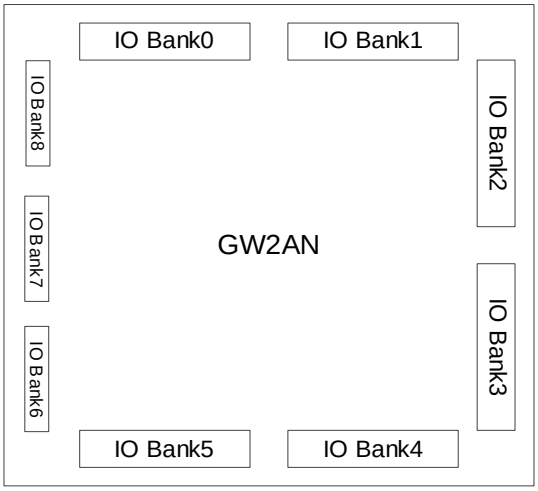
3.4.1 ~ 3.4.3 describe I/O buffer, I/O logic, and I/O logic modes. For further information about IOB, please refer to UG289, Gowin Programable IO User Guide.

3.4.1 I/O Buffer

There are nine I/O Banks in the GW2AN-18X and GW2AN-9X products, as shown in Figure 3-4. Each Bank has independent IO source V_{CCO}. V_{CCO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. For more detailed information, please refer to Table 4-2. In order to support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as reference voltage. User can choose from internal reference voltage of the bank (0.5 x V_{CCO}) or external reference voltage using any IO from the bank.

Different banks in the GW2AN-18X and GW2AN-9X Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O and is supported in Bank 2/3/6/7/8. Differential resistor is set for LVDS input and is only supported in Bank 4/5. Bank4/5 supports 100Ω on-chip differential termination resistors. Please refer to UG289, Gowin Programable IO User Guide for more detailed information.

Figure 3-4 GW2AN I/O Bank Distribution



Note!

By default, the Gowin Programmable IO is tri-stated weak pull-down.

The GW2AN series of FPGA products support LV, EV, and UV versions.

LV devices support 1.0 V V_{CC} and EV devices support 1.2 V V_{CC} to meet users' low power needs.

V_{CCO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V according to requirements.

Linear voltage regulator is integrated in UV devices to facilitate single power supply. UV devices support 2.5 V and 3.3 V.

For the V_{CCO} requirements of different I/O standards, see Table 3-1.

Table 3-1 Output I/O Standards and Configuration Options

I/O output standard	Single-ended/Differential	Bank V_{CCO} (V)	Driver Strength (mA)	Typ. Applicaiton
LVTTL33	Single-ended	3.3	4,8,12,16,24	universal interface
LVCMOS33	Single-ended	3.3	4,8,12,16,24	universal interface
LVCMOS25	Single-ended	2.5	4,8,12,16	universal interface
LVCMOS18	Single-ended	1.8	4,8,12	universal interface
LVCMOS15	Single-ended	1.5	4,8	universal interface
LVCMOS12	Single-ended	1.2	4,8	universal interface
SSTL25_I	Single-ended	2.5	8	memory interface
SSTL25_II	Single-ended	2.5	8	memory interface

I/O output standard	Single-ended/Differential	Bank V_{CCO} (V)	Driver Strength (mA)	Typ. Applicaiton
SSTL33_I	Single-ended	3.3	8	memory interface
SSTL33_II	Single-ended	3.3	8	memory interface
SSTL18_I	Single-ended	1.8	8	memory interface
SSTL18_II	Single-ended	1.8	8	memory interface
SSTL15	Single-ended	1.5	8	memory interface
HSTL18_I	Single-ended	1.8	8	memory interface
HSTL18_II	Single-ended	1.8	8	memory interface
HSTL15_I	Single-ended	1.5	8	memory interface
PCI33	Single-ended	3.3	N/A	PC and embedded system
LVPECL33E	Differential	3.3	16	High-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
RSDS25E	Differential	2.5	8	high-speed point-to-point data transmission
LVDS25E	Differential	2.5	8	high-speed point-to-point data transmission
LVDS25	Differential (TLVDS)	2.5/3.3	3.5/2.5/2/1.25	high-speed point-to-point data transmission
RSDS	Differential (TLVDS)	2.5/3.3	2	high-speed point-to-point data transmission
MINILVDS	Differential (TLVDS))	2.5/3.3	2	LCD timing driver interface and column driver interface
PPLVDS	Differential (TLVDS)	2.5/3.3	3.5	LCD row/column driver
SSTL15D	Differential	1.5	8	memory interface
SSTL25D_I	Differential	2.5	8	memory interface
SSTL25D_II	Differential	2.5	8	memory interface
SSTL33D_I	Differential	3.3	8	memory interface
SSTL33D_II	Differential	3.3	8	memory interface
SSTL18D_I	Differential	1.8	8	memory interface
SSTL18D_II	Differential	1.8	8	memory interface
HSTL18D_I	Differential	1.8	8	memory interface
HSTL18D_II	Differential	1.8	8	memory interface
HSTL15D_I	Differential	1.5	8	memory interface

I/O output standard	Single-ended/Differential	Bank V_{CCO} (V)	Driver Strength (mA)	Typ. Applicaiton
LVCMOS12D	Differential	1.2	8/4	universal interface
LVCMOS15D	Differential	1.5	8/4	universal interface
LVCMOS18D	Differential	1.8	8/12/4	universal interface
LVCMOS25D	Differential	2.5	8/16/12/4	universal interface
LVCMOS33D	Differential	3.3	8/24/16/12/4	universal interface

Table 3-2 Intput I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVTTL33	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single-ended	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single-ended	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single-ended	2.5/3.3	No	Yes
SSTL25_II	Single-ended	2.5/3.3	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
SSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
SSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_I	Single-ended	1.8/2.5/3.3	No	Yes
HSTL18_II	Single-ended	1.8/2.5/3.3	No	Yes
HSTL15_I	Single-ended	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	No	No
LVCMOS33OD18	Single-ended	1.8	No	No
LVCMOS33OD15	Single-ended	1.5	No	No
LVCMOS25OD18	Single-ended	1.8	No	No
LVCMOS25OD15	Single-ended	1.5	No	No
LVCMOS18OD15	Single-ended	1.5	No	No
LVCMOS15OD12	Single-ended	1.2	No	No
LVCMOS25UD33	Single-ended	3.3	No	No
LVCMOS18UD25	Single-ended	2.5	No	No
LVCMOS18UD33	Single-ended	3.3	No	No
LVCMOS15UD18	Single-ended	1.8	No	No
LVCMOS15UD25	Single-ended	2.5	No	No
LVCMOS15UD33	Single-ended	3.3	No	No

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVCMOS12UD15	Single-ended	1.5	No	No
LVCMOS12UD18	Single-ended	1.8	No	No
LVCMOS12UD25	Single-ended	2.5	No	No
LVCMOS12UD33	Single-ended	3.3	No	No
LVDS25	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS12D	Differential	1.2/1.5/1.8/2.5/ 3.3	No	No
LVCMOS15D	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS18D	Differential	1.8/2.5/3.3	No	No
LVCMOS25D	Differential	2.5/3.3	No	No
LVCMOS33D	Differential	3.3	No	No

3.4.2 I/O Logic

Figure 3-5 shows the I/O logic output of the GW2AN series of FPGA

products.

Figure 3-5 I/O Logic Output

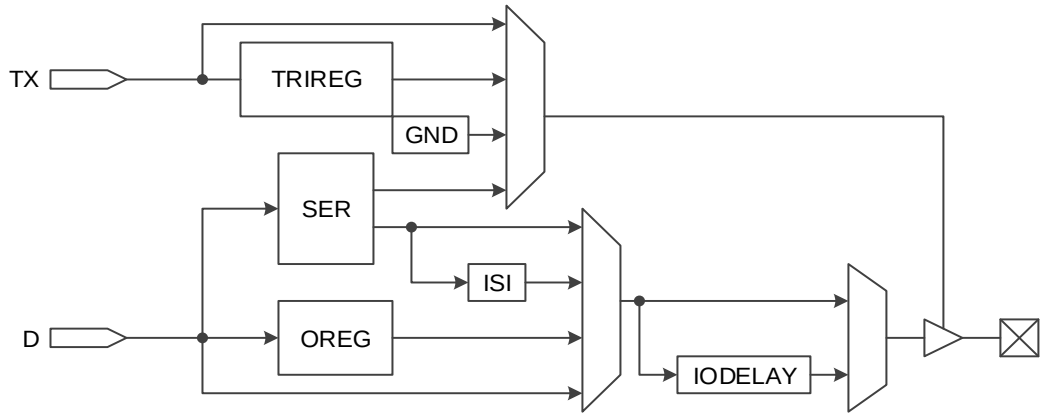


Figure 3-6 shows the I/O logic input of the GW2AN series of FPGA products.

Figure 3-6 I/O Logic Input

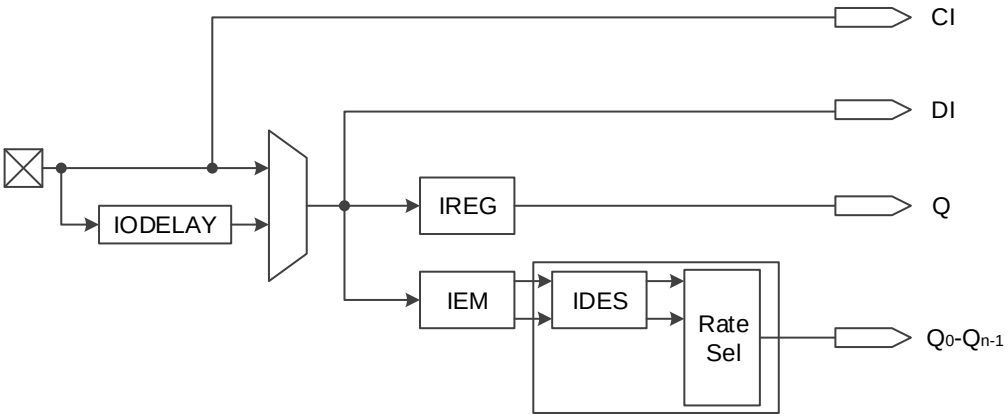


Table 3-3 Port Descsription

Ports	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to UG972, GW2AN-18X Pinout, UG978, GW2AN-9X Pinout.
DI	Input	IO port low-speed input signal, entering into Fabric directly.
Q	Output	IREG output signal in SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in DDR module.

Note!

When CI is used as GCLK input, DI, Q, and Q_0-Q_{n-1} cannot be used as I/O input and output.

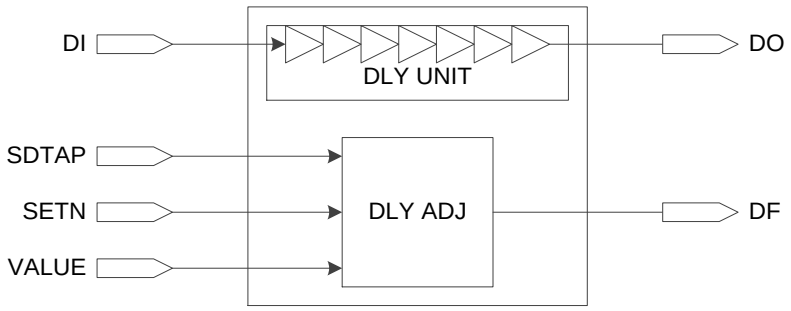
A description of the I/O logic modules of the GW2AN series of FPGA products is presented below.

IODELAY

See Figure 3-7 for an overview of the IODELAY. Each I/O of the

GW2AN series of FPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 18ps.

Figure 3-7 IODELAY



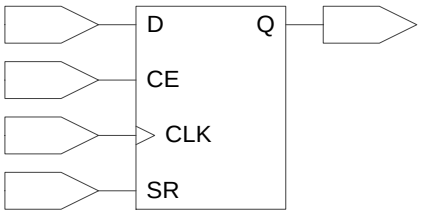
The delay cell can be controlled in two ways:

- Static control.
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time.

I/O Register

See Figure 3-8 for the I/O register in the GW2AN series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and a tristate Register (TRIREG).

Figure 3-8 Register Structure in I/O Logic



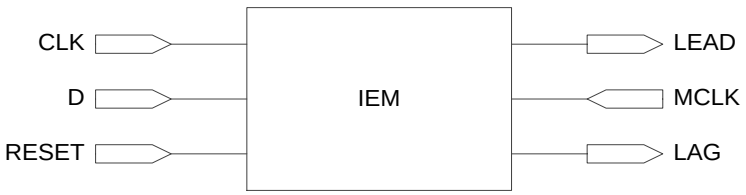
Note!

- CE can be either active low (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode, as shown in Figure 3-9.

Figure 3-9 IEM Structure



De-serializer DES and Clock Domain Transfer

The GW2AN series of FPGA products provides a simple serializer SER for each output I/O to support advanced I/O protocols. The Clock domain transfer module of the input clock in DES provides the ability to safely switch the external sampling clock to the internal continuous running clock. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- The internal continuous clock is used instead of the discontinuous DQS for data sampling. The function is applied to the interface of DDR memory.
- For the DDR3 memory interface standard, align the data after DQS read-leveling.
- In regular DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module also needs to be used.

Each DQS provides WADDR and RADDR signals to the same group in the clock domain transfer module.

Serializer SER

The GW2AN series of FPGA products provides a simple serializer (SER) for each output I/O to support advanced I/O protocols.

3.4.3 I/O Logic Modes

The I/O Logic in the GW2AN series of FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

3.5 Block SRAM (BSRAM)

3.5.1 Introduction

The GW2AN series of FPGA products provide abundant SRAM. The Block SRAM (BSRAM) is embedded as a row in the FPGA array and is different from SSRAM (Shadow SRAM). Each BSRAM occupies three columns of CFU in the FPGA array. Each BSRAM has 18,432 bits (18Kbits). There are five operation modes: single port, dual port, semi-dual port, ROM, and FIFO. The signals and functional descriptions of BSRAM are listed in the following table.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features include the following:

- Max.18,432 bits per BSRAM
- BSRAM itself can run at 380 MHz at max (typical, Read-before-write is 230MHz)
- Single port
- Dual port
- Semi-dual port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Normal read and write mode
- Read-before-write mode
- Write-through mode

3.5.2 Configuration Mode

The BSRAM mode in the GW2AN series of FPGA products supports different data bus widths. See Table 3-4.

Table 3-4 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Single Port Mode

In the single port mode, BSRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of BSRAM. Normal-Write Mode and Write–through Mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

Dual Port Mode

BSRAM support dual port mode. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

Note!

DP mode does not support Read-before-write.

For further information about Dual Port Block Memory ports and the related description, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

Semi-Dual Port Mode

Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to *UG285, Gowin BSRAM & SSRAM User Guide*.

Read Only

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to*UG285, Gowin BSRAM & SSRAM User Guide*.

3.5.3 Mixed Data Bus Width Configuration

The BSRAM in the GW2AN series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-5 and Table 3-6 below.

Table 3-5 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*"denotes the modes supported.

Table 3-6 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512x36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*"denotes the modes supported.

3.5.4 Byte-enable

The BSRAM in the GW2AN series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the BSRAM write operation.

3.5.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

3.5.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write.
- The output register can be used as a pipeline register to improve design performance.
- The output registers are bypass-able.

3.5.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.5.8 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the BSRAM via output registers or without using the registers.

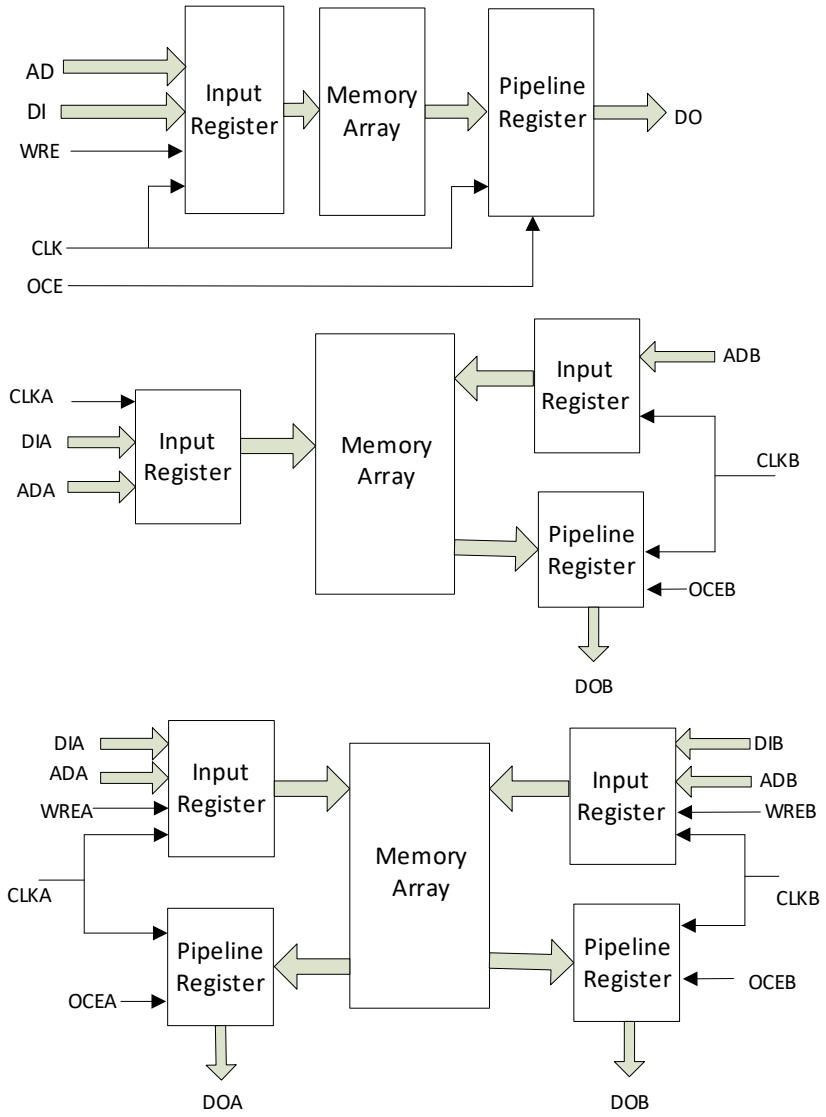
Pipeline Mode

While writing in the BSRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of the memory array.

Figure 3-10 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port



Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

Note!

DP mode does not support Read-before-write.

3.5.9 Clock Operations

Table 3-7 lists the clock operations in different BSRAM modes:

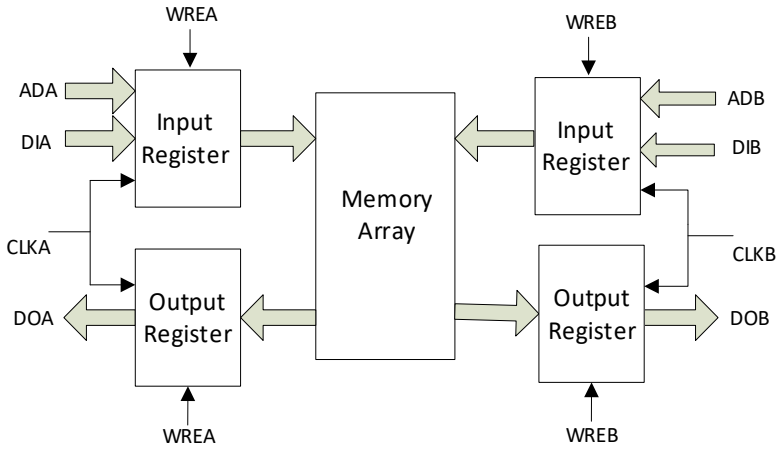
Table 3-7 Clock Operations in Different BSRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-11 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

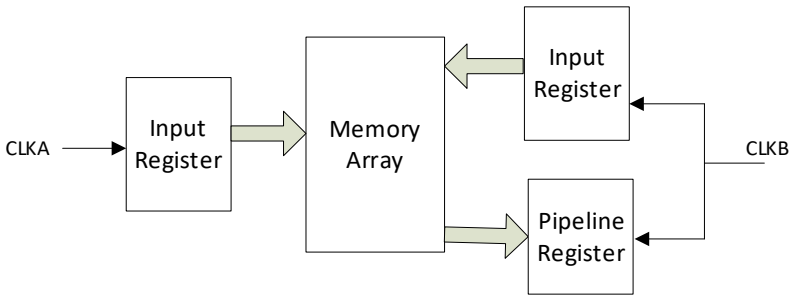
Figure 3-11 Independent Clock Mode



Read/Write Clock Operation

Figure 3-12 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

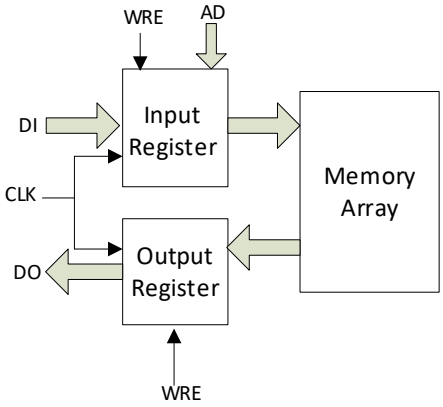
Figure 3-12 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-13shows the clock operation in single port mode.

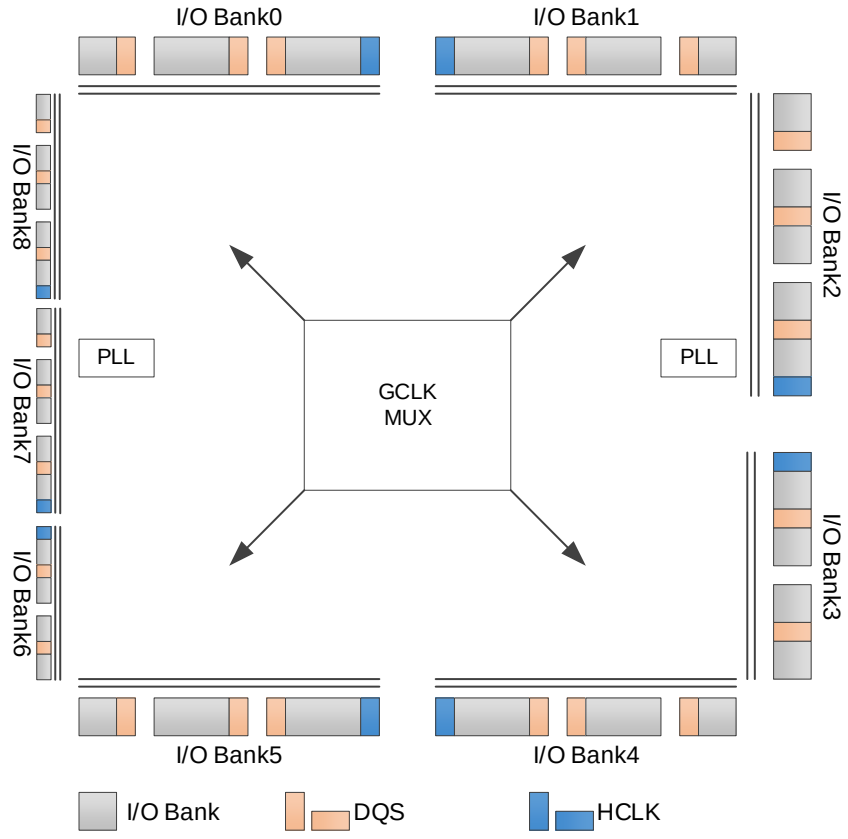
Figure 3-13 Single Port Clock Mode



3.6 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2AN series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW2AN series of FPGA products provide PLL, high speed clock HCLK, DDR memory interface, DQS, etc.

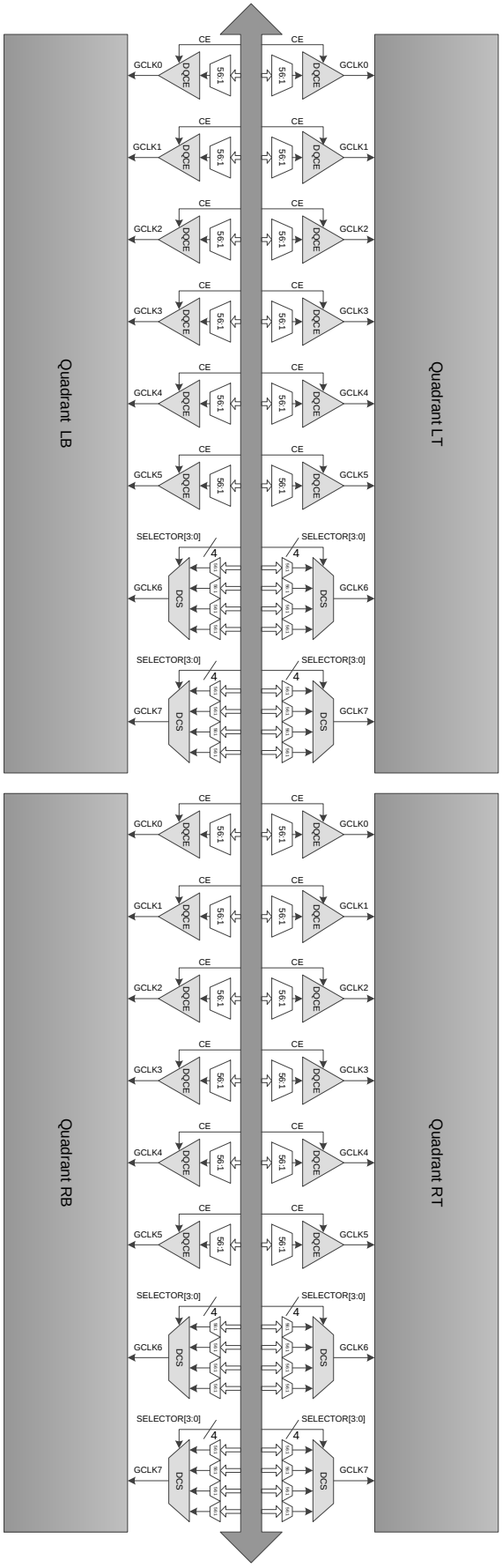
Figure 3-14 GW2AN Clock Resources



3.6.1 Global Clock

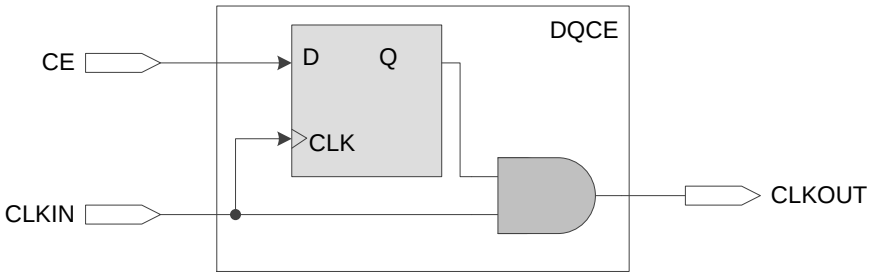
GCLK is distributed in the GW2AN devices as four quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

Figure 3-15 GCLK Quadrant Distribution



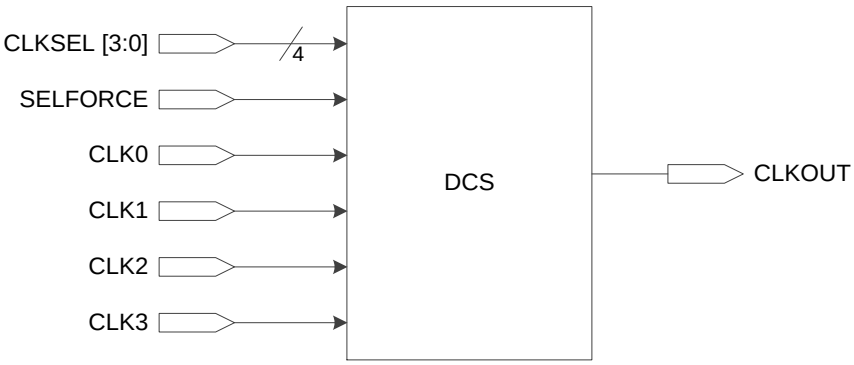
GCLK0~GCLK5 can be turned on or off by Dynamic Quadrant Clock Enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

Figure 3-16 DQCE Concept



GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-17. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

Figure 3-17 DCS Concept

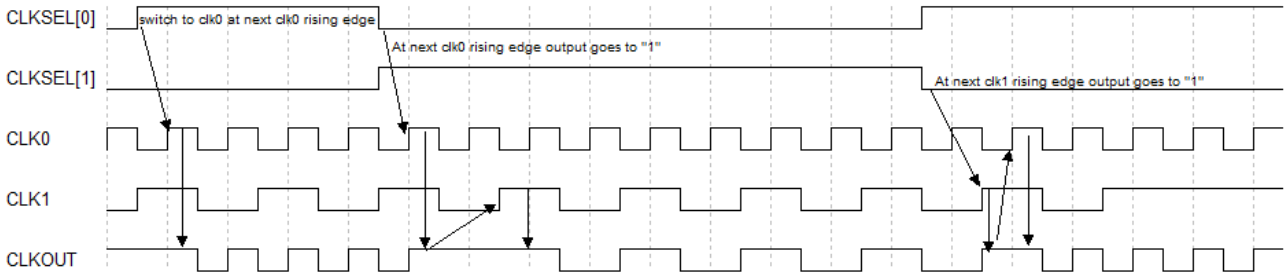


DCS can be configured in the following modes:

- DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-18.

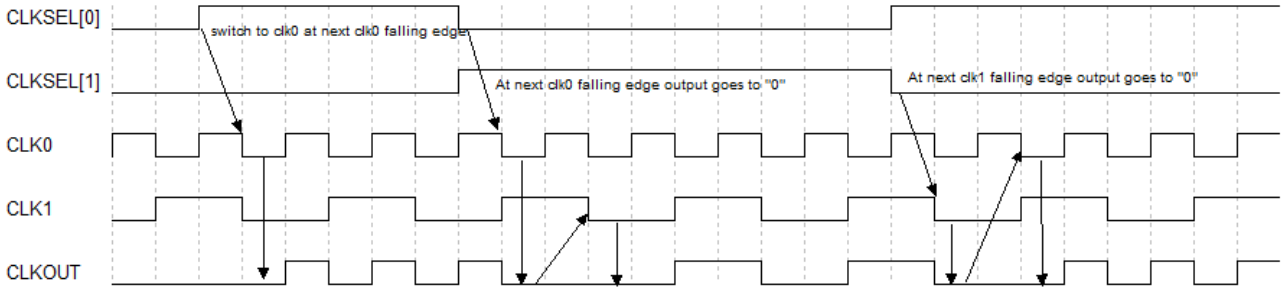
Figure 3-18 DCS Rising Edge



- DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-19.

Figure 3-19 DCS Falling Edge



- Clock Buffer Mode

In this mode, DCS acts as a clock buffer.

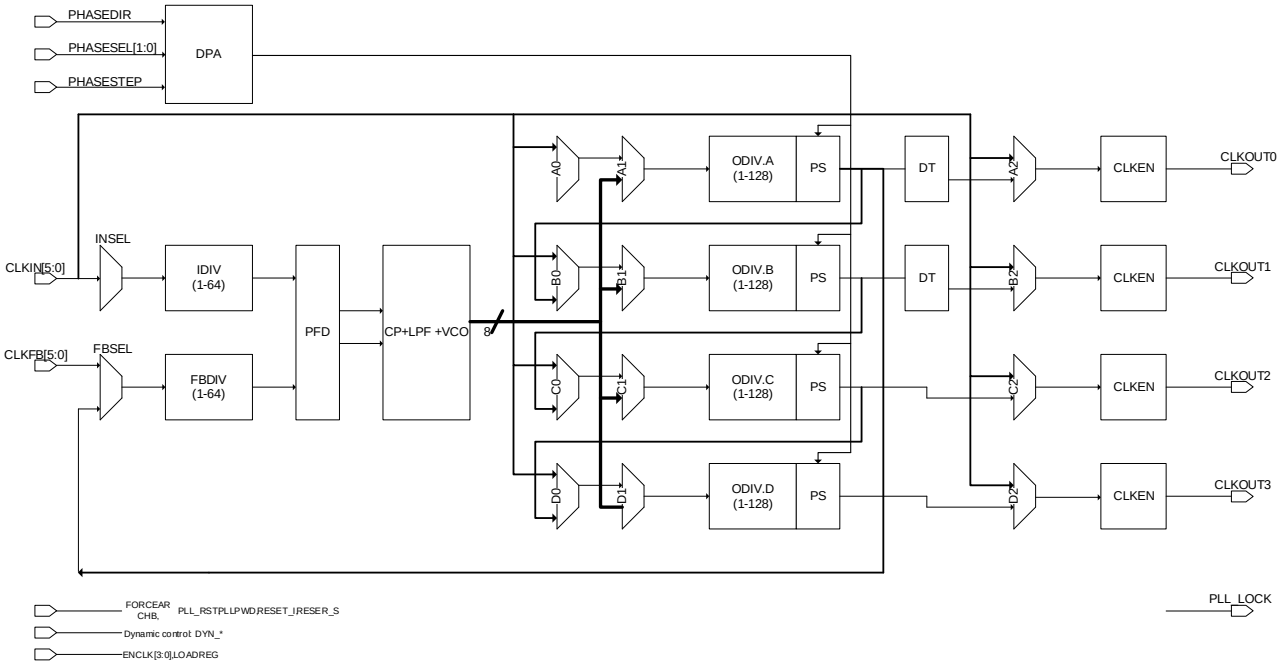
3.6.2 PLL

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks in the GW2AN series of FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-20 for the PLL structure.

Figure 3-20 PLL Structure



See Table 3-8 for a definition of the PLL ports.

Table 3-8 PLL Ports Definition

Port Name	Signal	Description
CLKIN	I	Reference clock input

Port Name	Signal	Description
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
RESET_I	I	PLL with IDIV reset
RESET_S	I	Only channel B/C/D reset
INSEL[2:0]	I	Dynamic clock control selector: 0~5
IDSEL [5:0]	I	Dynamic IDIV control: 0~63
FBDSEL [5:0]	I	Dynamic FBDIV control: 0~63
ODSELA[6:0]	I	Dynamic ODIVA control: 0~127
ODSELB[6:0]	I	Dynamic ODIVB control: 0~127
ODSELC[6:0]	I	Dynamic ODIVC control: 0~127
ODSELD[6:0]	I	Dynamic ODIVD control: 0~127
DTA[3:0]	I	Dynamic fine control of CLKOUTA dutycycle
DTB[3:0]	I	Dynamic fine control of CLKOUTB dutycycle
ICPSEL[4:0]	I	Dynamic control of ICP size
LPFRES[2:0]	I	Dynamic control LPFRES size
PSPULSE	I	Dynamic control of phase shift direction
PSSEl[1:0]	I	Dynamic control of phase shift channel selection
PSPULSE	I	Dynamic control of phase shift clock
ENCLKA ENCLKB ENCLKC ENCLKD	O	Dynamic control of clock output enable
CLKOUTA	O	Clock output of Channel A
CLKOUTB	O	Clock output of Channel B
CLKOUTC	O	Clock output of Channel C
CLKOUTD	O	Clock output of Channel D
LOCK	O	PLL lock status: 1: locked, 0: unlocked

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

For further PLL features, please refer to 4.4.6 PLL Switching Characteristic.

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1. **fCLKOUTA = (fCLKIN*FBDIV)/IDIV**
2. **fVCO = fCLKOUTA*ODIVA**
3. **fCLKOUTx = fIN_ODIVx/ODIVx**
4. **fPFD = fCLKIN/IDIV=fCLKOUTA/FBDIV**

Note!

- fCLKIN: The frequency of the input clock CLKIN
- fCLKOUTx: The output clock frequency of channel X, x=A/B/C/D.
- ODIVx: The Output frequency division coefficient of channel X, x=A/B/C/D.

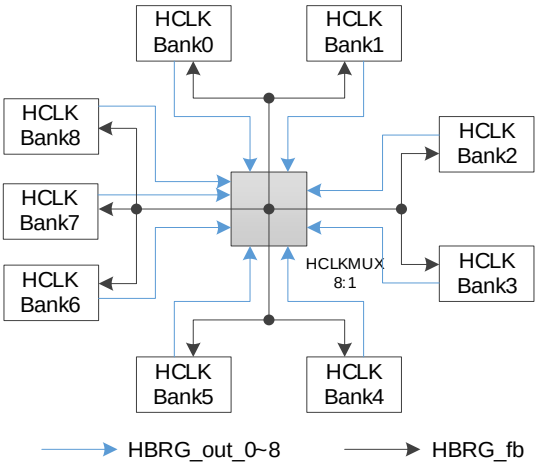
- fIN_ODIVx: The input clock frequency of ODIVx, x=A/B/C/D, and fvco is defaulted. It's determined by the actual circuit if the Chanel is cascaded.
- fPFD: PFD Phase Comparison Frequency, and the minimum value of fPFD should be no less than 3MHz.

Adjust IDIV, FBDIV, and ODIV to achieve the required clock frequency.

3.6.3 HCLK

HCLK is the high-speed clock in the GW2AN series FPGA products, which can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-21.

Figure 3-21 GW2AN HCLK Distribution



As shown in Figure 3-21, there is an 8: 1 HCLKMUX module in the middle of the high-speed clock HCLK. HCLKMUX can send HCLK clock signal from any Bank to any other bank, which makes the use of HCLK more flexible.

HCLK can provide user with the function modules as follows:

- DHCEN: Dynamic high-speed clock enable module, functions similar to DQCE. Dynamically turn on / off high-speed clock signal.
- CLKDIV/ CLKDIV2: high-speed clock divider module, each clock bank has a CLKDIV. Generates a clock divided by the input clock phase, which is used in the IO logic mode.
- DCS: Dynamic Global Clock Selector.
- DLLDLY: The dynamic delay adjustment module, the clock signal for the dedicated clock pin input.

3.6.4 DDR Memory Interface Clock Management DQS

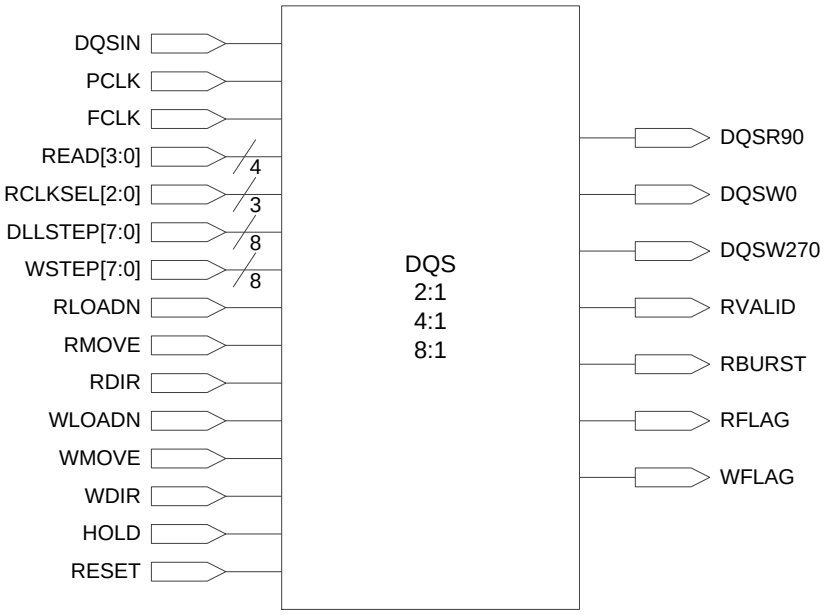
The DQS module of the GW2AN series of FPGA products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase

- Provide a read / write pointer for input cache
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module has three operating modes to meet the needs of different I/O interfaces, as shown in Figure 3-22.

Figure 3-22 DQS



CDRCLKGEN

CDRCLKGEN is used to support high-speed asynchronous input interfaces, such as SGMII. Each location has only one DQS and CDRCLKGEN.

CDRCLKDIV

The function of the clock divider module is similar to that of HCLKDIV.

3.7 Long Wire (LW)

As a supplement to the CRU, the GW2AN series of FPGA products provide another routing resource - Long Wire, which can be used as clock, clock enable, set/reset, or other high fan out signals.

3.8 Global Set/Reset (GSR)

A global set/rest (GSR) network is built into the GW2AN series of FPGA products. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

3.9 Programming and Configuration

The GW2AN series of FPGA products support SRAM configuration. Each time the device is powered on, it needs to download the bit stream file to configure. Users can select to keep the configuration data in embedded or external Flash chip according to requirements. After power-up, the GW2AN devices read the configuration data from the embedded or external Flash and write into SRAM.

Besides JTAG, the GW2AN series of FPGA products also support GOWINSEMI's own configuration mode: GowinCONFIG (Autoboot, SSPI, CPU, I²C, SERIAL). For more detailed information, please refer to *UG702, GW2AN-18X & 9X Programming and Configuration User Guide*.

3.9.1 I²C Timing Characteristics

Note!

- SDA pin is not open-drain;
- supports point-to-point applications;
- supports multiple chips of the same series accessing the bus at the same time and completing the configuration through broadcast.

Figure 3-23 I²C Timing Diagram

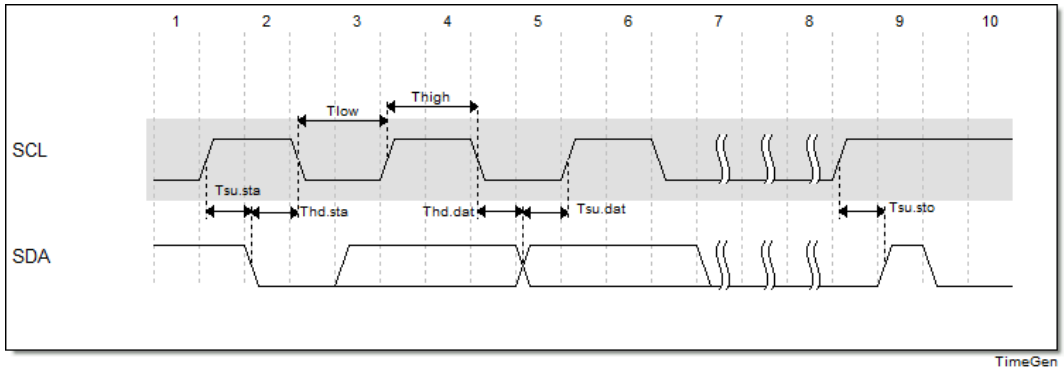


Table 3-9 I²C Timing Requirements for GW2AN-18X and GW2AN-9X

Symbol	Parameter	Min	Max	Unit
F_{SCL}	Clock Frequency	-	400	kHz
T_{low}	LOW period of the SCL	1.3	-	us
T_{high}	HIGH period of the SCL	0.6	-	us
$T_{hd.sta}$	Start Hold Time	0.6	-	us
$T_{su.sta}$	Start Setup Time	0.6	-	us
$T_{hd.dat}$	Data In Hold Time	80[1]	-	ns
$T_{su.dat}$	Data In Setup Time	500[1]	-	ns
$T_{su.sto}$	Stop Setup Time	0.6	-	us

Note!

- [1]: $T_{hd.dat}$ & $T_{su.dat}$ exceed the I²C specification.

3.10 On Chip Oscillator

There is an internal oscillator in each of the GW2AN series of FPGA product. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-10 for the output frequency. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formual is employed to get the output clock frequency:

f_{out}=200 MHz/Param

Note!

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

Table 3-10 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2MHz[1]	8	6.25MHz	16	12.5MHz
1	4.3MHz	9	6.7MHz	17	14.3MHz
2	4.5MHz	10	7.1MHz	18	16.7MHz
3	4.8MHz	11	7.7MHz	19	20MHz
4	5.0MHz	12	8.3MHz	20	25MHz
5	5.3MHz	13	9.1MHz	21	33.3MHz
6	5.6MHz	14	10MHz	22	50MHz
7	5.9MHz	15	11.1MHz	23	100MHz

Note!

[1] Default Frequency is 2 MHz.

4 AC/DC Characteristic

Note!

Users should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

4.1 Operating Conditions

4.1.1 Absolute Max. Ratings

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	LV Core voltage	-0.5V	1.1V
	EV Core voltage	-0.5V	1.32V
	UV Core voltage	-0.5V	3.75V
V_{CCO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
-	I/O Voltage Applied[1]	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65 ℃	+150 ℃
Junction Temperature	Junction Temperature	-40 ℃	+125 ℃

Note!

[1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions[1]

Name	Description	Min.	Max.
V_{CC}	LV Core voltage	0.95V	1.05V
	EV Core voltage	1.14V	1.26V
	UV Core voltage	2.375V	3.6V
V_{CCO}[2]	I/O Bank Power	1.14V	3.6V
V_{CCX}	Auxiliary voltage	2.7V	3.6V
T_{JCOM}	Junction temperature of commercial operation	0 ℃	+85 ℃
T_{JIND}	Junction temperature of Industrial operation	-40 ℃	+100 ℃

Note!

- [1] For the detailed recommended operating conditions for different packages, please refer to UG972, GW2AN-18X Pinout, UG978, GW2AN-9X Pinout .
- [2] When the V_{CCO5} voltage is less than 2.0V, the static current of V_{CCO5} will increase by about 20mA.

4.1.3 Power Supply Ramp Rates

Table 4-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
T_{RAMP}	Power supply ramp rates for all power supplies	0.1mV/μs	-	10mV/μs

4.1.4 Hot Socket Specifications

Table 4-4 Hot Socket Specifications

Name	Description	Condition	I/O	Max.
I_{HS}	Input leakage current (Input or I/O leakage current)	$V_{IN}=V_{IL}$ (MAX)	I/O	150uA
I_{HS}	Input leakage current (Input or I/O leakage current)	$V_{IN}=V_{IL}$ (MAX)	TDI, TDO TMS,TCK	120uA

4.1.5 POR Specifications

Table 4-5 POR Specifications

Name	Description	Device	Name	Value
VPOR_UP	Power on reset ramp up trip point	GW2AN-9X	VCC	TBD
			VCCX	TBD
			VCCO	TBD
		GW2AN-18X	VCC	0.78V
			VCCX	1.9V
			VCCO	0.95V
VPOR_DOWN		GW2AN-9X	VCC	TBD
			VCCX	TBD

Name	Description	Device	Name	Value
	Power on reset ramp down trip point		VCCO	TBD
		GW2AN-18X	VCC	0.63V
			VCCX	1.3V
			VCCO	0.65V

4.2 ESD

Table 4-6 GW2AN ESD - HBM

Device	GW2AN-18X	GW2AN-9X
UG256	HBM>1,000V	HBM>1,000V
UG332	HBM>1,000V	-
UG324	HBM>1,000V	HBM>1,000V
UG400	HBM>1,000V	HBM>1,000V
UG484	HBM>1,000V	HBM>1,000V -
PG256	HBM>1,000V	HBM>1,000V

Table 4-7 GW2AN ESD - CDM

Device	GW2AN-18X	GW2AN-9X
UG256	CDM>500V	CDM>500V
UG332	CDM>500V	-
UG324	CDM>500V	CDM>500V
UG400	CDM>500V	CDM>500V
UG484	CDM>500V	CDM>500V
PG256	CDM>500V	CDM>500V

4.3 DC Electrical Characteristics

4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

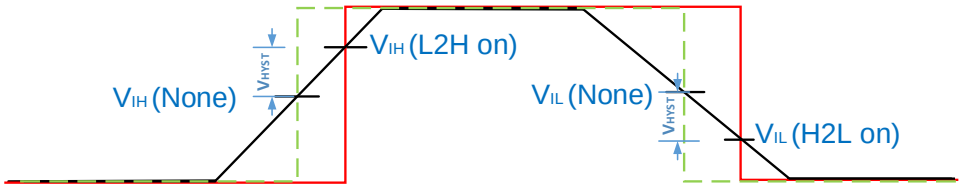
Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	I/O Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$(MAX)	-	-	210μA
		$0V<V_{IN}<V_{CCO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCO}$	-30μA	-	-150μA
I_{PD}	I/O Active Pull-down Current	V_{IL}(MAX)$<V_{IN}<V_{CCO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$(MAX)	30μA	-	-
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCO}$	-30μA	-	-

Name	Description	Condition	Min.	Typ.	Max.
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCO}$	-	-	150μA
I_{BHHO}	BusHoldHigh Overdrive Current	$0 \le V_{IN} \le V_{CCO}$	-	-	-150μA
V_{BHT}	Bus hold trip points	-	V_{IL}(MAX)	-	V_{IH}(MIN)
C1	I/O Capacitance	-	-	5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCO}=3.3V, Hysteresis=L2H[1],[2]	-	240mV	-
		V_{CCO}=2.5V, Hysteresis=L2H	-	140mV	-
		V_{CCO}=1.8V, Hysteresis=L2H	-	65mV	-
		V_{CCO}=1.5V, Hysteresis=L2H	-	30mV	-
		V_{CCO}=3.3V, Hysteresis=H2L[1],[2]	-	200mV	-
		V_{CCO}=2.5V, Hysteresis=H2L	-	130mV	-
		V_{CCO}=1.8V, Hysteresis=H2L	-	60mV	-
		V_{CCO}=1.5V, Hysteresis=H2L	-	40mV	-
		V_{CCO}=3.3V,Hysteresis=HIGH[1],[2]	-	440mV	-
		V_{CCO}=2.5V,Hysteresis=HIGH	-	270mV	-
		V_{CCO}=1.8V,Hysteresis=HIGH	-	125mV	-
		V_{CCO}=1.5V,Hysteresis=HIGH	-	70mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(L2H). The diagram is shown below.



4.3.2 Static Supply Current

Table 4-9 Static Supply Current

Device	Name	Description	Device type	C8/I7	C7/I6
				Typ.	Typ.
GW2AN-LV9X GW2AN-LV18X	I_{CC}	Core Current (V_{CC}=1.0V)	LV	-	30mA
	I_{CCX}	V_{CCX} Current (V_{CCX}=3.3V)	LV	-	12mA
	I_{CCO}[1]	I/O Bank Current (V_{CCO}=2.5V)	LV	-	1mA
GW2AN-UV9X GW2AN-UV18X	I_{CC}+I_{CCX}	V_{CCX} Current and Core Current (V_{CCX}= V_{CC}=3.3V)	UV	-	46mA
	I_{CCO}[1]	I/O Bank Current (V_{CCO}=2.5V)	UV	-	2mA

Note!

When the V_{CCO5} voltage is less than 2.0V, the static current of V_{CCO5} will increase by about 20mA.

4.3.3 I/O Operating Conditions Recommended

Table 4-10 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Note!

It is recommended to set the V_{CCO} of the Bank using TrueLVDS to 2.5V.

4.3.4 IOB Single - Ended DC Electrical Characteristic

Table 4-11 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							4	-4
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Note!

The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents

the number of IOs bonded out from a bank.

4.3.5 IOB Differential Electrical Characteristics

Table 4-12 IOB Differential Electrical Characteristics

LVDS

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage (Input Voltage)		0	-	2.4	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±10	μA
V_{OH}	Output High Voltage for VOP or VOM	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output High Voltage for VOP or VOM	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in VOD Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in VOS Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristic

4.4.1 Internal Switching Characteristics

Table 4-13 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.337	ns
t_{LUT5_CFU}	LUT5 delay	-	0.694	ns
t_{LUT6_CFU}	LUT6 delay	-	1.005	ns
t_{LUT7_CFU}	LUT7 delay	-	1.316	ns
t_{LUT8_CFU}	LUT8 delay	-	1.627	ns
t_{SR_CFU}	Set/Reset to Register output	-	0.93	ns
t_{CO_CFU}	Clock to Register output	-	0.38	ns

4.4.2 BSRAM Internal Timing Parameters

Table 4-14 BSRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	2.55	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.28	ns

4.4.3 Gearbox Switching Characteristics

Table 4-15 Gearbox Internal Timing Parameters

TBD

4.4.4 External Switching Characteristics

Table 4-16 External Switching Characteristics

Name	Description	Device	-8		-7		Unit
			Min	Max	Min	Max	
Pin-LUT-Pin Delay(1)	Pin(IOxA) to Pin(IOxB) delay	GW2AN-18X	-	3.83	-	4.59	ns
$T_{HCLKdly}$	HCLK tree delay	GW2AN-18X	-	0.82	-	0.98	ns
$T_{GCLKdly}$	GCLK tree delay	GW2AN-18X	-	1.77	-	2.12	ns

4.4.5 On chip Oscillator Output Frequency

Table 4-17 On chip Oscillator Output Frequency

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to 85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

4.4.6 PLL Switching Characteristic

Table 4-18 PLL Switching Characteristic

Device	Speed Grade	Name	Min.	Max.
GW2AN-18X	C8/I7	CLKIN	3MHz	500MHz
		PFD	3MHz	500MHz
		VCO	500MHz	1250MHz
		CLKOUT	3.90625MHz	1250MHz
	C7/I6	CLKIN	3MHz	400MHz
		PFD	3MHz	400MHz
		VCO	400MHz	1000MHz
		CLKOUT	3.125MHz	1000MHz
GW2AN-9X	C8/I7	CLKIN	3MHz	500MHz

Device	Speed Grade	Name	Min.	Max.
		PFD	3MHz	500MHz
		VCO	500MHz	1250MHz
		CLKOUT	3.90625MHz	1250MHz
	C7/I6	CLKIN	3MHz	400MHz
		PFD	3MHz	400MHz
		VCO	400MHz	1000MHz
		CLKOUT	3.125MHz	1000MHz

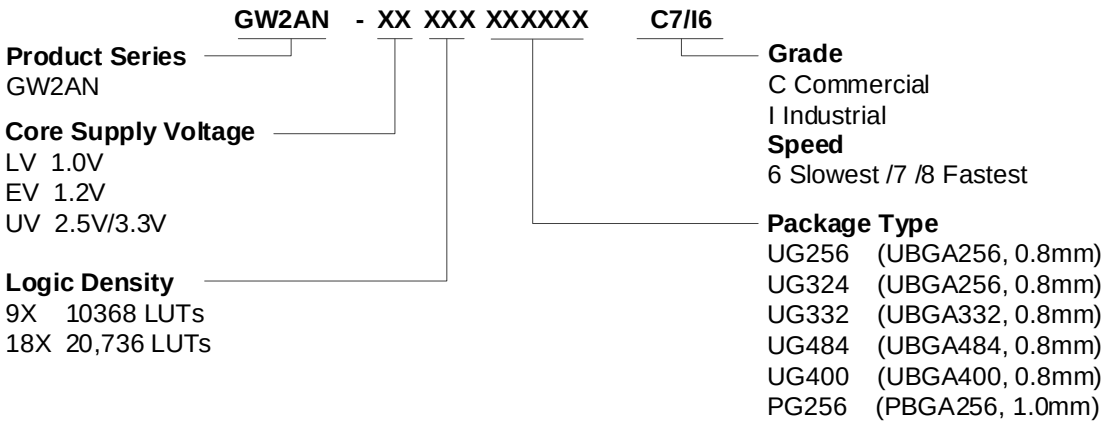
4.5 Configuration Interface Timing Specification

The GW2AN series of FPGA products GowinCONFIG support the following configuration modes: MSPI, SSPI, CPU, and SERIAL. For detailed information, please refer to *UG702, GW2AN-18X & 9X Programming and Configuration User Guide*.

5 Ordering Information

5.1 Part Name

Figure 5-1 Part Naming Example– Production



Note!

- For further information of Package type and pin number, please refer to 2.2 Product Resources.
- The LittleBee® family devices and Arora family devices of the same speed level may have different speed.
- Both “C” and “I” are used in GOWIN part name marking for one same device. GOWIN devices are screened using industrial standards, so one device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets the speed level 7 in commercial grade applications, the speed level is 6 in industrial grade applications.

5.2 Package Mark Example

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-2.

Figure 5-2 Package Mark Example

Note!

The first two lines in the right figure above are the “Part Number”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