SPECIFICATION
FOR
CTP+LCD Module
KD030FM-1-C003A

MODULE:	**KD030FM-1-C003A**
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2016.04.13

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Data	Rev. No.	Page	Summary
2016.04.13	V1.0	ALL	FIRST ISSUE

Contents

General Description

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorp hous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.0'TFT-LCD contains 240x400 pixels, and c an display up to 65K/262K colors.

*** Features**

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

-RGB Interface: 8/9/16/18-bit MCU

3-SPI+16/18-bit RGB 4-SPI+16/18-bit RGB

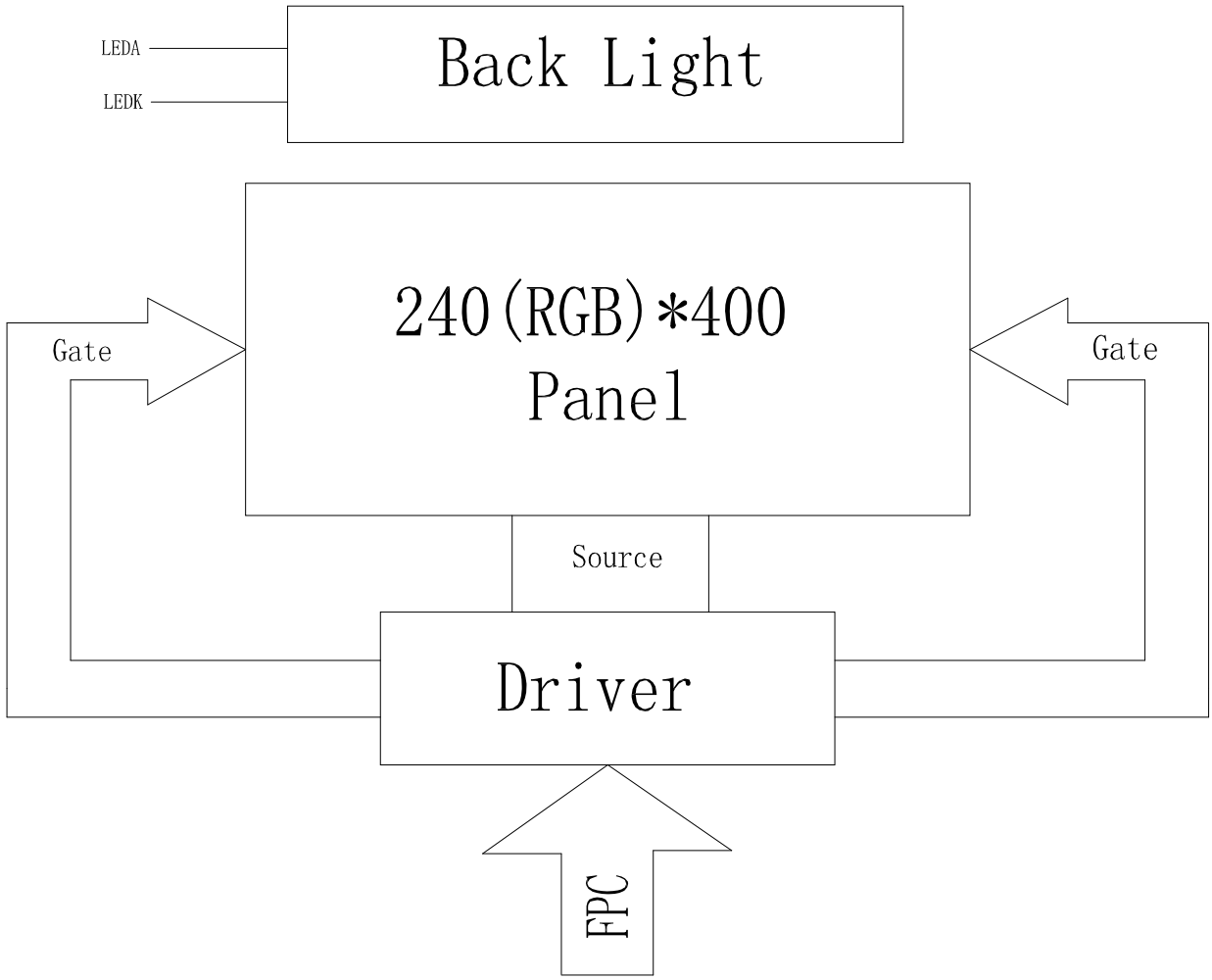
-CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	39.24(H)*65.40(V) (3.0inch)	mm	-
CTP View area	39.54(H)*66.00(V)	mm	
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*400	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1635(H)*0.1635(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9327	-	-
CTP Driver IC	FT6336G		
Simultaneous Touch Points	Single point and Gestures		
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

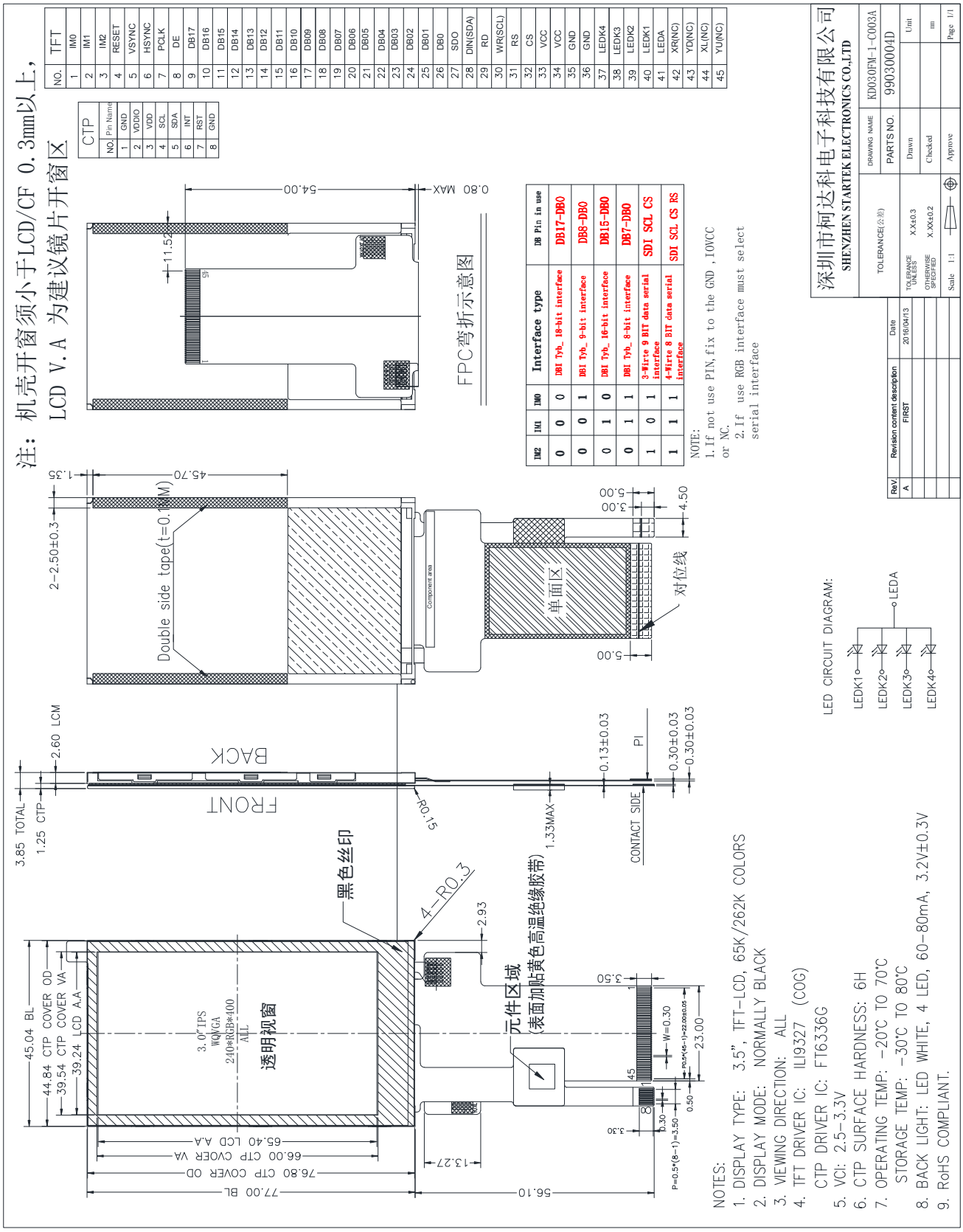
*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		45.04		mm	-
	Vertical(V)		77.00		mm	-
	Depth(D)		3.85		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



NO.	CTP
NO.	Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NO.	TFT
1	IM0
2	IM1
3	IM2
4	RESET
5	VSYNC
6	HSYNC
7	PCLK
8	DE
9	DB17
10	DB16
11	DB15
12	DB14
13	DB13
14	DB12
15	DB11
16	DB10
17	DB09
18	DB08
19	DB07
20	DB06
21	DB05
22	DB04
23	DB03
24	DB02
25	DB01
26	DB0
27	SDO
28	DIN(SDA)
29	RD
30	WR(SCL)
31	RS
32	CS
33	VCC
34	VCC
35	GND
36	GND
37	LEDK4
38	LEDK3
39	LEDK2
40	LEDK1
41	LEDA
42	XR(NC)
43	YD(NC)
44	XL(NC)
45	YU(NC)

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Typ_ 18-bit interface	DB17-DB0
0	0	1	DBI Typ_ 9-bit interface	DB8-DB0
0	1	0	DBI Typ_ 16-bit interface	DB15-DB0
0	1	1	DBI Typ_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

ReV.	Revision content description	Date
A	FIRST	2016/04/13

TOLERANCE(公差)	DRAWING NAME	KD030FM-1-C003A	
	PARTS NO.	99030004D	
TOLERANCE UNLESS OTHERWISE SPECIFIED	Drawn		Unit
	Checked		mm
X.X±0.3 X.XX±0.2	Approve		Page 1/1
	Scale 1:1		

3. Input terminal Pin Assignment

3.1 TFT

NO.	SYMBOL	Description	
1	IM0	Interface selecting signal.	I
2	M1		
3	IM2		
4	RESET	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active	I
5	VSYNC	Vertical sync. Signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_CS) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
6	HSYNC	Horizontal sync. signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_RS) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
7	PCLK	Pixel clock signal in DPI interface mode. If not used, please fix this pin at GND level.	I
8	DE	Data enable signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_WR) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
9-26	DB17-DB0	These pins are data bus. In MDDI operation, DB[17:9]/S_DB[8:0] can be assigned for the sub-display interface output. In MDDI mode, these pins are output, If they are not used; please let these pins as open. In other mode, these pins are input, If they are not used; please fix these pins as GND.	I/O
27	SDO	Serial data output pin and used for the DBI type C mode.	O
28	DIN	Serial data input pin and used for the DBI type C mode.	I

		If not used, please connect this pin to ground.	
29	RD	Read control pin for the DBI interface. If not used, please connect this pin to VCC.	I
30	WR(SCL)	Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to VCC.	I
31	RS	Display data / Command selection pin D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.	I
32	CS	Chip select input pin ("Low" enable). When it is not used, please fix this pin at VCC.	I
33	VCC	Power supply voltage (VCI=2.5V-3.3V).	P
34	VCC		
35	GND	Ground.	P
36	GND		
37	LEDK4	LED Cathode 4.	P
38	LEDK3	LED Cathode 3.	P
39	LEDK2	LED Cathode 2.	P
40	LEDK1	LED Cathode 1.	P
41	LEDA	LED Anode.	P
42	XR(NC)	NC.	
43	YD(NC)	NC.	
44	XL(NC)	NC.	
45	YU(NC)	NC.	

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
*1) Threshold Voltage	Vsat	3.7	3.8	3.9	V	Fig.2
	Vth	1.9	2.0	2.1	V	
*1) Transmittance	T(%)	3.86	4.40	-	%	Fig.1
*1) Contrast Ratio	C/R	400	500	-		
*1) Response Time	Tr+Tf	-	35	50	msec	Fig.3
*2) CIE Color Coordinate	Rx	0.640	0.660	0.680		
	Ry	0.297	0.317	0.337		
	Gx	0.240	0.260	0.280		
	Gy	0.555	0.575	0.595		
	Bx	0.121	0.141	0.161		
	By	0.055	0.075	0.095		
	Wx	0.275	0.295	0.315		
	Wy	0.297	0.317	0.337		
*1) Viewing Angle	Θl	-	80	-	Degree	C/R>10 Fig.4
	Θr	-	80	-		
	Θu	-	80	-		
	Θd	-	80	-		

4.2 Measuring Condition

■ Measuring surrounding：dark room

■ Ambient temperature：25±2℃

■ 15min. warm-up time.

4.3 Measuring Equipment

■ FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

FIG. 1 Optical Characteristic Measurement Equipment and Method

Pritchard 880 System

[Test Equipment Set Up]

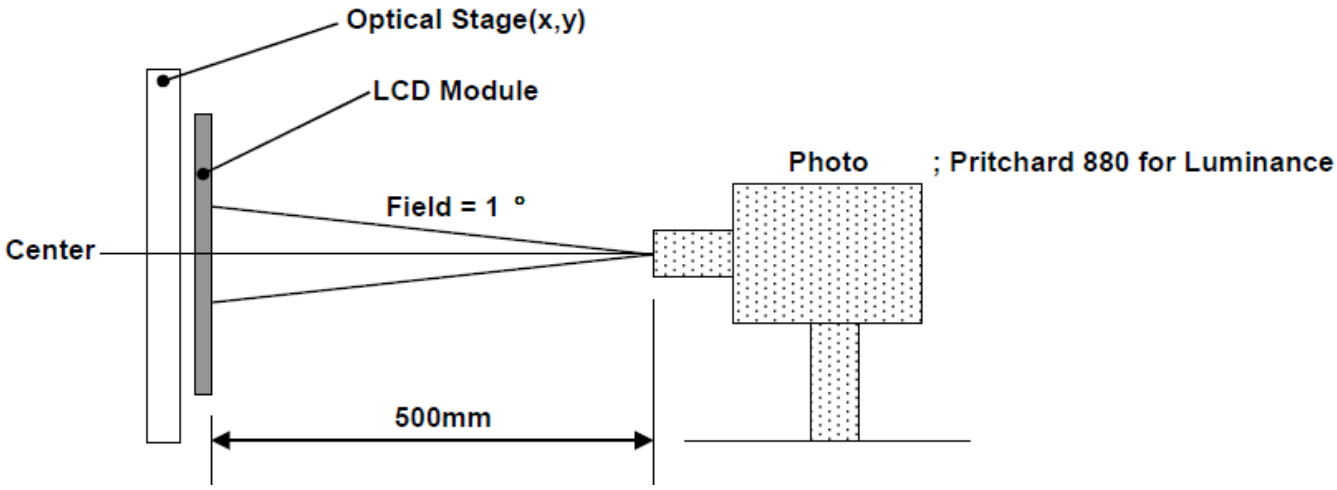


FIG. 2 The definition of Vth and Vsat

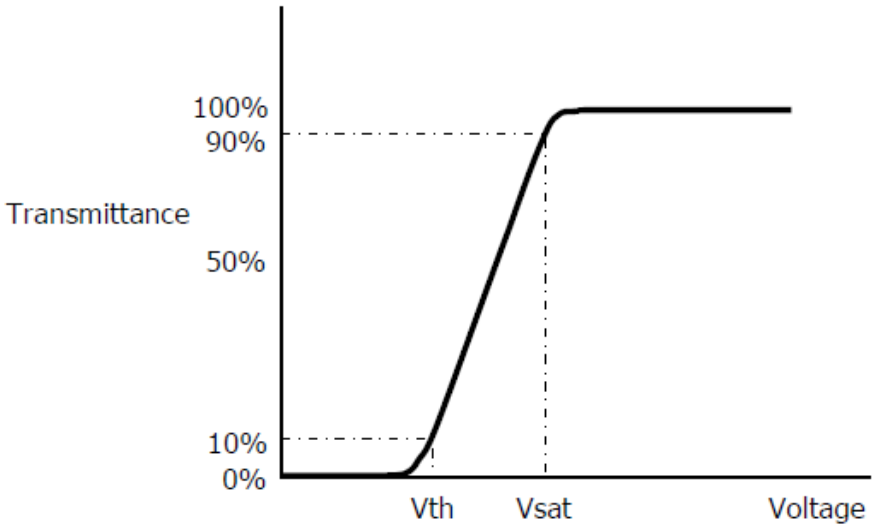


FIG. 4 The definition of viewing angle

<dimension of viewing angle range>

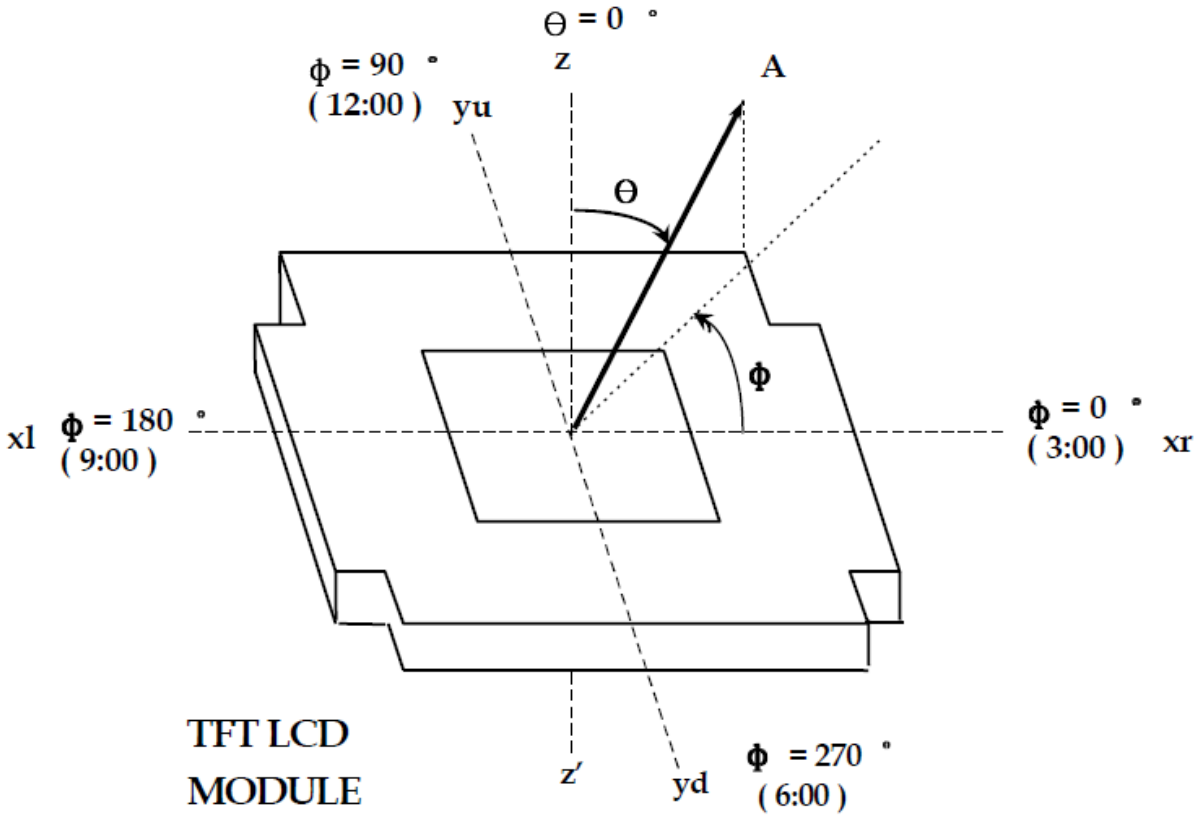
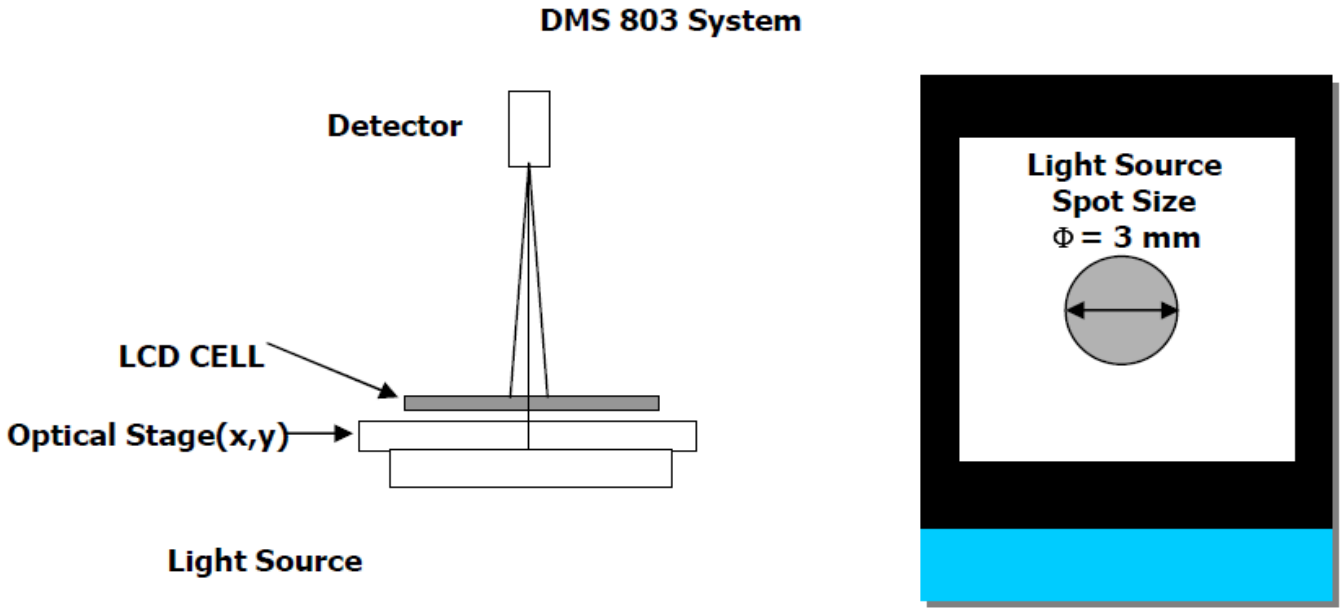


FIG. 5 Response Time Measurement Equipment and Method



<Transmissive Mode>

5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCC	-0.3	4.6	**V**
Digital interface supple Voltage	IOVCC	-0.3	4.6	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCC	2.5	2.8	3.6	V	
Digital interface supple Voltage	IOVCC	1.65	2.8	3.6	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V_{IH}	0.7IOVCC		IOVCC	V	
	V_{IL}	GND		0.3IOVCC	V	
Level output voltage	V_{OH}	0.8IOVCC		IOVCC	V	
	V_{OL}	GND		0.2IOVCC	V	

5.3 LED Backlight Characteristics

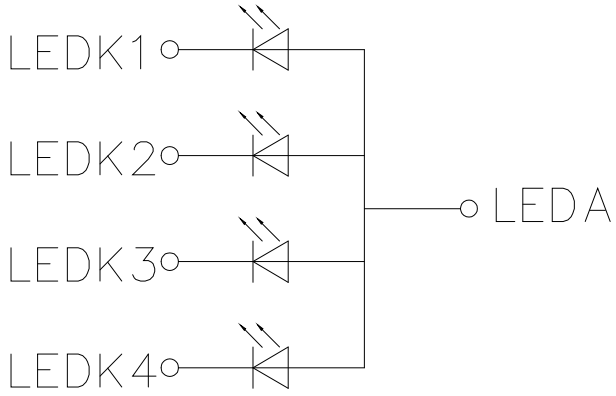
The back-light system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	60	80	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	340		--	cd/m2	I_F =80mA
LED life time	Hr	50000	--	--	Hour	Note1,2

Uniformity	AVg	80	--	--	%	

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

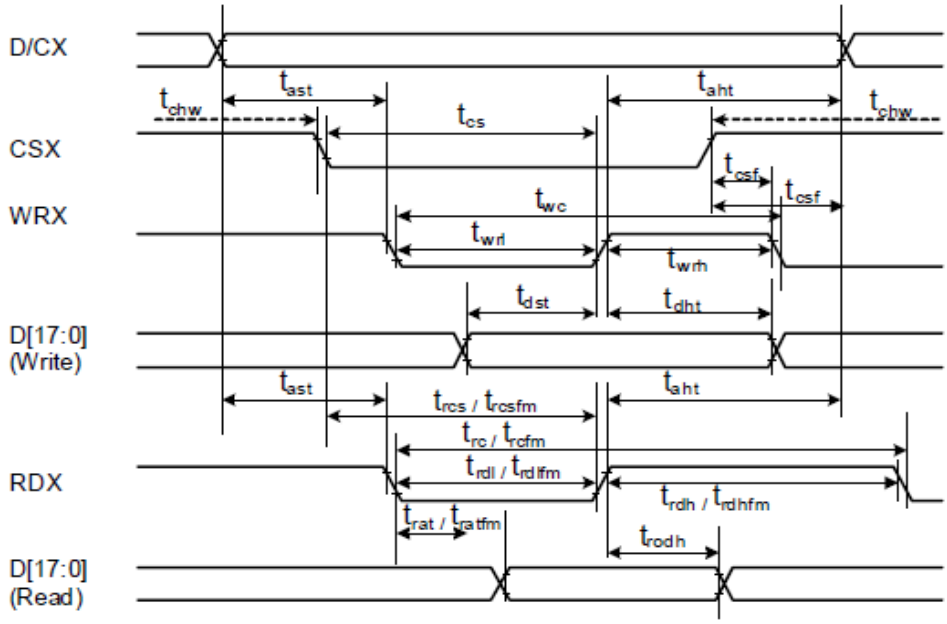
Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



LED CIRCUIT DIAGRAM:

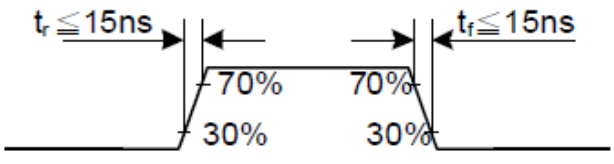
6. TFT AC Characteristic

6.1. Display Parallel Interface Timing Characteristics: 18/16/9/8-bit bus

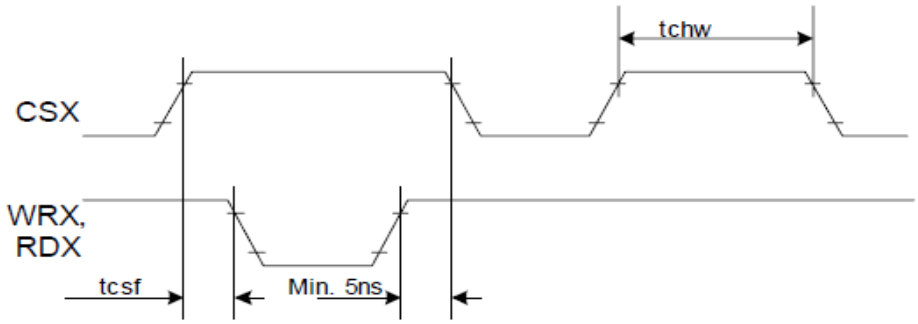


Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" Pulse Width	0	-	ns	
	tcs	Chip Select setup time (Write)	20	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	80	-	ns	
	twrh	Write Control pulse H duration	25	-	ns	
	twrl	Write Control pulse L duration	25	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration (ID)	90	-	ns	
	trdl	Read Control pulse L duration (ID)	45	-	ns	
RDX (FM)	trcfm	Read cycle (FM)	450	-	ns	
	trdhfm	Read Control pulse H duration (FM)	90	-	ns	
	trdlfm	Read Control pulse L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	tdst	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Data hold time	10	-	ns	
	trat	Read access time (ID)	-	40	ns	
	tratfm	Read access time (FM)	-	340	ns	
	todh	Output disable time	20	-	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, DGND=0V

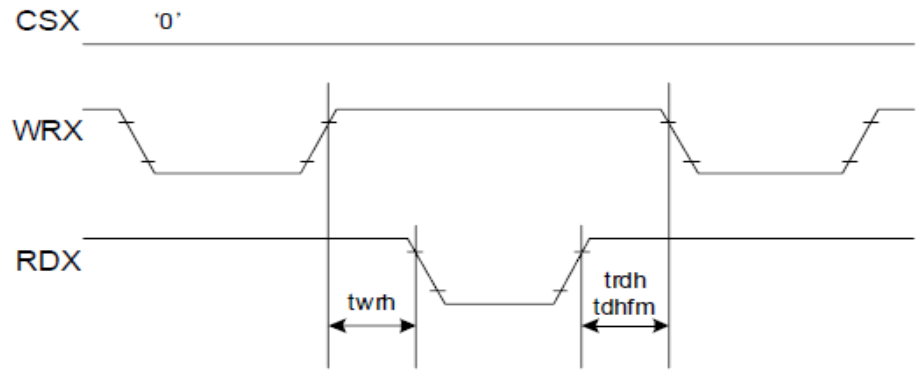


CSX timings:



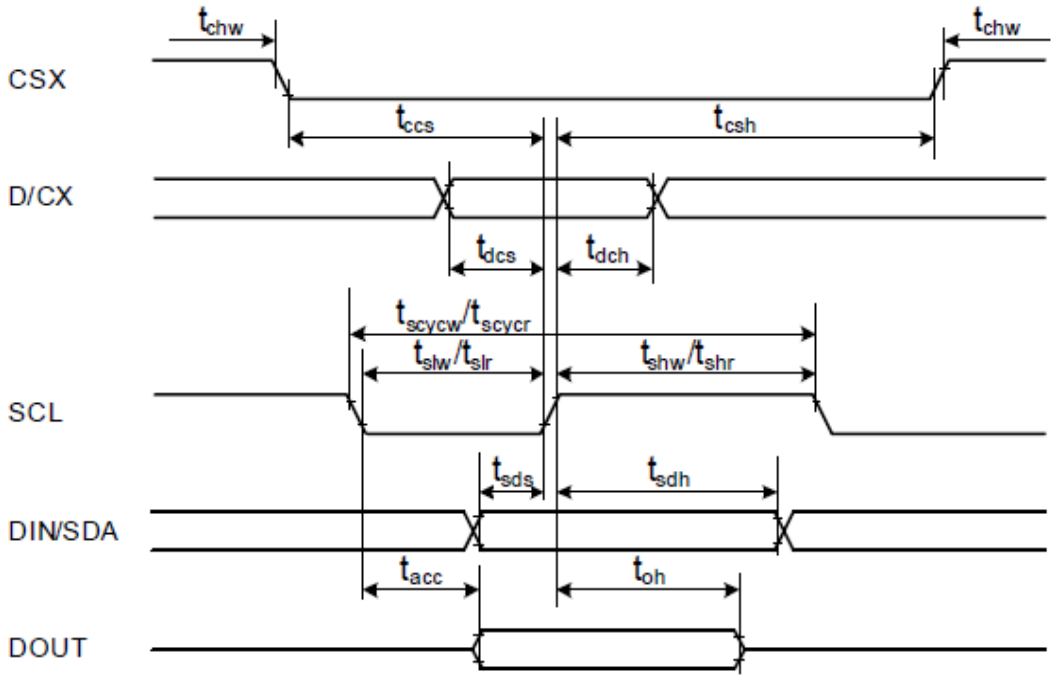
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



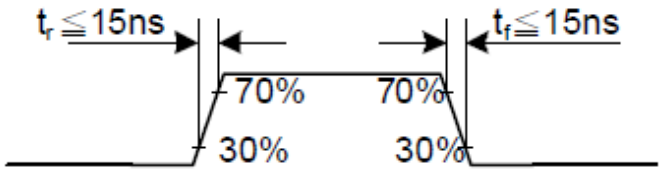
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.2 DBI Type C (SPI) Interface Timing Characteristics

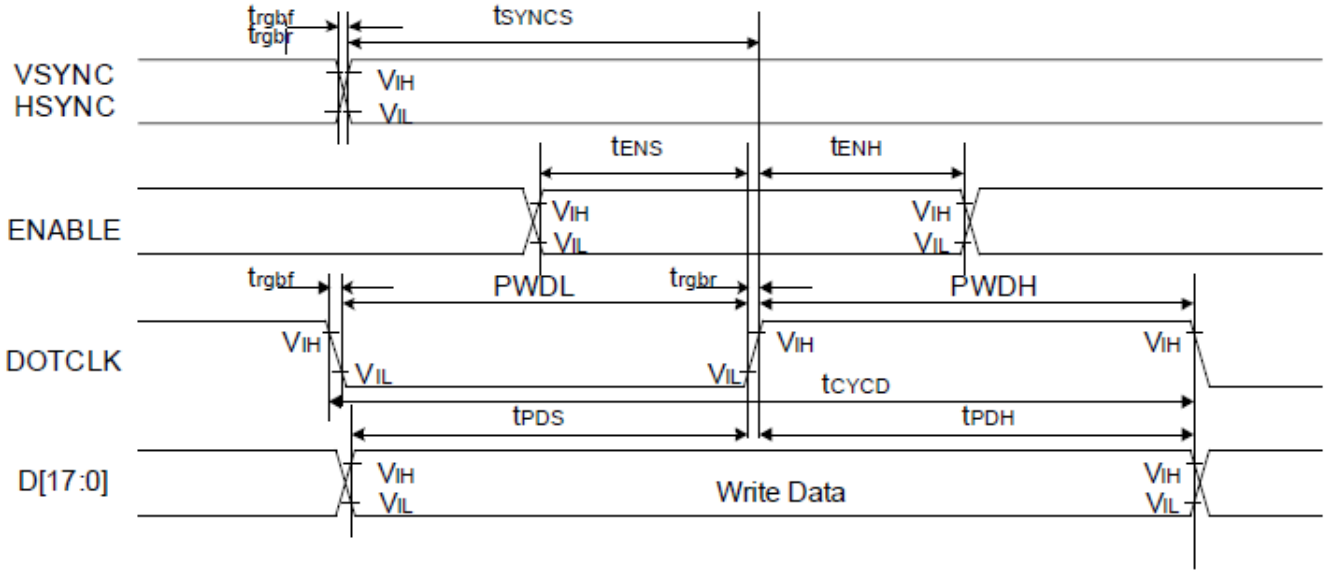


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	CSX-SCL time (Write)	15	-	ns	
	tcsh	CSX-SCL time (Write)	15	-	ns	
	tcss	CSX-SCL time (Read)	60	-	ns	
	tcsh	CSX-SCL time (Read)	60	-	ns	
	tchw	CSX "H" pulse time	40	-	ns	
SCL	tscycw	Serial clock cycle (Write)	60	-	ns	
	tshw	SCL "H" pulse width (Write)	15	-	ns	
	tslw	SCL "L" pulse width (Write)	15	-	ns	
	tscycr	Serial clock cycle (Read GRAM)	300	-	ns	
	tshr	SCL "H" pulse width (Read GRAM)	110	-	ns	
	tslr	SCL "L" pulse width (Read GRAM)	110	-	ns	
	tscycr	Serial clock cycle (Read ID)	150	-	ns	
	tshr	SCL "H" pulse width (Read GRAM)	54	-	ns	
	tslr	SCL "L" pulse width (Read GRAM)	54	-	ns	
D/CX	tdcs	D/CX setup time	7	-	ns	
	tdch	D/CX hold time	7	-	ns	
SDA (Input) (Output)	tacc	Access time	10	50	ns	For maximum CL=30pF
	toh	Output disable time	15	50	ns	For minimum CL=8pF
	tsds	Data setup time	7	-		
	tsdh	Data hold time	7	-		

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V

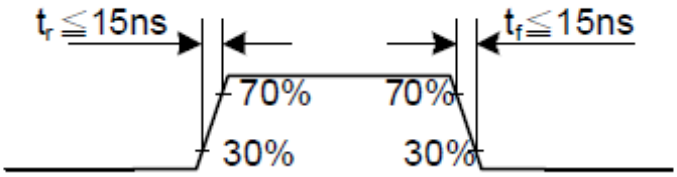


6.3 DPI Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V



6.4 Reset Timing Characteristics

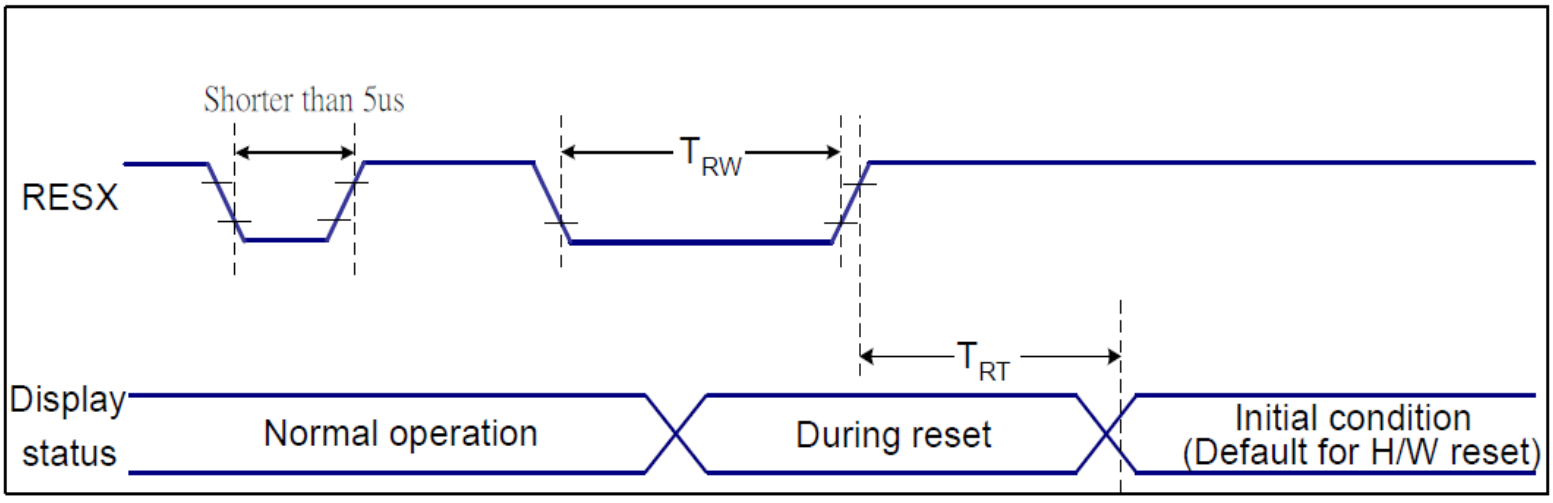


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDDA - VSSA	-0.3 ~ +3.6	V	1, 2
Power Supply Voltage2	VDD3 - VSS	-0.3 ~ +3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.8~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

7.1.2 DC Electrical Characteristics (Ta=25℃)

Table 3-2 DC Characteristics (VDDA=2.8~3.6V, Ta=-40~85℃)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 x IOVCC	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	0.3 x IOVCC	V	
Output high -level voltage	VOH	IOH=-0.1mA	0.7 x IOVCC	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	0.3 x IOVCC	V	
I/O leakage current	ILI	Vin=0~VDDA	-1	-	1	μA	
Current consumption (Normal operation mode)	Iopr	VDDA =VDD3= 2.8V Ta=25℃ MCLK=18MHz	-	4.32*1	-	mA	
Current consumption (Monitor mode)	Imon	VDDA =VDD3= 2.8V Ta=25℃ MCLK=18MHz	-	220*2	-	mA	
Current consumption (Sleep mode)	Islp	VDDA =VDD3= 2.8V Ta=25℃	-	55	-	uA	
Step-up output voltage	VDD5	VDDA = VDD3=2.8V	-	5	-	V	
Power Supply voltage	VDDA VDD3		2.8	-	3.3	V	

*1: Report Rate: 75Hz @ 4"TP

*2: Report Rate: 25Hz @ 4"TP

7.2 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V； Ta=25℃	34.64	36	36.36	MHz	

Table 3-4 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V； Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V； Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V； Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V； Ta=25℃	-	5	-	V	

7.2.1 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure2-4:

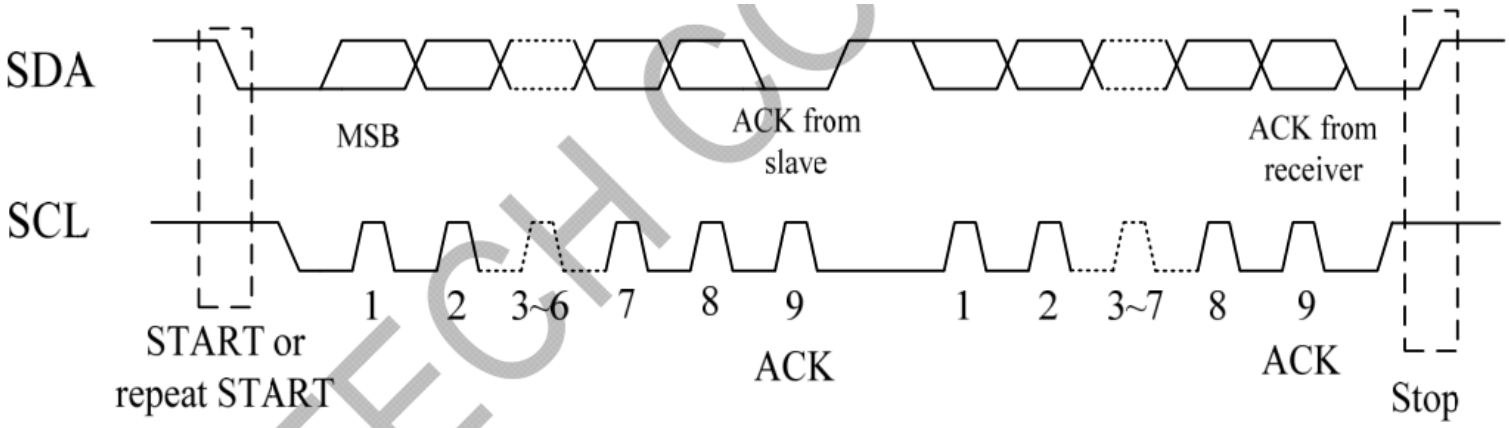


Figure 2-4 I2C Serial Data Transfer Format

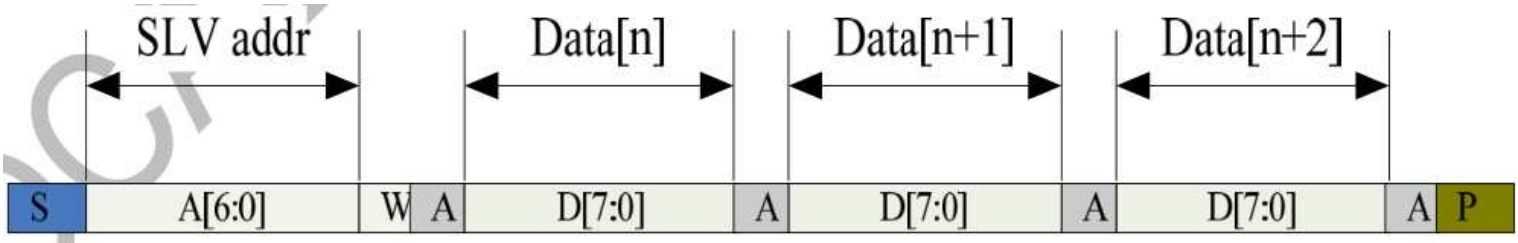


Figure 2-5 I2C master write, slave read

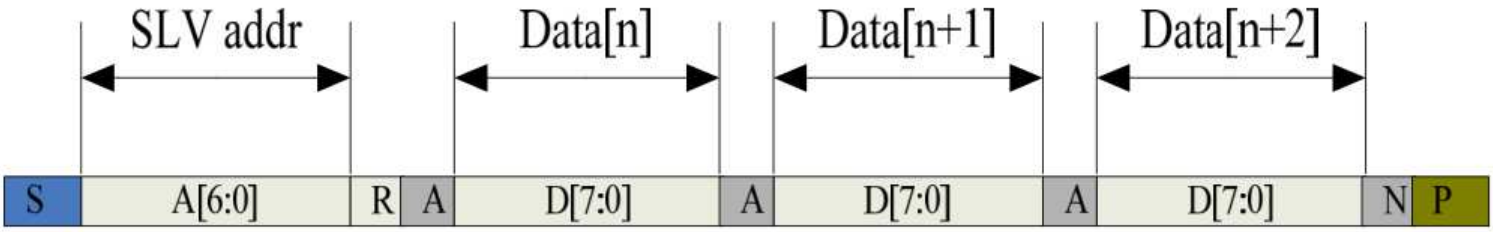


Figure 2-6 I2C master read, slave write

Table2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

Slave Address is 0x38;

I2C Interface Timing Characteristics is shown in Table2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

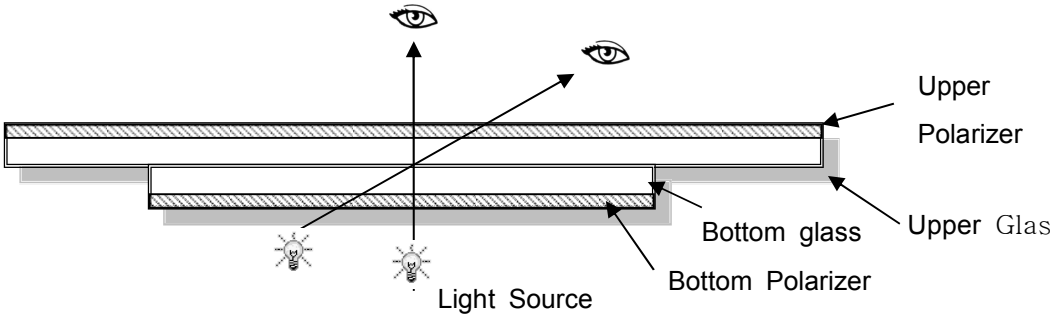
Temperature : 25±5℃

Humidity : 65%±10%RH

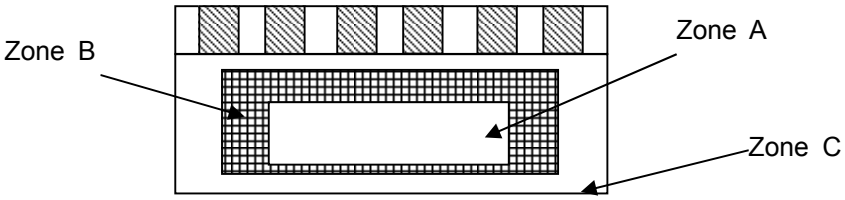
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

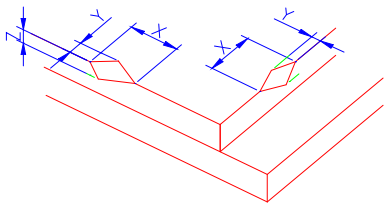
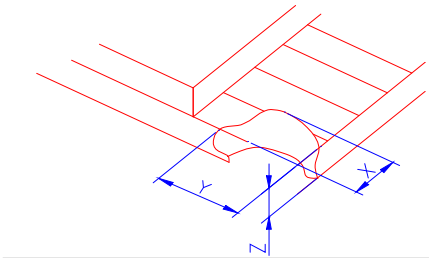
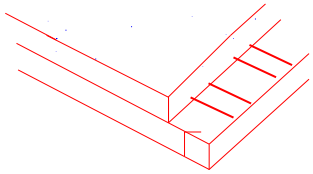
Major defect	Minor defect
0.65	1.5

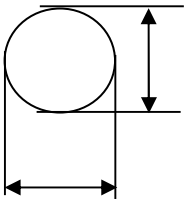
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken

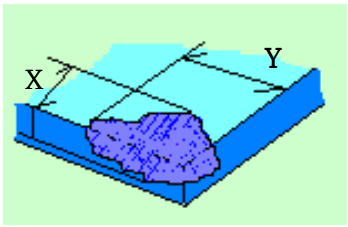
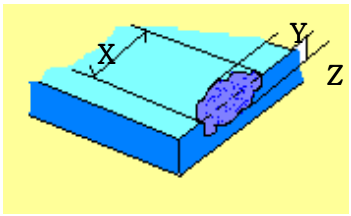
NOTE:
X: Length
Y: Width
Z: Height
L: Length of I TO,
T: Height of L CD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

<table>
<tr><th>Number</th><th>Items</th><th>Criteria (mm)</th></tr>
<tr><td>2.0</td><td>Spot defect
 
Y
X
Φ=(X+Y)/2</td><td>① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.25</td><td colspan="2">0</td></tr>
</table>
②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.20<Φ≤0.30</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.30</td><td colspan="2">0</td></tr>
</table>
③ Polarizer accidented spot
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.3<Φ≤0.5</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table></td></tr>
<tr><td></td><td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td><td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>3.0</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">2</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>SMT</td><td>According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td></tr>
</table>

<table>
<tr><td rowspan="3">5.0</td><td rowspan="3">TP Related</td><td>TP bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.25</td><td colspan="2">3 (distance≧10m</td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td colspan="2">beyond the edge of backlight ≤0.15mm</td></tr>
<tr><td>Newton Ring</td><td>Newton Ring area>1/3 TP area NG
Newton Ring area≤1/3 TP area OK</td><td> 
1.规律性

2.非规律性</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td><td> 
</td></tr>
<tr><td></td><td></td><td>TP corner broken
X：length
Y：width
Z：height</td><td><table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thickness</td></tr></table>*
Circuitry broken is not allowed.</td><td> 
</td></tr>
<tr><td></td><td></td><td>TP edge broken
X：length
Y：width
Z：height</td><td><table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table>* Circuitry broken is not allowed.</td><td> 
</td></tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	－30℃, 96HR	3ea	pass	-
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11.Packing

----TBD----------