Gowin Design Physical Constraints

User Guide

SUG935-1.3.3E, 03/31/2023

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Revision History

Date	Version	Description
05/09/2020	1.0E	Initial version published.
09/04/2020	1.1E	● FloorPlanner menu bar optimized. ● Back-annotate Physical Constraints supported.
06/10/2021	1.2E	The description of the combined use of Port Constraints and Vref Constraints added.
11/02/2021	1.3E	● Some descriptions updated. ● Document structure adjusted.
10/28/2022	1.3.1E	GW1NS-2 removed.
12/16/2022	1.3.2E	● A.10 Other Constraints added. ● VCC modified to VCCIO
03/31/2023	1.3.3E	● Slew Rate setting shielded. ● Find function removed.

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1 About This Guide

1.1 Purpose

This manual describes Gowin FloorPlanner. It introduces the GUI and syntax of FloorPlanner in order to help you add physical constraints to your design. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website: www.gowinsemi.com. You can find the related documents:

- SUG100, Gowin Software User Guide
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- DS102, GW2A series of FPGA Products Data Sheet

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology that are used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
I/O	Input/Output
IDE	Integrated Development Environment
SIP	System in Package

Terminology and Abbreviations	Meaning
VREF	Voltage Reference

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

FloorPlanner is a physical constraints editor and designed in-house by Gowin. It supports reading and editing the attributes and locations of I/O, Primitive, and Group, etc. It also supports the generation of place constraints files according to your configuration. These files define I/O attributes, as well as locations of primitives and modules. FloorPlanner provides easy and fast placement and constraint editing functions to improve the efficiency of writing physical constraint files, and provides timing optimization based on placement information and timing paths.

The functions of FloorPlanner are as follows.

- Supports the input of user design files & constraints files, editing constraints files, and the output of constraints files.
- Supports the display of I/O Port, Primitive and Group constraints in user design files.
- Can create, edit and modify constraints files.
- Supports grid mode, macro cell mode and primitive mode of chip array.
- Supports Package View.
- Can display Chip Array and Package View synchronously.
- Supports real-time display and differences display of constraints locations.
- Can generate locations by dragging.
- Supports I/O port configuration and batch configuration.
- Supports display and editing function of Clock Assignment.
- Supports constraints legality check.
- Supports Back-annotate Physical Constraints.
- Supports manual adjustment of timing.

3 FloorPlanner GUI

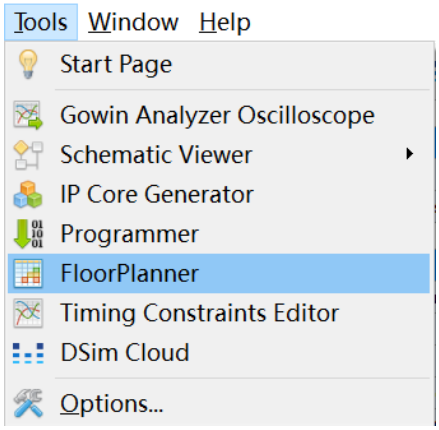
FloorPlanner can create and edit physical constraint files. It supports tabulated constraints editing and efficient netlist lookup so as to improve the efficiency of writing physical constraints files.

3.1 Start FloorPlanner

There are three methods to start FloorPlanner:

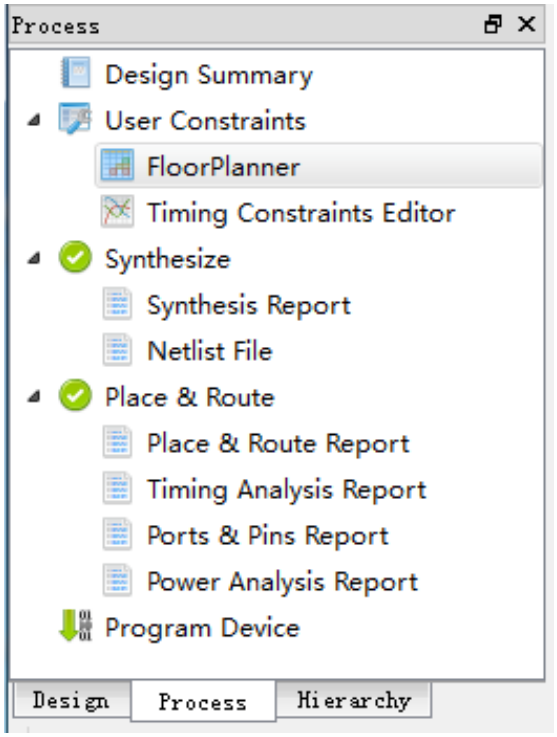
1. Click "IDE > Tools" to open "FloorPlanner", as shown in Figure 3-1.

Figure 3-1 Start FloorPlanner via Menu Bar



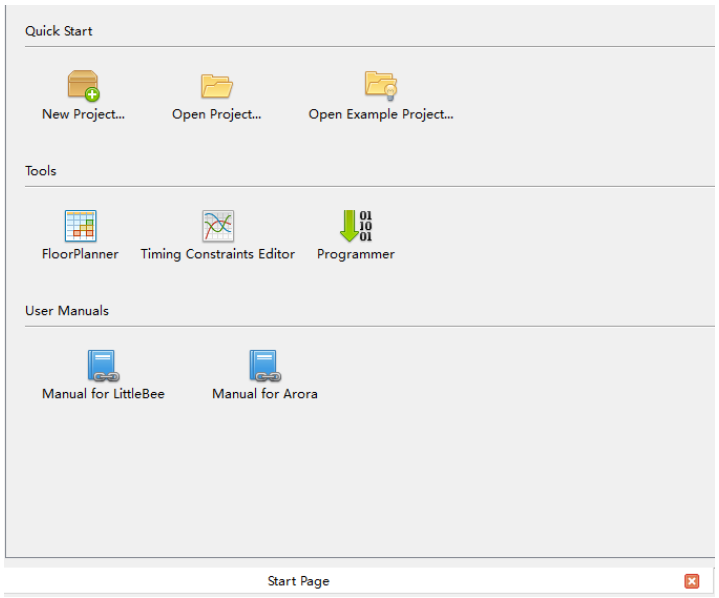
2. After synthesis, Double-click "FloorPlanner" in Process view, as shown in Figure 3-2.

Figure 3-2 Start FloorPlanner in Process View



3. Click "IDE > Start Page>Tools> FloorPlanner" to open FloorPlanner, as shown in Figure 3-3.

Figure 3-3 Start FloorPlanner via Start Page



Note!

- If you use Gowin FloorPlanner for constraints, the netlist file should be added first.
- When you choose the first or the second method to start Gowin FloorPlanner, the netlist file will be loaded automatically.

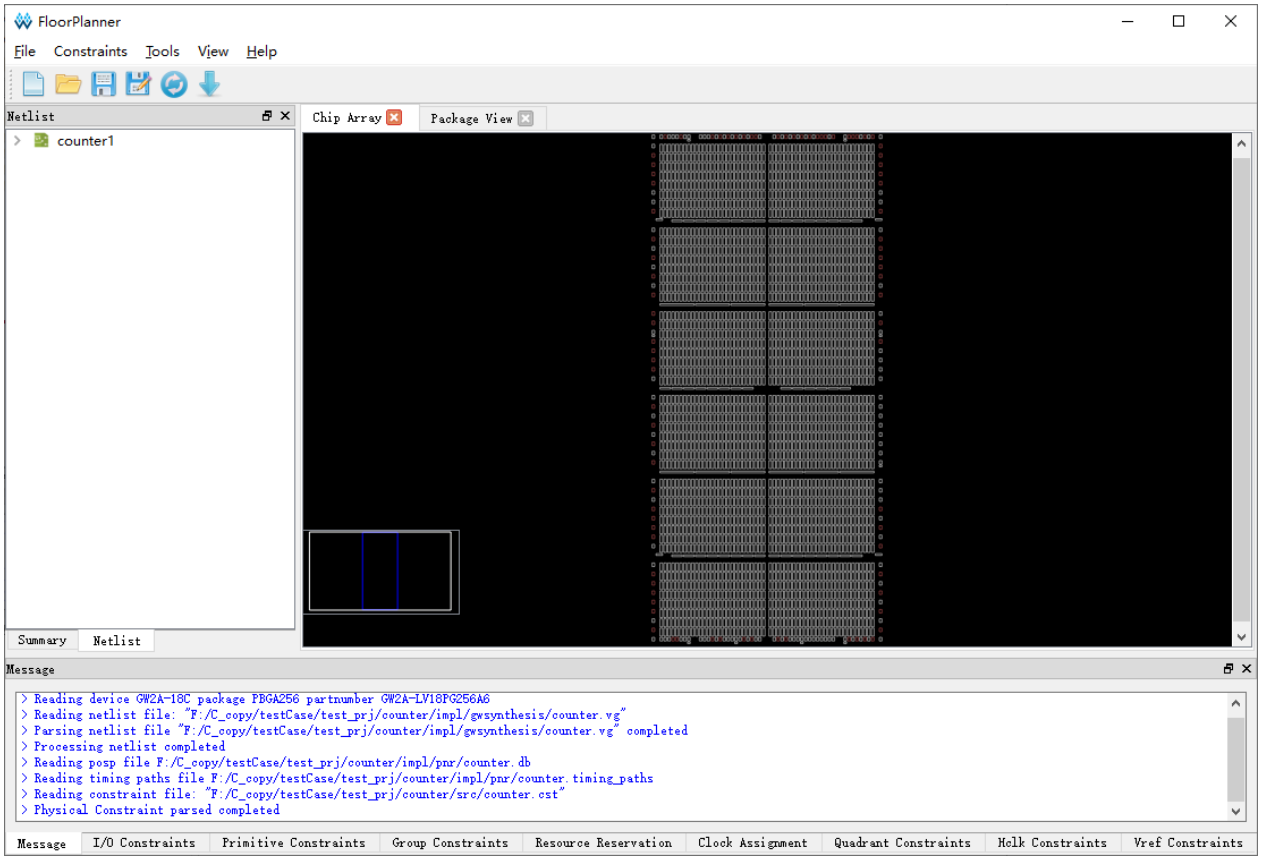
- When you choose the third method to start Gowin FloorPlanner, the netlist file is needed to be loaded via "File > New".

3.2 FloorPlanner Interface

Create or open FloorPlanner interface (including the netlist file), as shown in Figure 3-4.

The interface displays menu, toolbar, Netlist, Project, Chip Array, Package View, and Message, etc.

Figure 3-4 FloorPlanner Interface



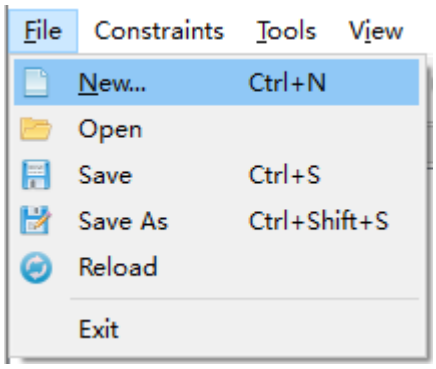
3.2.1 Menu Bar

The menu bar includes "File", "Constraints", "Tools", "View", and "Help".

File Menu

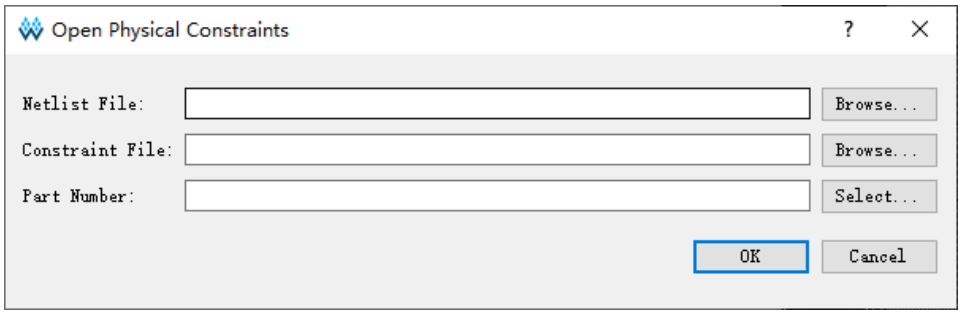
File view is shown in Figure 3-5.

Figure 3-5 File



- New: Create constraints, add user design and select device, etc.
- Open: Open to add constraints, select part number, as shown in Figure 3-6.
- Reload: Physical constraints files, place files and timing path files can be reloaded after modifying.
- Save: Save the modified files.
- Save As: Save the modified file to a specified file and use the netlist name as the name of constraints file, which can be modified.
- Exit: Exit FloorPlanner.

Figure 3-6 Open Physical Constraints

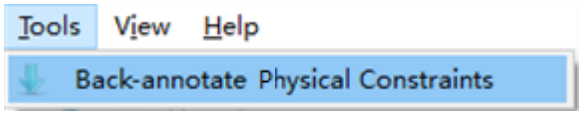


Tools Menu

Tools view is shown in Figure 3-7.

Back-annotate Physical Constraints: Back annotate each primitive and I/O place information to physical constraints file.

Figure 3-7 Tools



1. Click "Tools > Back-annotate Physical Constraints" to open a dialog box, as shown in Figure 3-8. Back-Annotate Physical Constraints is effective only when FloorPlanner is started in the project after Place & Route runs successfully.
2. You can select one or more objects in the Back-annotate Physical Constraints dialog box. Click "OK" to open the "Save as" dialog box and print the place information to the physical constraint file.
3. As shown in Figure 3-9, it is the generated physical constraints file when Port and Port Atrribute selected in Back-annotate Physical Constraints.

Figure 3-8 Back-annotate Physical Constraints

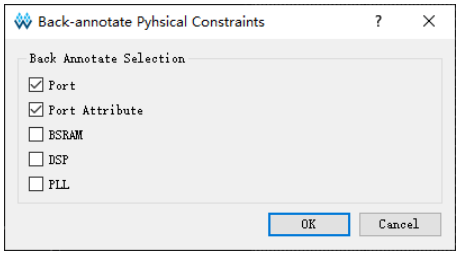
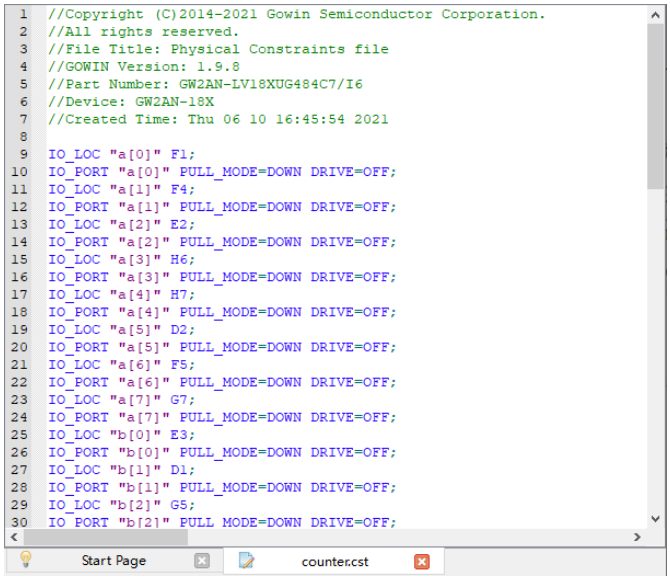


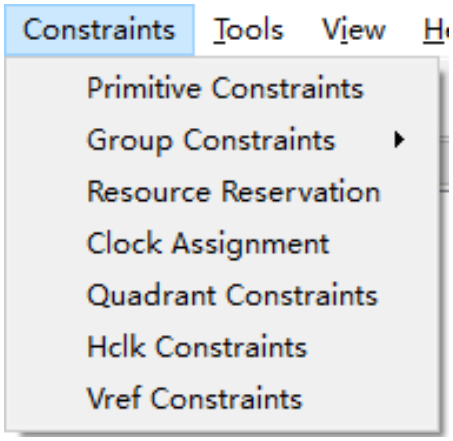
Figure 3-9 Back-annotate Port



Constraints Menu Bar

Constraints menu bar is as shown in Figure 3-10.

Figure 3-10 Constraints



Primitive Constraints

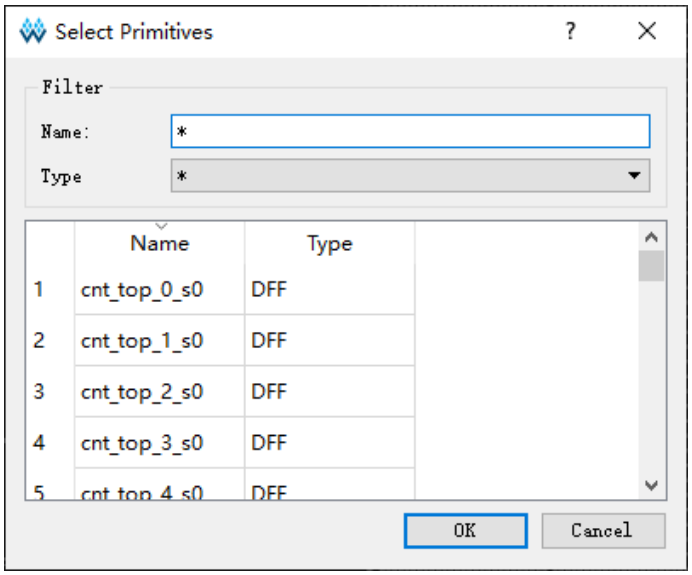
Right-click to select "Select Primitives" and a dialog box pops up, as shown in Figure 3-11.

1. You can select primitives by name or type.
2. Click "OK" to generate the constraints and the constraints are displayed in "Primitive Constraints" at the bottom of main interface.
3. You can set the location by typing or dragging in editing view.

Note!

The location is highlighted in light blue in Chip Array.

Figure 3-11 Primitive Finder



Group Constraints

Group constraints include New Primitive Group and New Relative Group.

Create Primitive Group.

1. Create primitive group. Right-click to select "New Primitive Group" and a dialog box pops up, as shown in Figure 3-12.
2. You can set Group name, Primitives locations and Exclusive. you can add and remove Primitives by clicking "  " and "  " buttons to create a right Primitive Group, as shown in Figure 3-13.

Note!

- Group name, Primitive, and Locations are required.
- Locations can be inputted in the following ways:
  - Manually input
  - Before creating group constraints, copy the location and paste it into "New Primitive Group > Locations" in Chip Array window.

3. After finishing configuration, click "OK", and the syntax of the locations will be checked by the tool.
   - If the location is invalid, a prompt dialog box as Figure 3-14 and Figure 3-15 will pop up. You need to change the location.
   - If there is no error, click "OK", and the available location will be displayed in Chip Array.
4. You can see the created group constraints in "Group Constraints". Double-click the group constraint, and Figure 3-13 pops up; you can edit the constraints.

Figure 3-12 New Primitive Group

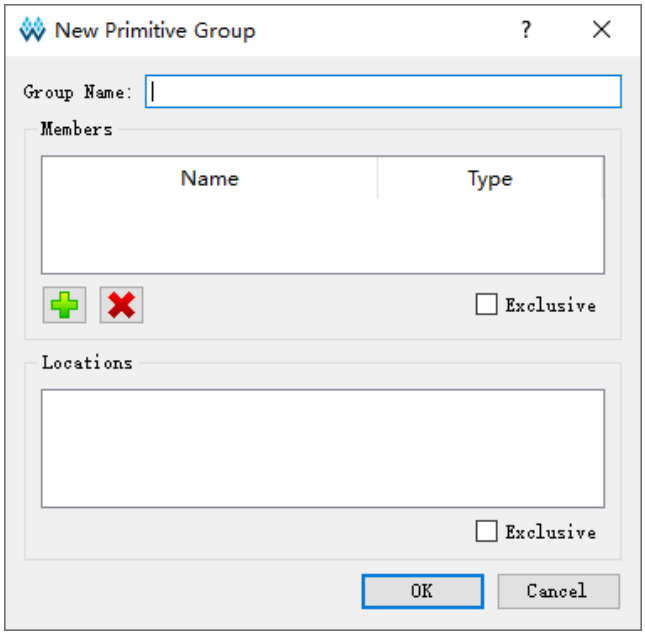


Figure 3-13 Right Primitive Group

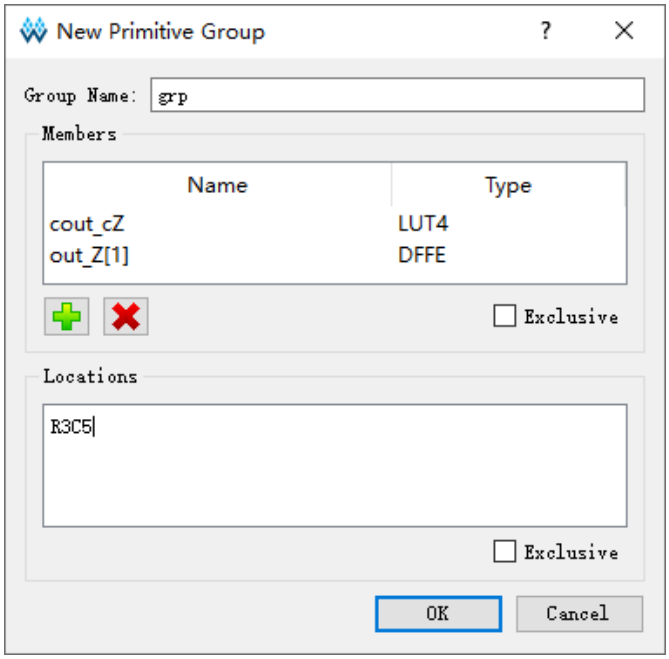


Figure 3-14 Invalid Locations

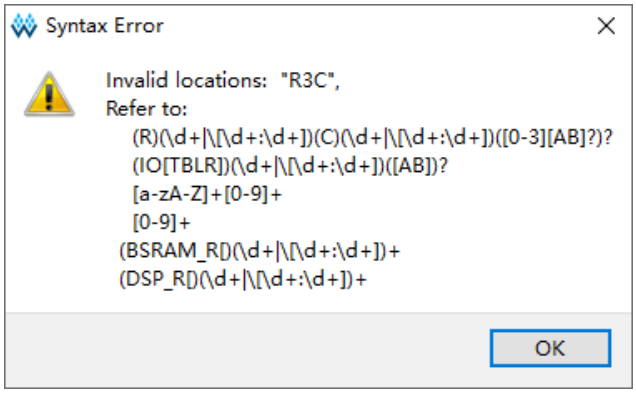
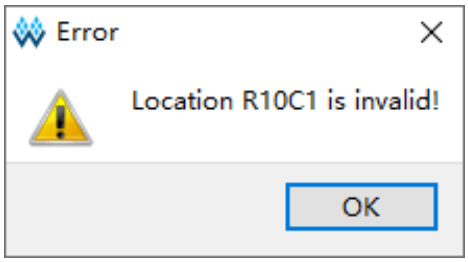


Figure 3-15 Invalid Locations



Create Relative Group.

1. Create Relative Group constraints. Right-click to select "New Relative Group" and a dialog box pops up, as shown in Figure 3-16.
2. You can set the group name, group members, and their relative

locations. You can add and remove primitives by "  " and "  " buttons. The created relative group constraints are shown in Figure 3-17.

Note!

- Group name, Primitive, and Relative Location are required.
- The locations can be inputted in the following ways:
  - Manually input
  - Before creating group constraints, copy the location and paste it to "New Relative Group > Relative Location" in Chip Array window.

3. Click "OK" to generate the constraints.
4. See the created constraints in "Group Constraints".Double-click the constraints, and a dialog box pops up, as shown in Figure 3-17; you can edit the constraints.

Figure 3-16 New Relative Group

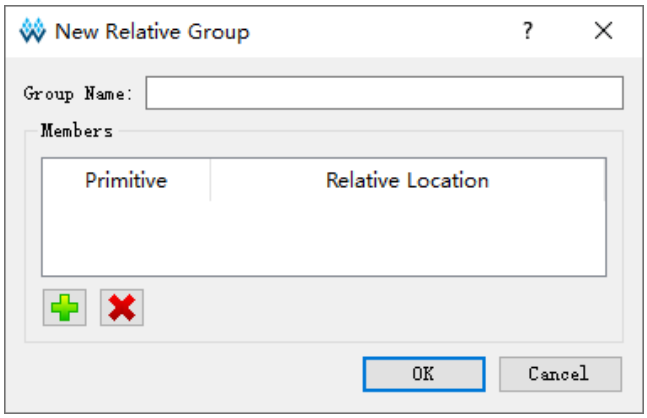
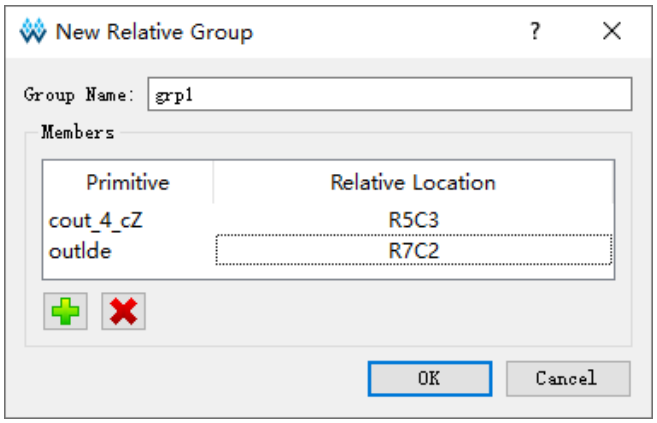


Figure 3-17 Right Relative Group



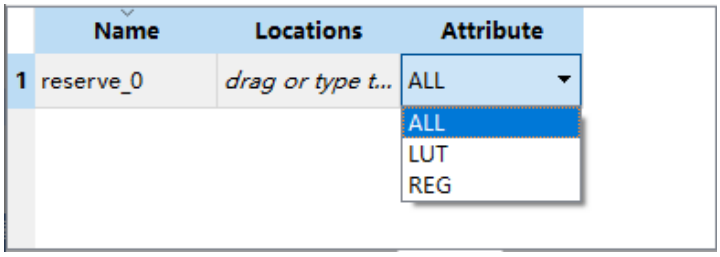
Resource Reservation

1. Create Resource Reservation constraints. Click Reserve Resources to create a new constraint in "Resource Reservation" window at the bottom of the interface.
2. You can type the locations or by dragging.
3. Double-click "Attribute" or click the "Attribute" column drop-down box to set the attribute of the reserved locations, as shown in Figure 3-18.

Note!

Name is used to distinguish reserved constraints. The name cannot be modified.

Figure 3-18 Resource Reservation



Clock Assignment

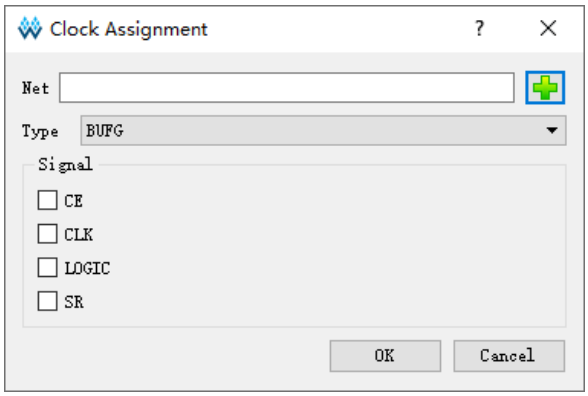
Create global clock constraints and the number of constraints is limited； and the constraints validity will be checked. Right-click to select "Clock Assignment" and a dialog box pops up, as shown in Figure 3-19. You can perform the following operations.

1. Click "  " to select the corresponding Net.
2. Select "BUFG", "BUFG[0]~[7]", "BUFS" and "LOCAL_CLOCK" via "Type" drop-down list.
3. Configure Signal via "CE" and "CLK". After finished, click "OK" to generate constraints in "Clock the Assignment". Double-click to open the dialog box for editing.

Note!

When LOCAL_CLOCK selected, the signal check box is grayed.

Figure 3-19 Clock Assignment



Quadrant Constraints

Create DCS and DQCE clock quadrant constraints. Constrain the specified instance to the specific quadrant according to the chip quadrants distribution. Right-click to select "Quadrant Constraints" and a dialog box pops up, as shown in Figure 3-20 and Figure 3-21. The related operations are as follows.

1. Select the corresponding DCS/DQCE primitive by clicking "  ". If there are no DCS/DQCE primitives in the design, you can not add.
2. Configure quadrant positions via the check boxes under "Position".
3. Click "OK" to generate constraints, which will be displayed in the "Quadrant Constraints" window. You can double-click to open the dialog box for editing.

Figure 3-20 Quadrant Constraints (GW1N-1)

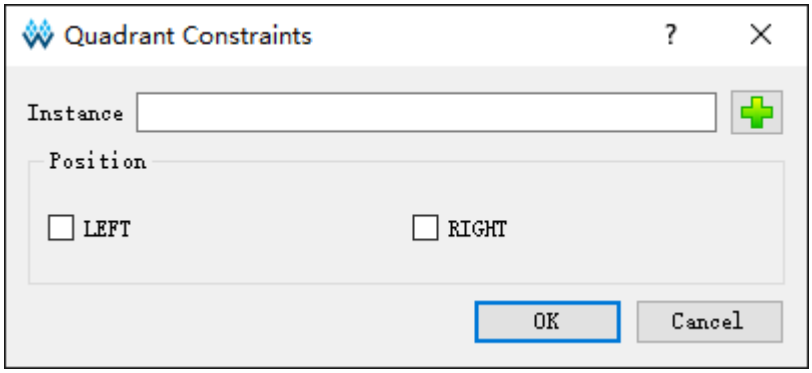
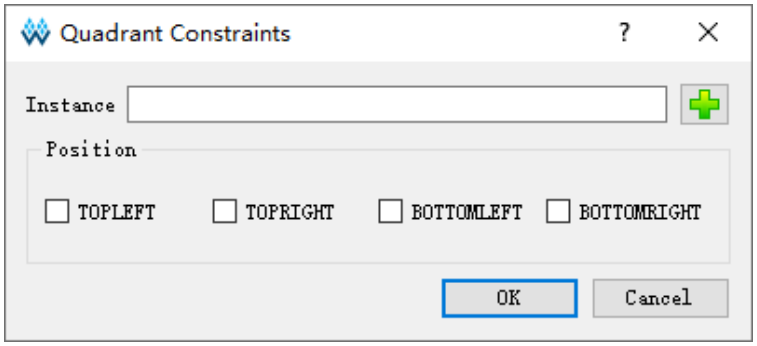


Figure 3-21 Quadrant Constraints (GW2A-18)



Hclk Constraints

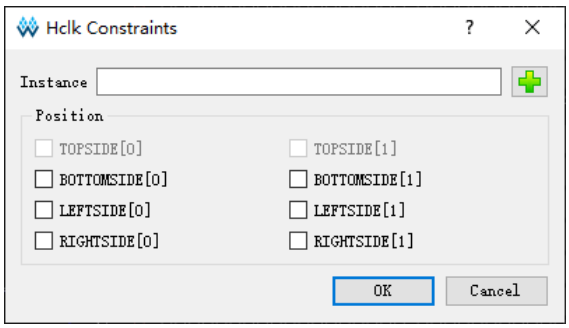
Create HCLK primitive constraints and specify the constraint locations on the device. Right-click to select "Hclk Constraints" and a dialog box pops up, as shown in Figure 3-22. The related operations are as follows.

1. You can select a primitive by clicking "". If there are no corresponding primitives in the design, you can not add.
2. Configure quadrant positions via the check boxes under "Position".
3. Click "OK" to generate constraints, which will display in "Hclk Constraints" window. You can double-click to open the dialog box for editing.

Note!

The available positions are different due to different devices in project, and the unavailable positions are greyed.

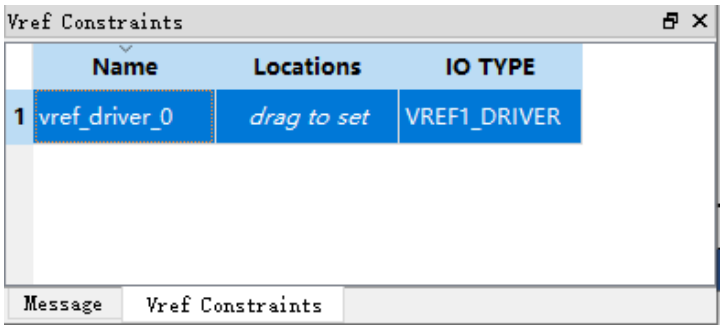
Figure 3-22 Hclk Constraint



Vref Constraints

Create Vref Driver to configure IO Port Vref; right-click and select "Define Vref Driver" to create a new constraint in the "Vref Constraints" window, as shown in Figure 3-23.

Figure 3-23 Vref Constraints



Note!

- Specify the location of Vref by dragging.
- Modify Vref name by double-clicking.

View Menu

As shown in Figure 3-24, View includes Toolbars, Windows, Zoom In, Zoom Out and Zoom Fit. The description of these sub-menus is as follows.

- Toolbars: Display shortcuts
- Windows: Display different windows, as shown in Figure 3-25
- Zoom In: Zoom in Chip Array or Package View
- Zoom Out: Zoom out Chip Array or Package View
- Zoom Fit: Zoom in/out Chip Array or Package View according to the window size.

Figure 3-24 View

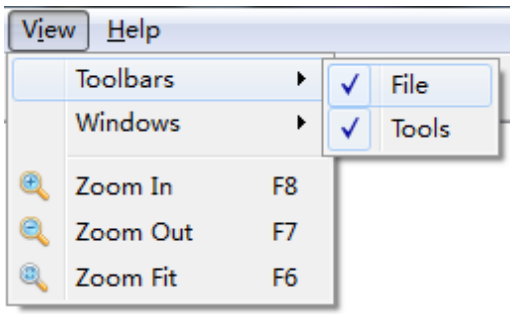
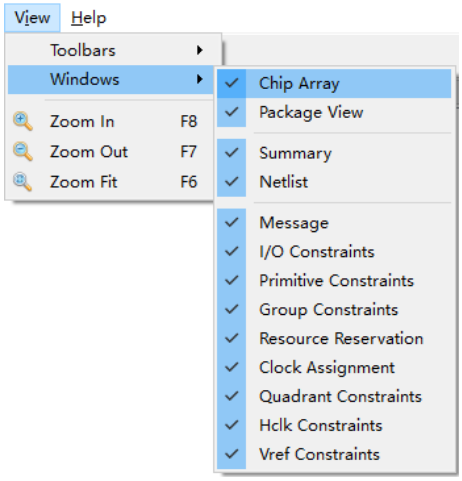


Figure 3-25 Windows



Help Menu

Help is used to provide software version and copyright information.

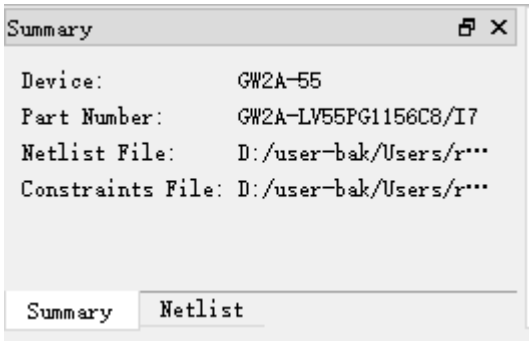
3.2.2 Summary and Netlist Windows

Summary and Netlist windows display device, part number, user design, constraints path and netlist, etc.

Summary Window

The summary window is shown in Figure 3-26. It displays the information of device, part number, design files and constraints files.

Figure 3-26 Summary Window



Netlist Window

As shown in Figure 3-27, Netlist window displays Ports, Primitives, Nets, Module, and timing paths.

Note!

- The Ports and Primitives names are displayed in full path and sorted in alphabetical ascending order by default.

- Port and Net display via Bus and non-Bus, as shown in Figure 3-28.
- Modules are displayed in hierarchy and the number of instances in each module is also displayed, as shown in Figure 3-29.
- The timing path is listed in the ascending order of slack, as shown in Figure 3-30.

Figure 3-27 Netlist Window

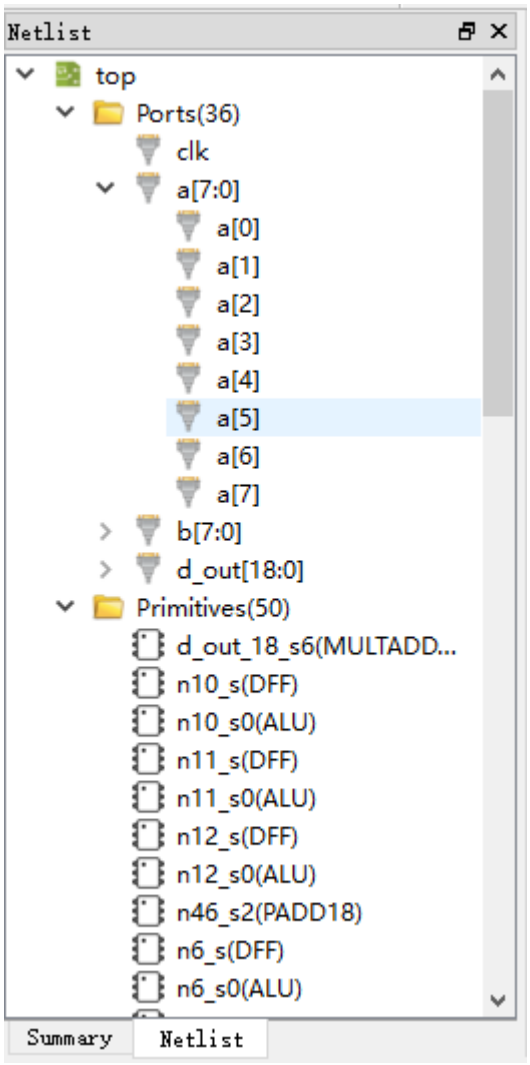


Figure 3-28 BUS and Non-Bus Display

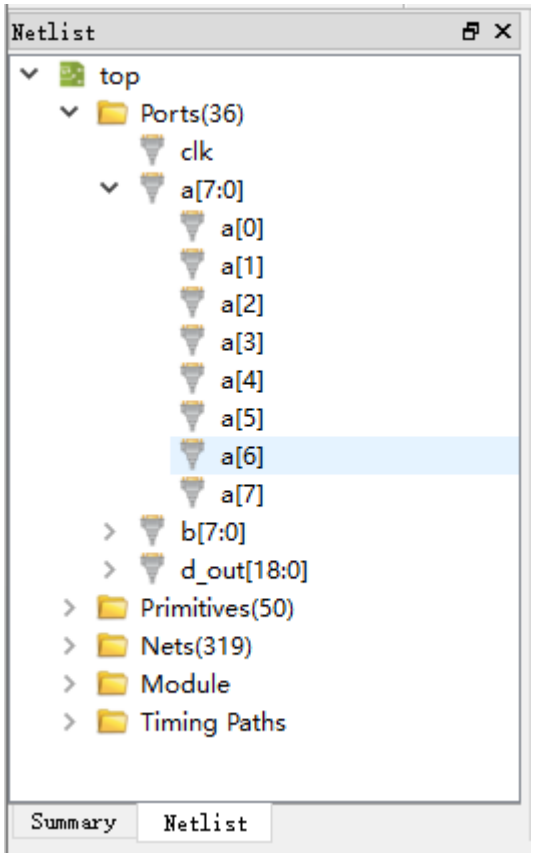


Figure 3-29 Hierarchy Display

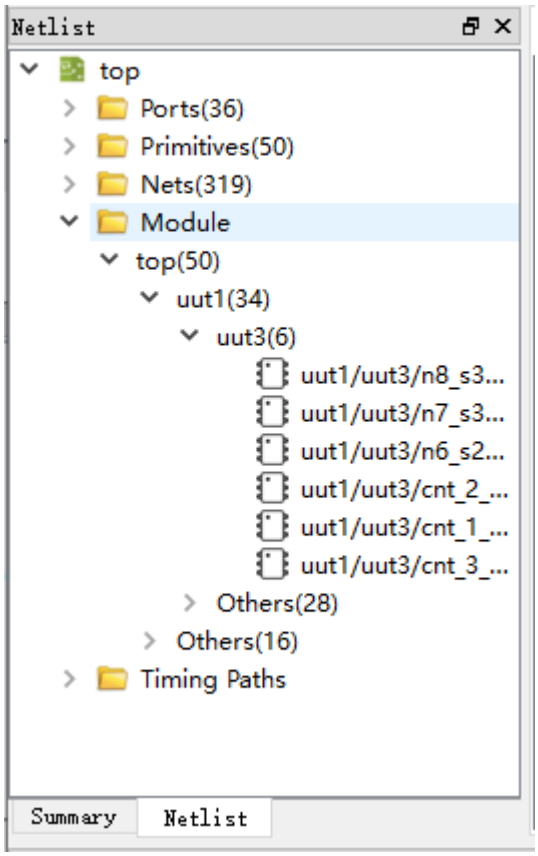
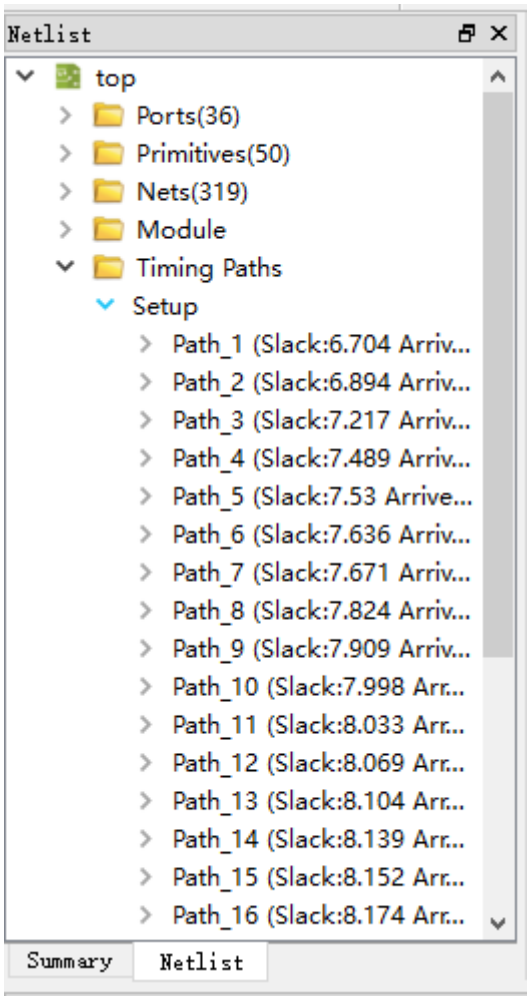


Figure 3-30 Timing Paths



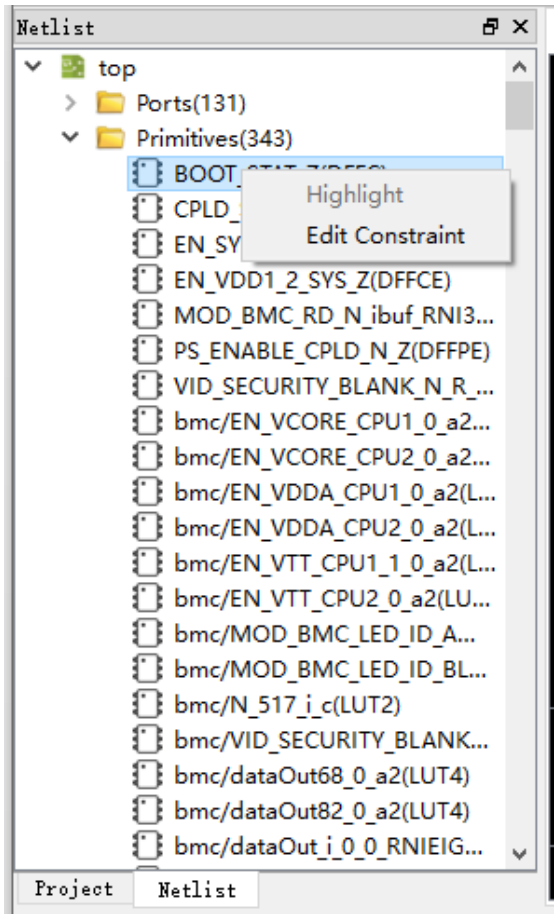
Netlist provides right-click menu as shown below.

- Highlight: Highlight the corresponding constraint location in Chip Array.
- Edit Constraint: Edit the corresponding constraints.

Note!

If the current Primitive or Port has no constraints locations, the highlight is not available, as shown in Figure 3-31.

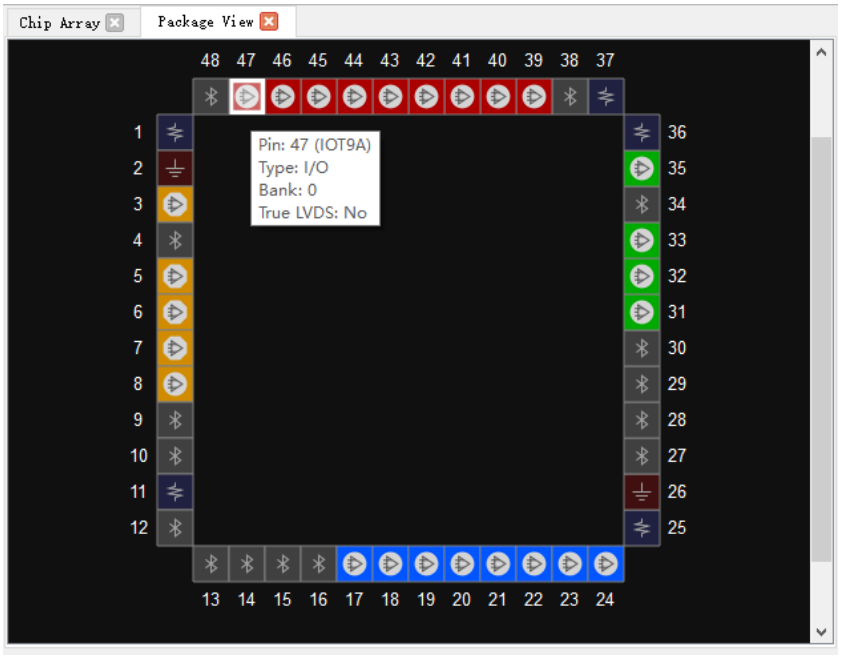
Figure 3-31 Netlist Right-clicking



3.2.3 Package View

As shown in Figure 3-32 , taking GW1NRF-4B-QFN48 as an example, Package View displays I/O, supply pin, and ground pin based on chip package. When the mouse is placed on a location, the I/O type, bank, and LVDS will display.

Figure 3-32 Package View (GW1NRF-4B-QFN48)



Various symbols and colors are used to distinguish user I/Os, power supply pins and ground pin. The colors of IO pins of different BNAKS are different, as shown below.

- "  ": User I/O
- "  ": VCCIO
- "  ": VSS
- "  ": Bluetooth interface

The right-click menu supported by the Package View is shown in Figure 3-33. The descriptions are as follows.

- Zoom In: Zoom in Package View
- Zoom Out: Zoom out Package View
- Zoom Fit: Zoom in/out Package View to fit window size
- Show Differential IO Pairs: Display differential pair. As shown in Figure 3-34, a differential pair is connected by a red line.
- Top View: Package View is displayed in the top view by default. The top view of GW1N-9-WLCSP64 with coordinate origin at the top left corner is as shown in Figure 3-35; and the top view of GW1N-9-WLCSP81M package with coordinate origin at the top right

corner as shown in Figure 3-37.

- Bottom View: The bottom view of GW1N-9-WLCSP64 with coordinate original at the bottom right corner is as shown in Figure 3-36; and the bottom view of GW1N-9-WLCSP81M with coordinate original at the bottom left is as shown in Figure 3-38.

Figure 3-33 Package View Right-clicking

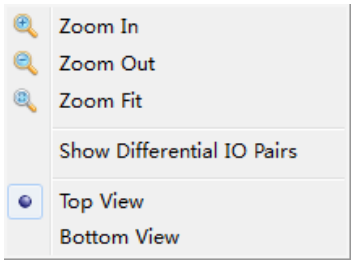


Figure 3-34 Differential Pair Display

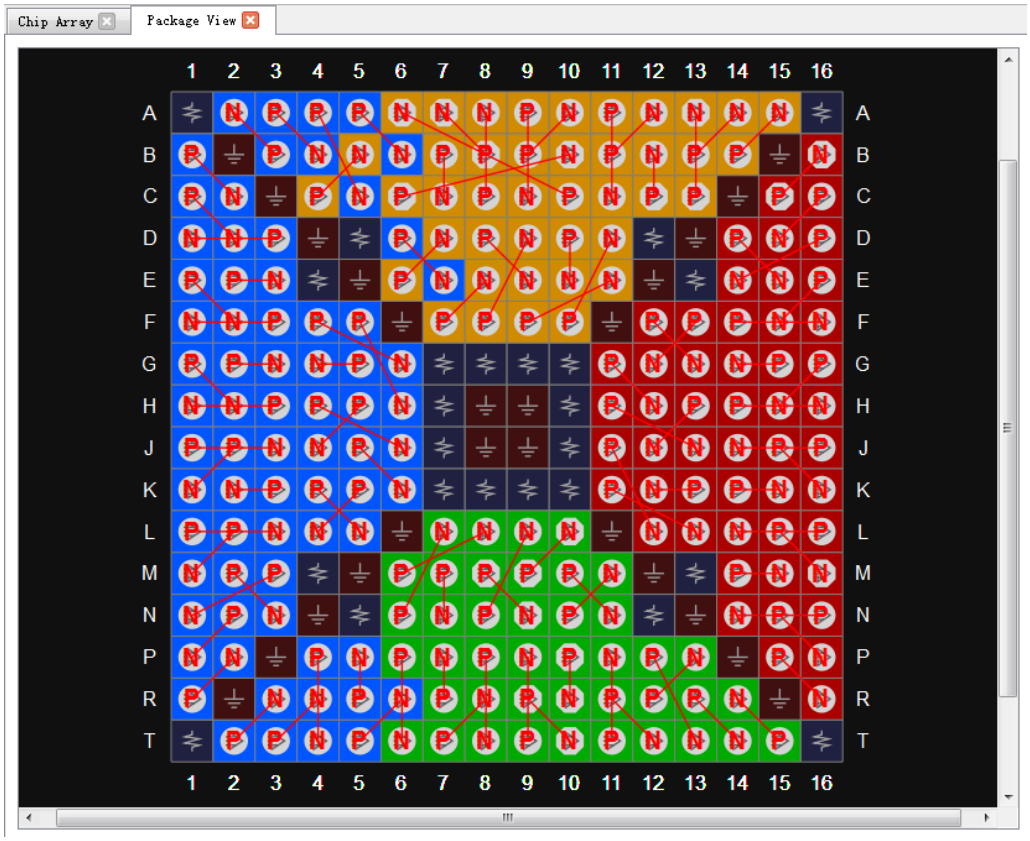


Figure 3-35 Top View

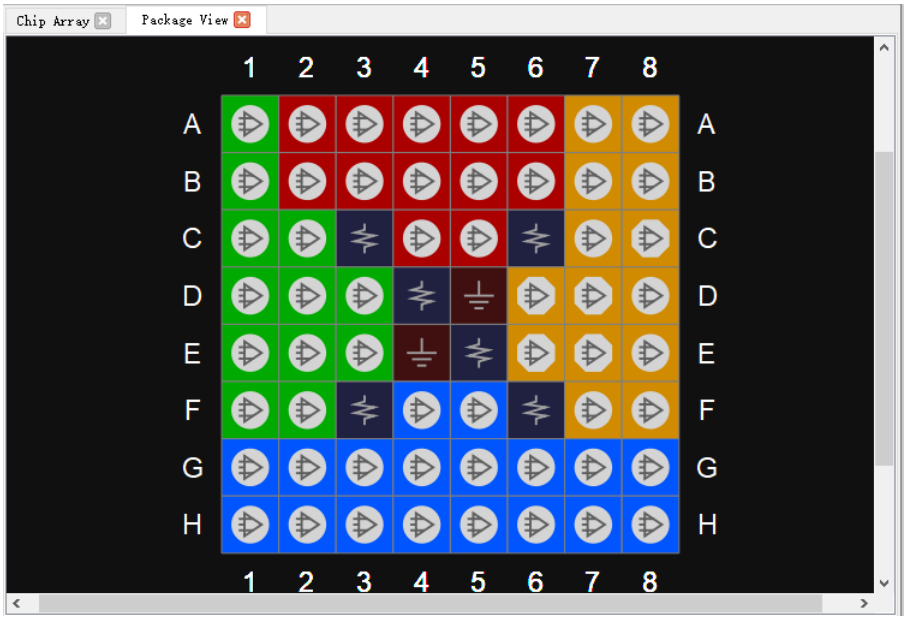


Figure 3-36 Bottom View

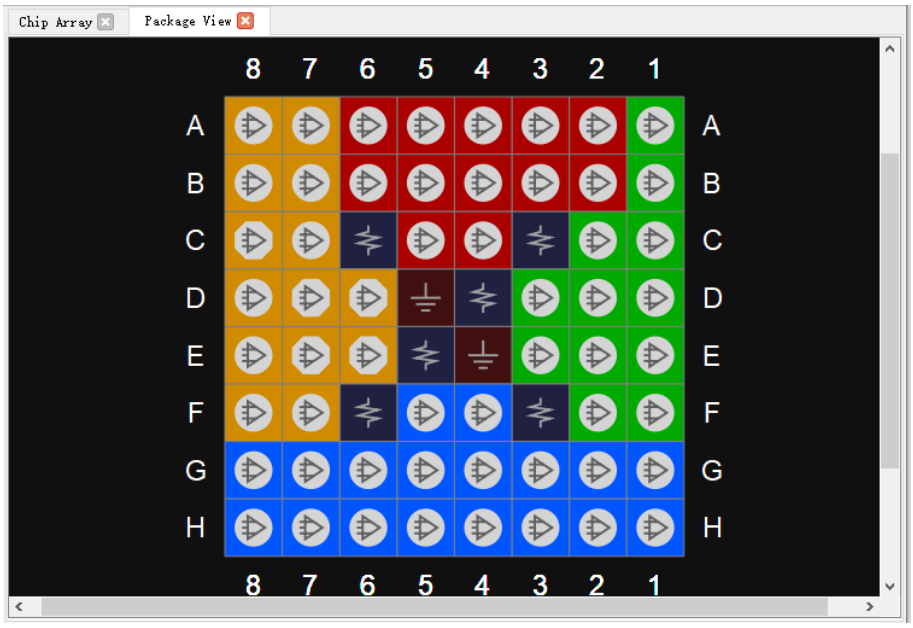


Figure 3-37 GW1N-9-WLCSP81M Top View

Figure 3-38 GW1N-9-WLCSP81M Bottom View

Package View supports the display of IO Port constraint locations, and the IO Port can be constrained by dragging from the Netlist or I/O Constraints to the Package View window. When dragged, the port name will be displayed; the unconstrianted pins are grayed out and not dragged.

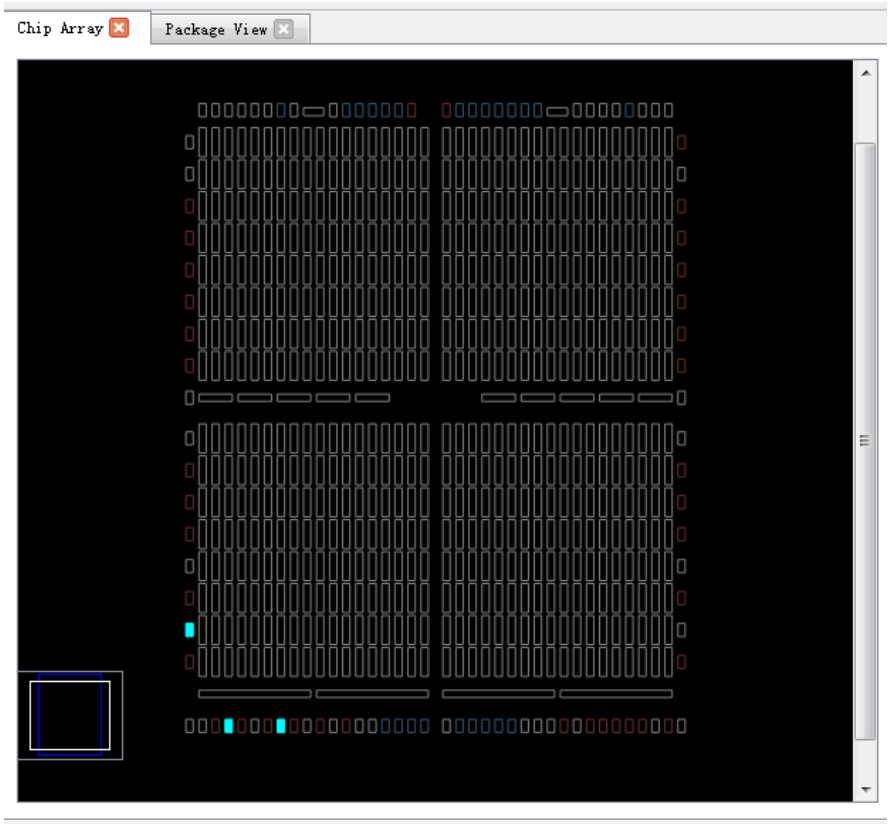
3.2.4 Chip Array Window

The Chip Array window of FloorPlanner is shown in Figure 3-39. Chip Array displays I/O, CFU, CLU, DSP, PLL, BSRAM, and DQS according to the row and column information of the chip, supports real-time display of all constraints locations, and also supports the functions of zoom in/out and dragging, etc.

I/O denotes all I/O locations of die and is distinguished with different colors.

- White: Bonded out I/O location
- Red: Unbonded I/O location
- Blue: If it is a SIP device, such as GW2AR-18, GW1NR-4, and GW1NR-9, there will be blue marked I/O.

Figure 3-39 Chip Array Window



Chip Array provides grid mode, macrocell mode, and primitive mode.

- Grid mode: Display constraints locations in grid, as shown in Figure 3-40.
- Macrocell mode: Display constraints locations in CLS, IOBLK, as shown in Figure 3-41.

- Primitive mode: Display constraints locations in REG, LUT etc., as shown in Figure 3-42.

Figure 3-40 Constraints in Grid

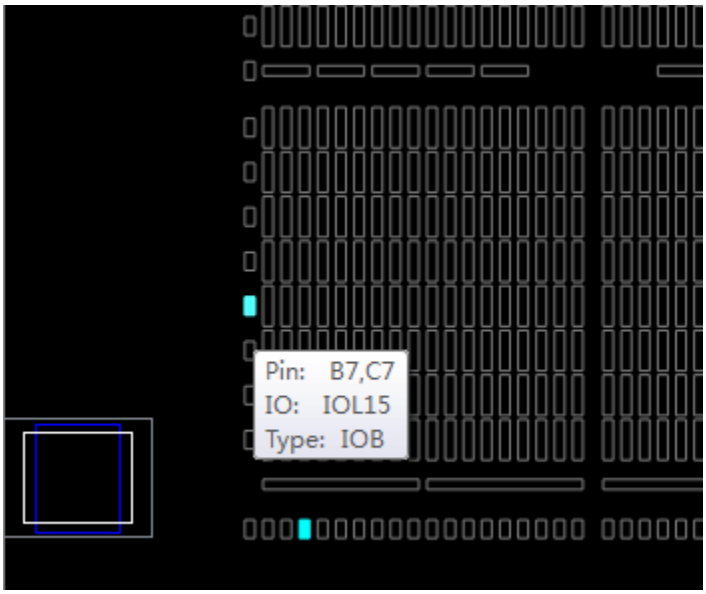


Figure 3-41 Constraints in Macrocell

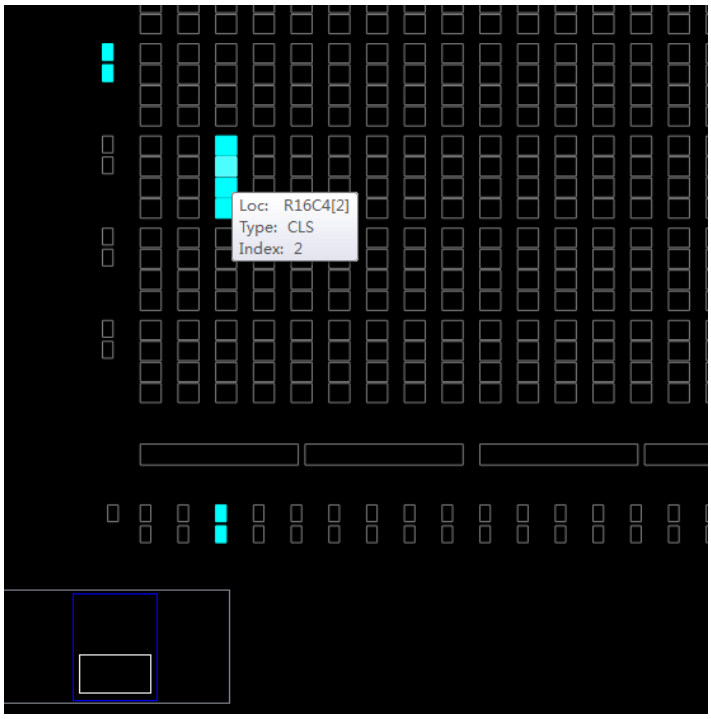
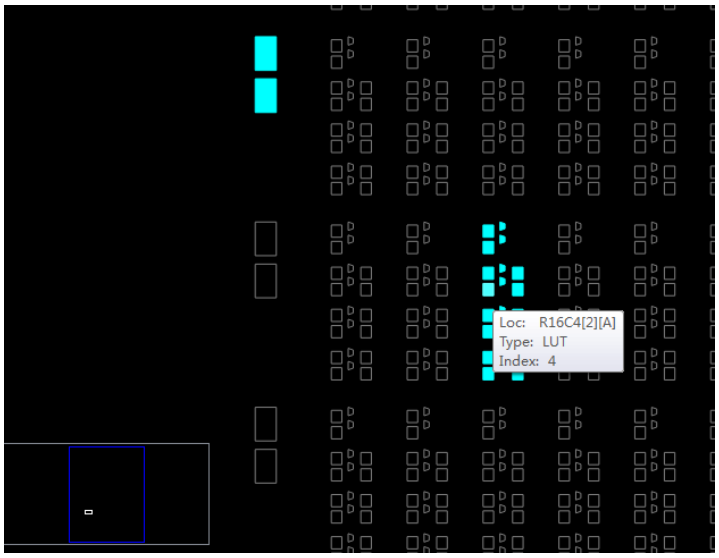


Figure 3-42 Constraints in Primitive



Chip Array supports following dragging functions.

- Drag from Netlist to Array to generate constraints and specify constraints location.
- Drag from Editing to Array to specify constraints location.

There is a chip sub-window in Chip Array for real-time display of the current view relative to the device. Drag the white frame in the chip sub-window to move Chip Array. Chip Array distinguishes constraints type and displays constraints locations in different colors. The color meaning is as follows.

- White: Display constraints location being selected or highlighted.
- Dark blue: Display reserved constraints, indicating that the location cannot be occupied again.
- Light blue: Display IO and Primitive constrained in a grid or range.

Chip Array supports right-clicking functions are as follows.

- Zoom In: Zoom in Chip Array
- Zoom Out: Zoom out Chip Array
- Zoom Fit: Zoom in/out Chip Array to fit the window size
- Show Constraints View: Show instances constraints view of Chip Array
- Show Place View: Show instances place view of Chip Array; it is only effective when FloorPlanner is started after running Place & Route. Otherwise, it is greyed out.
- Show Multi-View: Show instances constraints and place views of Chip

Array; it is only effective when FloorPlanner is started after running Place & Route. Otherwise, it is greyed out.

- Show In-Out Connection: Show and select the input and output connection of the instance in the Place View; it can only be used if an instance is selected when Show Place View > All Instance view opens. Otherwise, it is greyed out.
- Show In Connection: Show and select the input connection of the instance in the Place View; it can only be used if an instance is selected when Show Place View > All Instance view opens. Otherwise, it is greyed out.
- Show Out Connection: Show and select the output connection of the instance in the Place View; it can only be used if an instance is selected when Show Place View > All Instance view opens. Otherwise, it is greyed out.
- Unhighlight All: Remove highlight.
- Copy Location: Copy the selected location or area; If GRID and Block are selected, "Copy Location" in right-click menu is available. Otherwise, it is unavailable, as shown in Figure 3-43.

Show Place View also shows Lut and Reg density, as shown in Figure 3-44.

- ALL Instance: Show place of all instances. Light green indicates less than five, green indicates six to ten, and dark green indicates more than ten.
- Only Lut: Shows place of all Lut. Light green indicates less than two, green indicates three to four, and dark green indicates more than four.
- Only Dff: Shows place of all Reg. Light green indicates less than two, green indicates three to four, and dark green indicates more than four.

You can view the place of all instances in the design by clicking Show Place View > ALL Instance.

- Hover the mouse over the instance place location in the Chip Array window to display the name of the instance, as shown in Figure 3-45.
- Select a specific instance in the Netlist window; right-click and select "Highlight", the place location of that instance will be highlighted, as shown in Figure 3-46.

Note!

You can select an area by "Ctrl" + left mouse button; right click and select "Copy Location", you can copy the location and paste it to any constraint editing window.

Figure 3-43 Chip Array Right-clicking

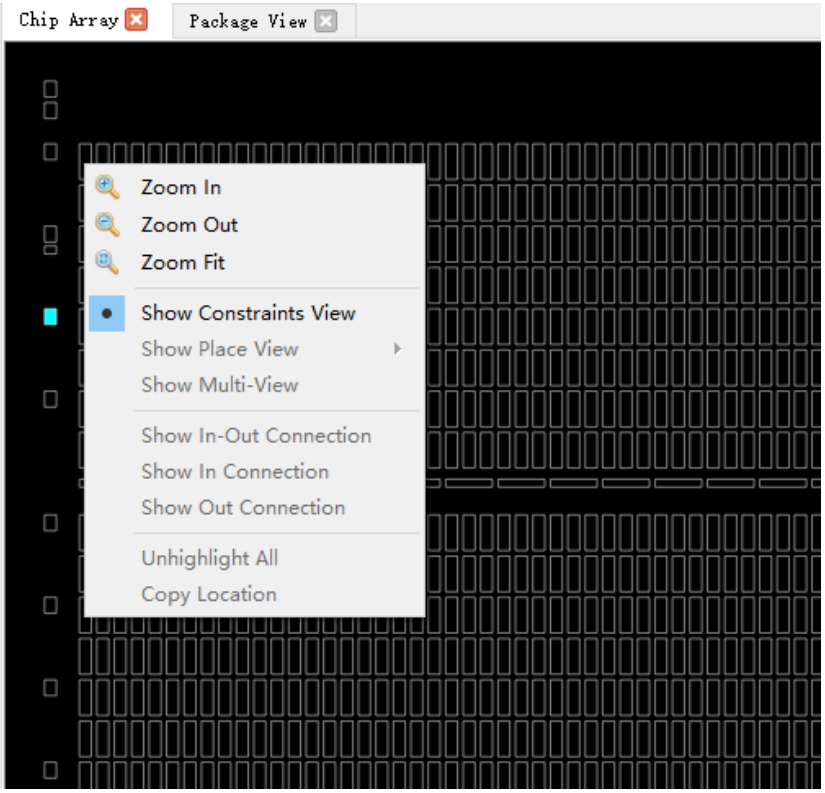


Figure 3-44 Show Place View

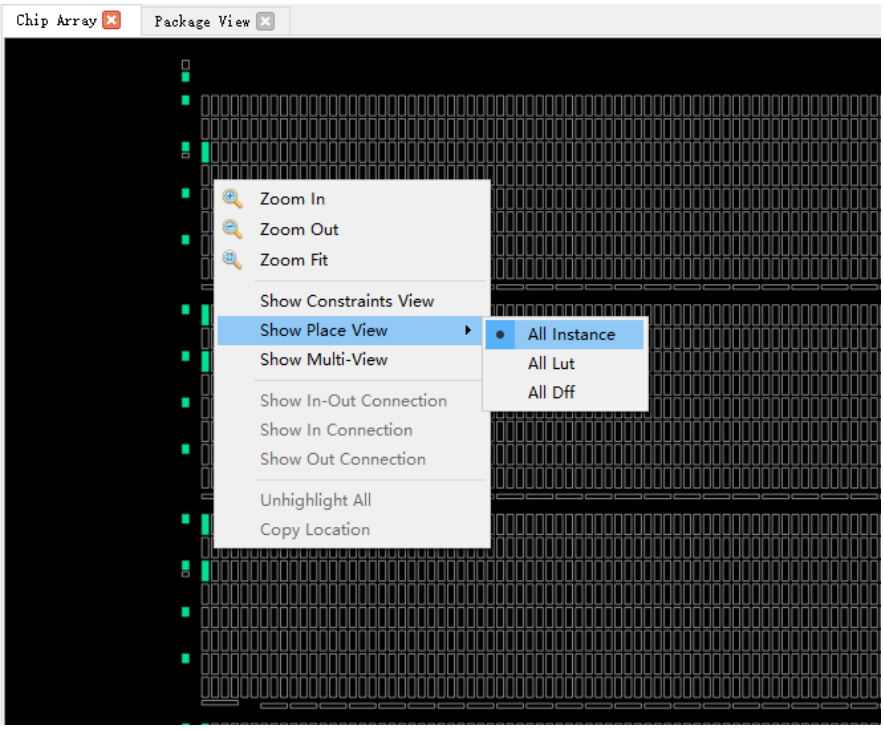


Figure 3-45 Mouse Hovering Display

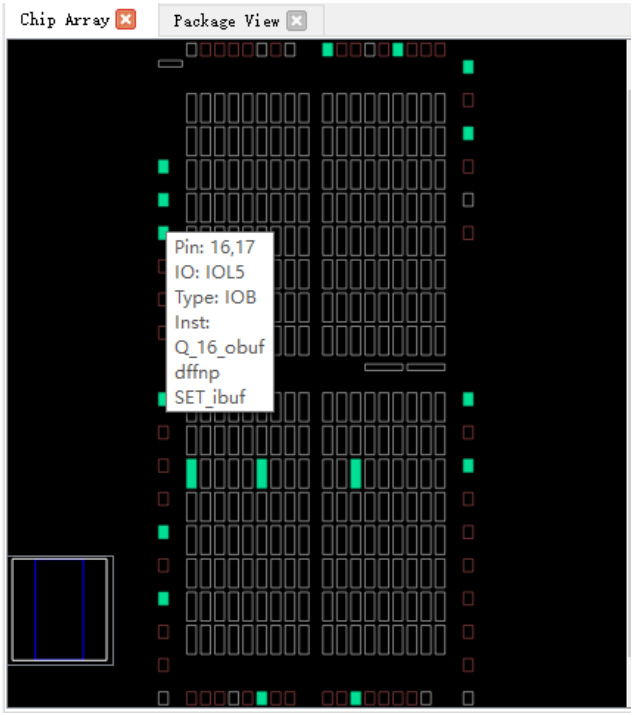
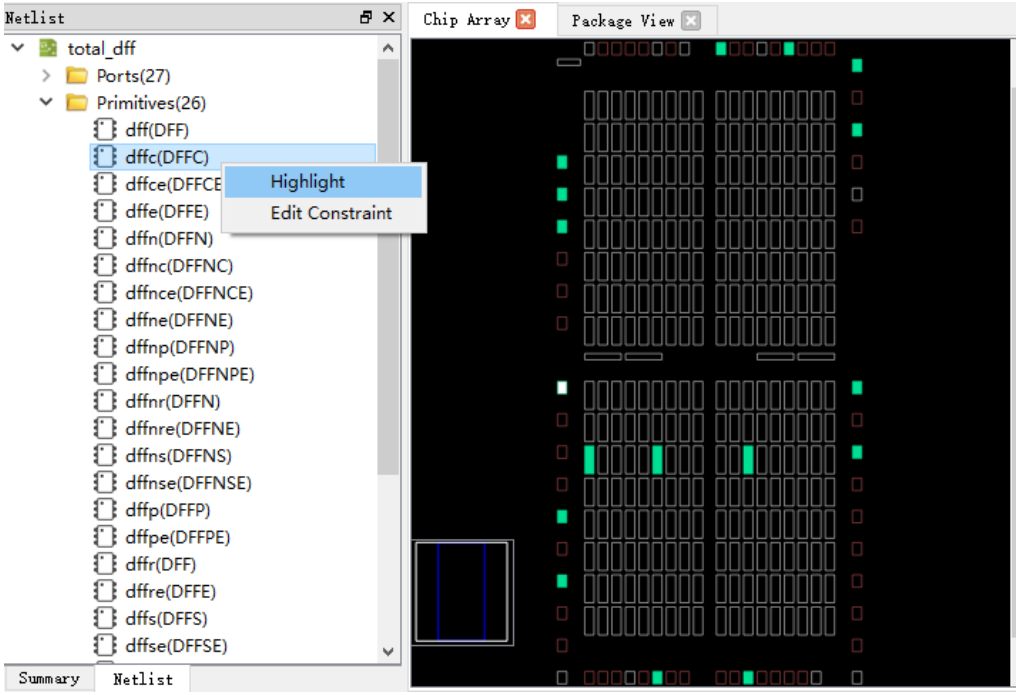
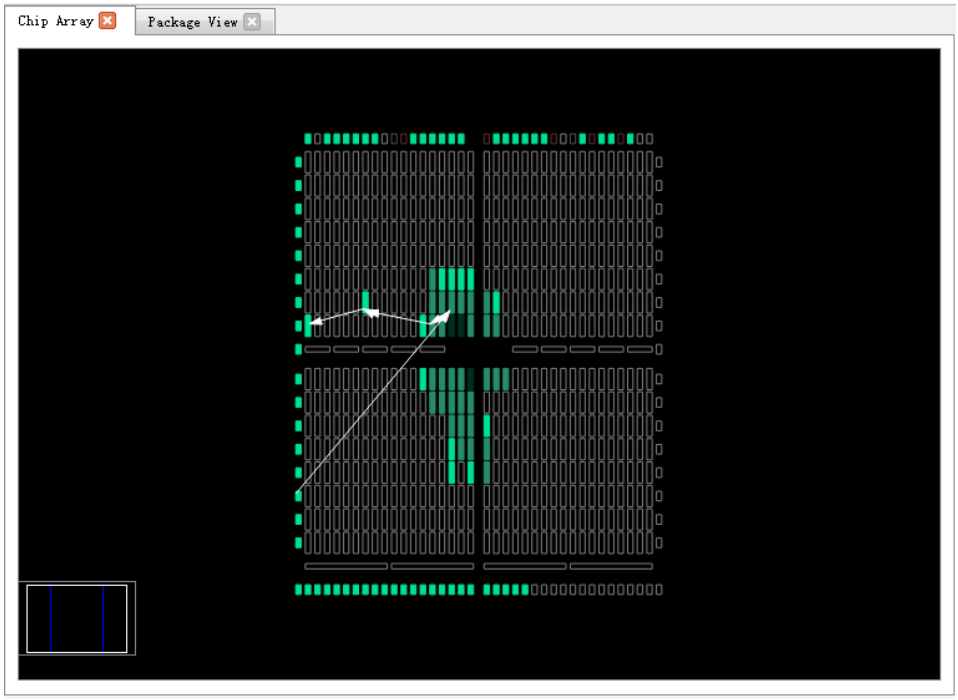


Figure 3-46 Right-click to Select Hightlight



Chip Array also can highlight timing paths, as shown in Figure 3-47.

Figure 3-47 Timing Path Highlighted



3.2.5 Constraints Editing Window

Constraints editing window includes eight constraints views, such as, "I/O Constraints", "Primitive Constraints", "Group" Constraints, etc., which are used to display constraints and provide constraints editor and drag function. The brief introduction of each view is as follows.

I/O Constraints

I/O Constraints is used to constrain ports. I/O constraint view is as shown in Figure 3-48, and the functions are as follows.

- Display IO Port attributes and constraints in user design, such as Direction, Bank, IO Type, Pull Mode, etc.
- Support to edit constraints locations and attribute, etc.
- Change constraints by dragging, double-clicking, etc.

Note!

- Set I/O location by dragging or double-clicking.
- Display IO name when dragged.
- When I/O is dragged into Chip Array window, the location where I/O can be placed is brightened, and the color of the location where I/O cannot be placed remains unchanged.
- When I/O is dragged into Package View window, the color of the location where I/O can be placed remains unchanged and the location where I/O cannot be placed becomes darker.

- After setting, the constraints location in Chip Array is highlighted in light blue, and the constraints location in Package View is highlighted in orange.

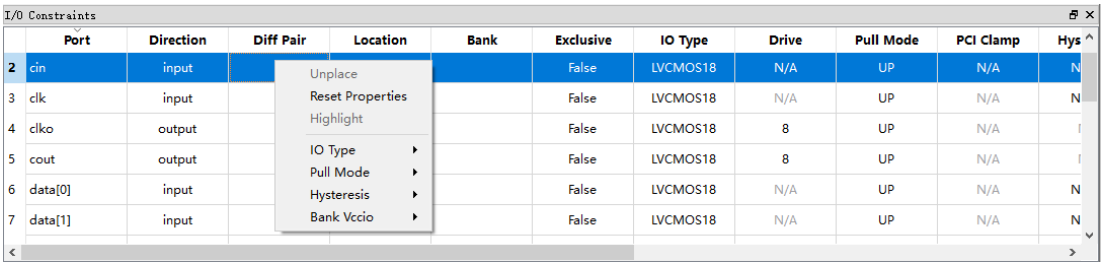
The details of the right-click menu are as follows.

- Unplace: Cancel placement
- Reset Properties: Reset Port properties
- Highlight: Highlight constraints location
- IO Type: Set the level standard
- Drive: Set drive voltage
- Pull Mode: Set pull-up mode
- PCI Clamp: Set the switch of PCI protocol
- Hysteresis: Set hysteresis
- Open Drain: Set the switch of open-drain circuit
- Vref: Set reference voltage
- Single Resistor: Set the switch of single-ended resistor
- Diff Resistor: Set the switch of differential resistor
- Bank Vccio: Set BANK voltage

Note!

You can modify port attributes in batches by right-clicking; if you select multiple ports, and these ports have the same attribute values to be configured, they can be configured in batches. For the details, you can see *DS102, GW2A series of FPGA Products Data Sheet*.

Figure 3-48 I/O Constraints View



Primitive Constraints

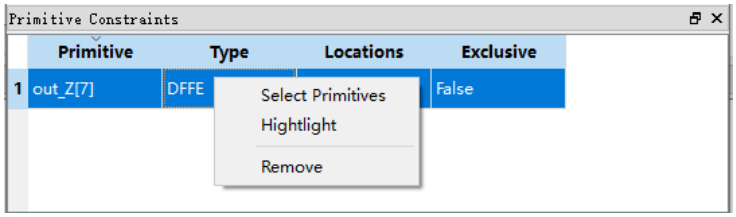
Primitive Constraint is used to constrain primitive location, as shown in Figure 3-49, and the functions are as follows:

- Display the name, type, location, and Exclusive of all Primitive constraints;
- Support editing; you can highlight, remove, add and update constraints by right-clicking.

Note!

- Modify the locations by dragging or double-clicking
- Set Exclusive by double-clicking
- Syntax and legality will be checked for the locations when manually writing primitive constraints, and error message dialog boxes are as shown in Figure 3-14 and Figure 3-15.

Figure 3-49 Primitive Constraints View

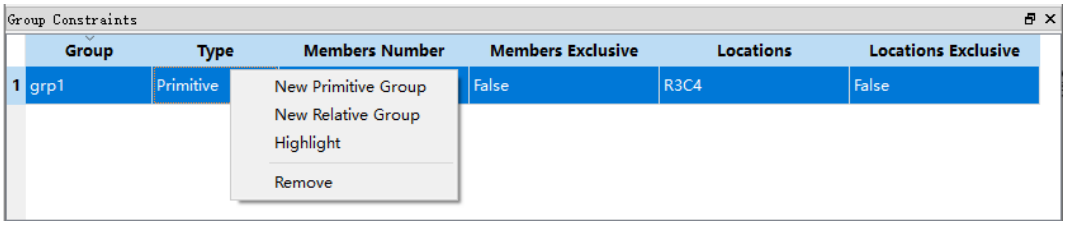


Group Constraints

Group Constraints is used for group constraints on the I/O and some primitives in the design, the group constraint view is shown in Figure 3-50; and the functions are as follows.

- The view displays the name, type, number of primitive, location, and Exclusive of all group constraints, which includes primitive and relative group constraints. As shown in Figure 3-13 and Figure 3-17, double-click the group to edit constraints.
- You can highlight, remove, add and update constraints by right-clicking.

Figure 3-50 Group Constraints View



Resource Reservation

Resource Reservation is used for reservation constraints on the resources available in the current package, as shown in Figure 3-51; and the functions are as follows.

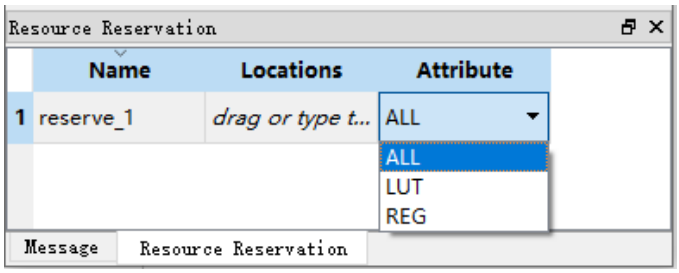
- The view can display reserved constraints locations.
- You can highlight, remove, add and update constraints by right-clicking.

- "Name" is used to distinguish utilization resource of each reservation constraint; and you cannot modify the name.

Note!

You can change the locations by dragging or double-clicking;

Figure 3-51 Resource Reservation View



Clock Assignment

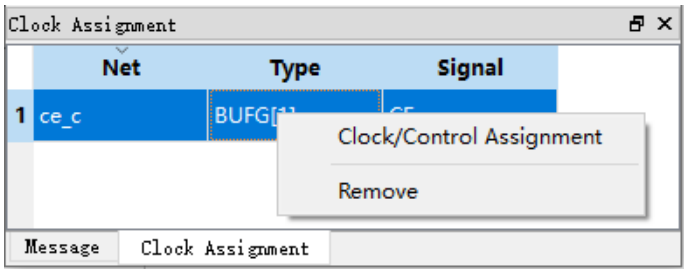
Clock Assignment is used for clock constraints on the net in the design, as shown in Figure 3-52, and the functions are as follows.

- The view displays all clock constraints.
- You can add and remove clock constraints by right-clicking.

Note!

- Double-click to edit.
- Dragging is not supported if there is no location.
- Clock constraint creation is as shown in Figure 3-19.

Figure 3-52 Clock Assignment View



Quadrant Constraints

Quadrant Constraints is used for quadrant constraints on the DCS, DQCE in the design, as shown in Figure 3-53, and the functions are as follows.

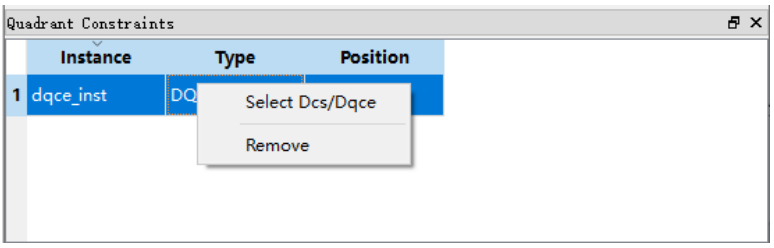
- Display all quadrant constraints, including Instance name, type, and locations.

- You can remove and add constraints by right-clicking.

Note!

Quadrant constraint creation is as shown in Figure 3-20 and Figure 3-21.

Figure 3-53 Quadrant Constraints View

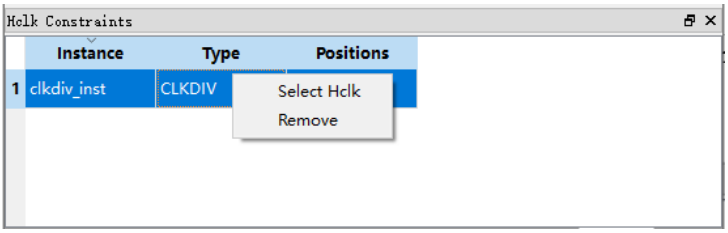


Hclk Constraints

Hclk Constraints is used for Hclk constraints on CLKDIV, DLLDLY in the design, as shown in Figure 3-54, and the functions are as follows.

- The view can display the instance location constraints of Hclk, including Instance name, type, and quadrant location.
- You can remove and add constraints by right-clicking. Hclk constraints creation is shown in Figure 3-22.

Figure 3-54 Hclk Constraints View



Vref Constraints

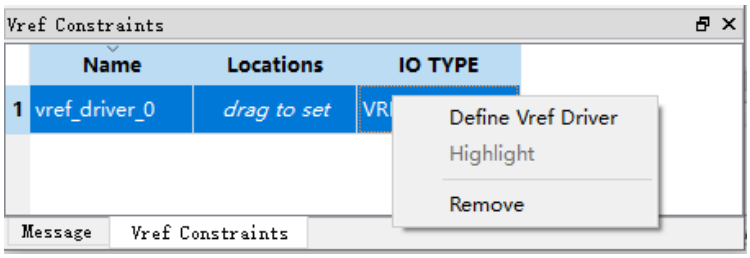
Vref Constrains is used for the external reference voltage of the bank where the constraint is located, as shown in Figure 3-55, and the functions are as follows.

- The view can display Vref Driver defined by users, such as, Vref name and location.
- You can highlight, remove, and add constraints by right-clicking.

Note!

Locations can only be set by dragging.

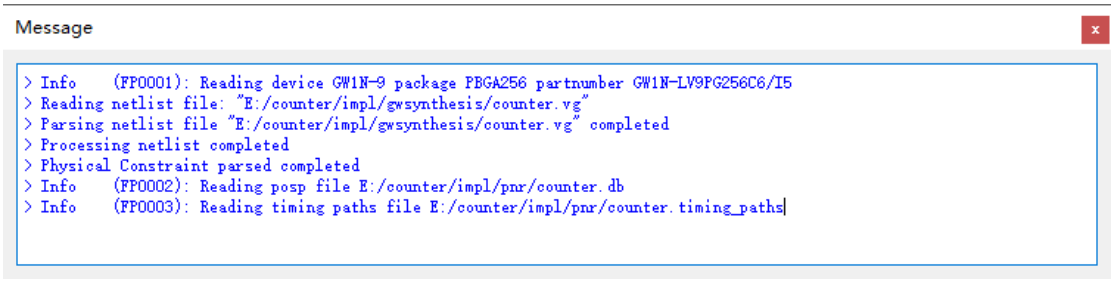
Figure 3-55 Vref Constraints View



3.2.6 Message Window

The message window is as shown in Figure 3-56, and it displays the output.

Figure 3-56 Message Window



4 FloorPlanner Usage

FloorPlanner can create and edit constraints, generate physical constraint files used in Place & Route.

4.1 Create Constraints File

FloorPlanner can output newly created or modified physical constraint files, and the steps are shown below.

1. Start FloorPlanner as described in 3.1 Start FloorPlanner.
2. Click "File > New" to open the "New" dialog box.

   Note!

   You can also open "New" dialog box in the following two ways.

   - Use the "Ctrl+N" shortcut
   - Click the "New" icon in the toolbar
3. Select netlist file and part number, as shown in Figure 4-1.

Figure 4-1 New Physical Constraints

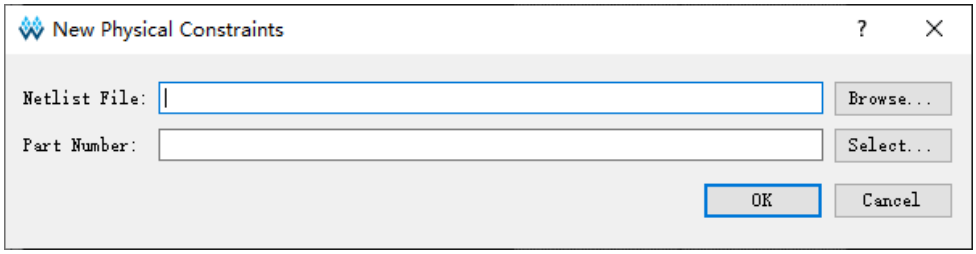
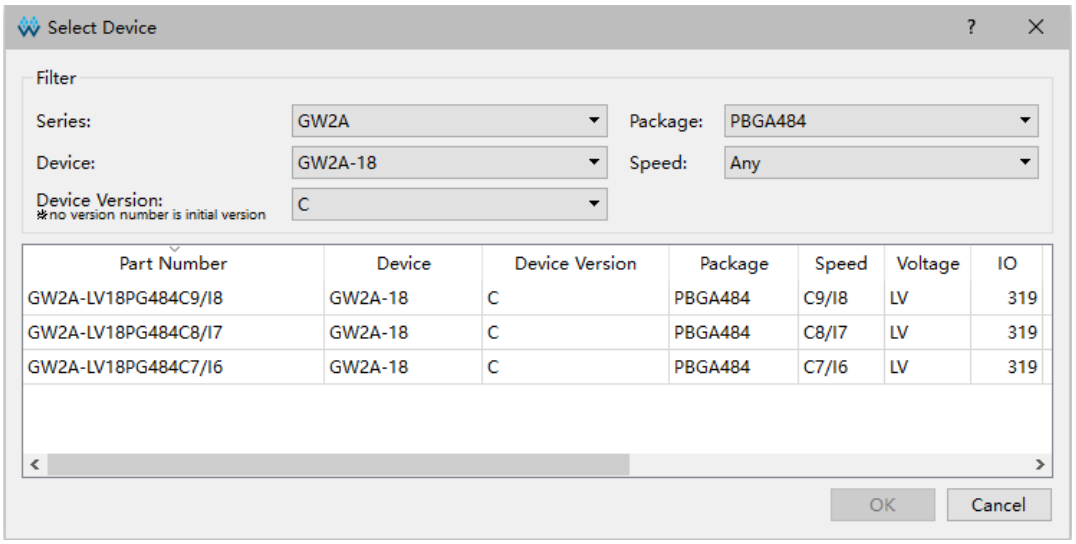


Figure 4-2 Select Device



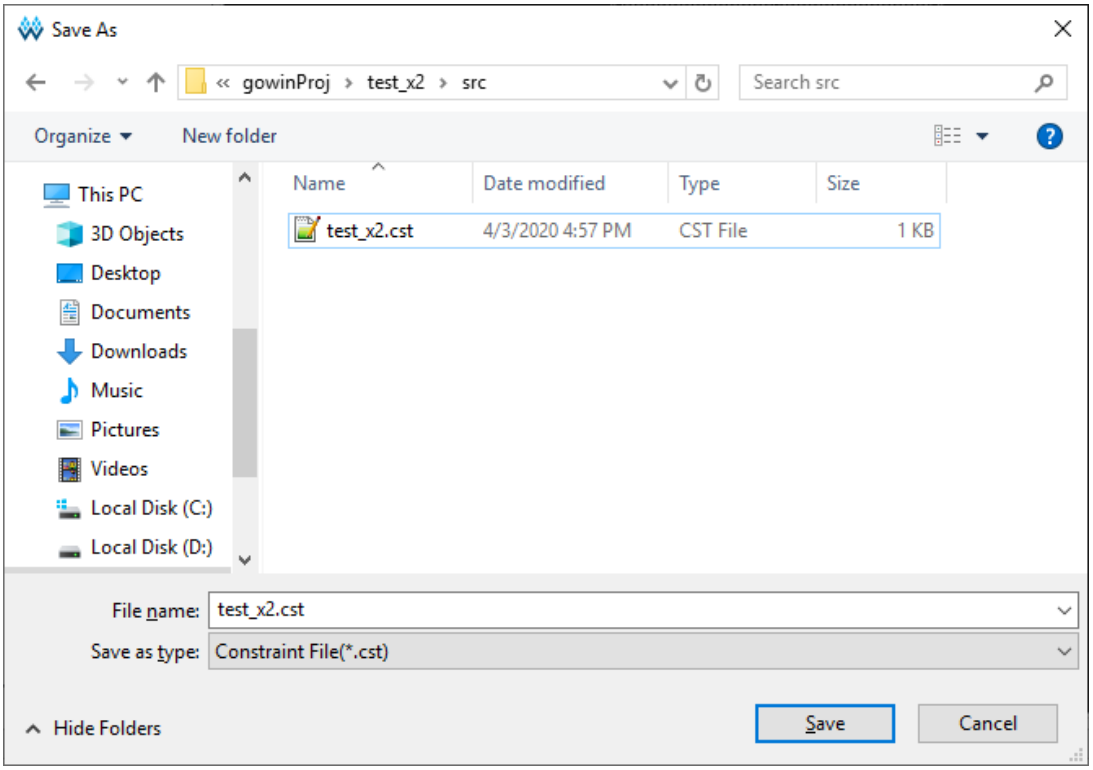
Note!

- You can select the device, package, and all Gowin FPGA devices, as shown in Figure 4-2.
- Start FloorPlanner using the first way in 3.1 Start FloorPlanner.

You can perform the following operations in FloorPlanner:

1. Distribute the pins location by dragging;
2. Click "Save" to output constraint files.
3. You can modify the file name in "Save" dialog box, as shown in Figure 4-3.

Figure 4-3 Save Output File



4.2 Edit Constraints File

FloorPlanner supports constraints creation of I/O, primitive, group, resource reservation, global clock assignment, clock quadrant, high-speed clock, and reference voltage, etc. Constraints can be generated via Constraints menu, see 3.2.1 Menu Bar for details.

Note!

Constraints can also be created by other ways; the following section mainly introduces how to generate constraints by dragging.

4.2.1 Constraints Examples

Take the user design counter.v for an instance to introduce how to create various constraints.

```
module counter1(out, cout, data, load, cin, clk, ce, clko);
output [7:0] out;
output cout;
output clko;
input ce;
```

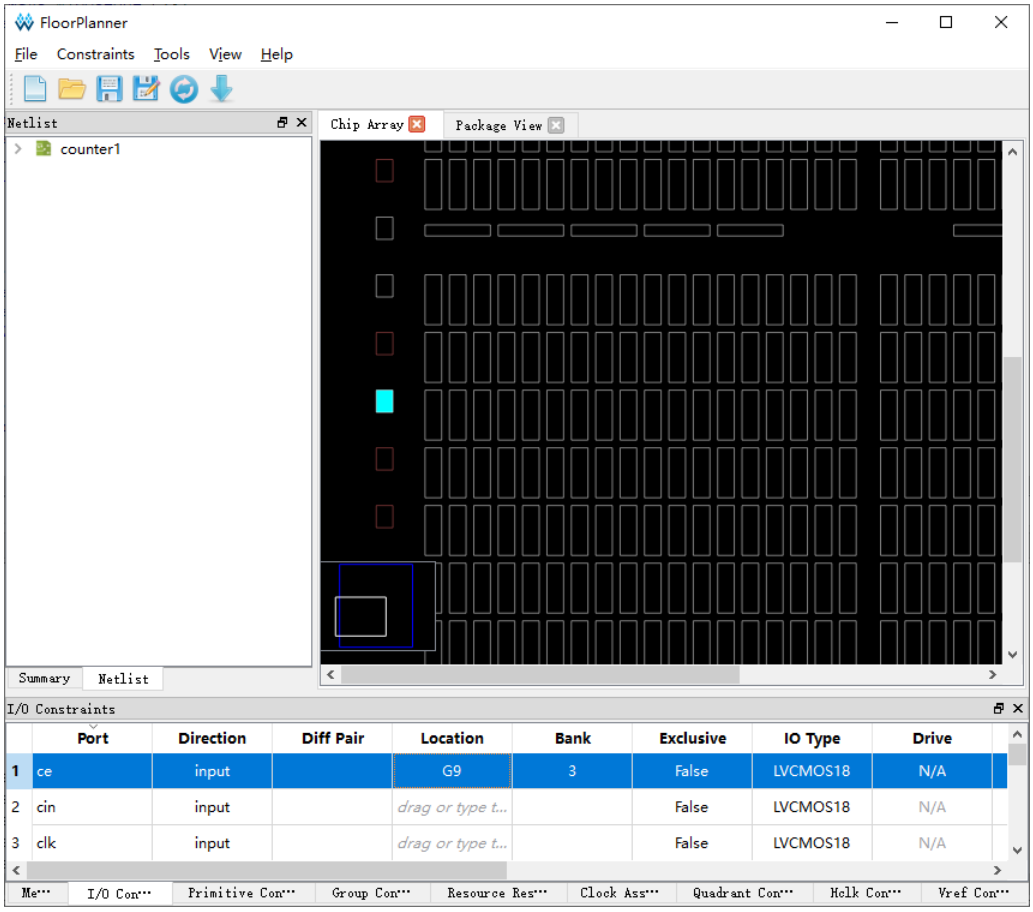
```
input [7:0] data;
input load, cin, clk;
reg [7:0] out;
always @(posedge clk)
begin
    if (load)
        out = data;
    else
        out = out + cin;
end
assign cout = &out & cin;
wire clkout;
CLKDIV clkdiv_inst (
      .CLKOUT(clkout),
      .HCLKIN(clk),
      .RESETN(1'b1),
      .CALIB(1'b0)
);
defparam clkdiv_inst.DIV_MODE = "2";
defparam clkdiv_inst.GSREN = "false";
DQCE dqce_inst (
      .CLKOUT(clko),
      .CLKIN(clkout),
      .CE(ce)
);
endmodule
```

4.2.2 Edit I/O Constraints

Drag to Chip Array to create I/O constraints.

1. Click I/O Constraints to zoom in Chip Array to macrocell mode.
2. Select Port "ce" and drag it to "G9" in Chip Array, as shown in Figure 4-4.
3. Port "ce" location is displayed as G9.

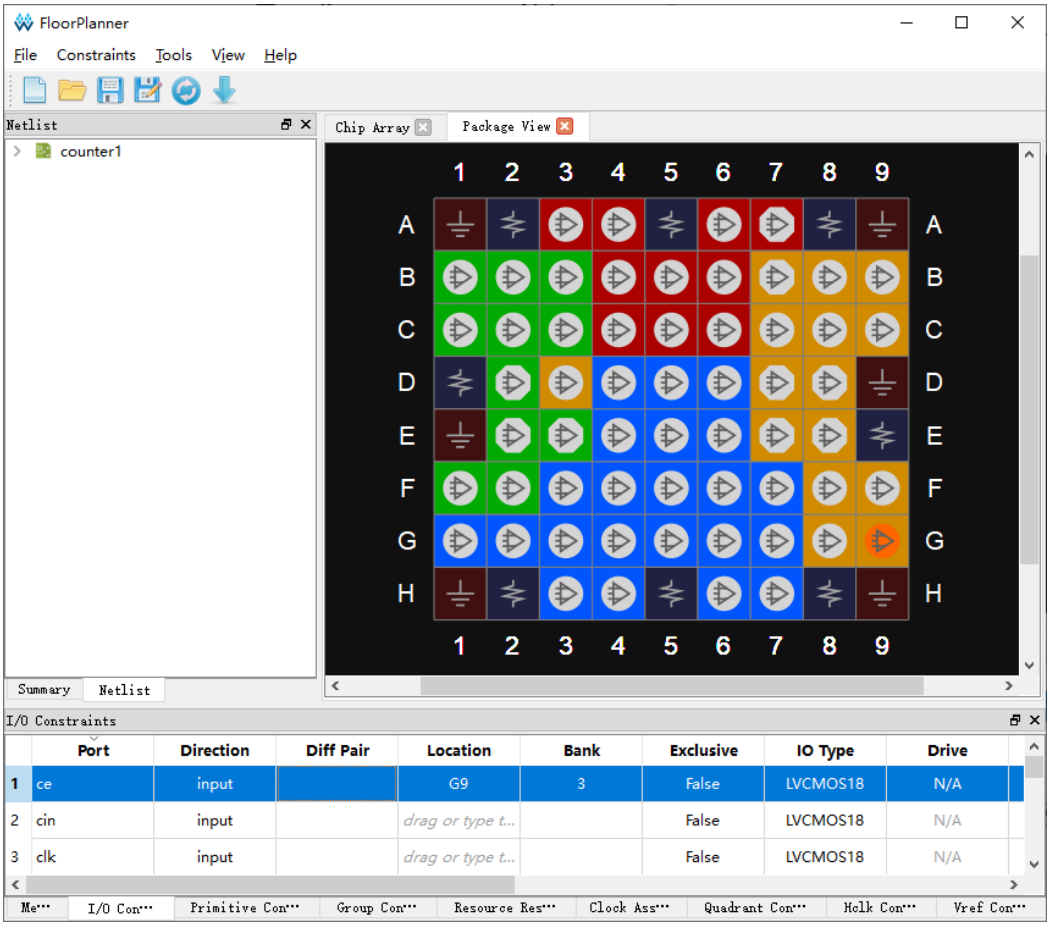
Figure 4-4 Drag to Chip Array to Create I/O Constraints



Drag to Package View to create I/O constraints.

1. Click IO Constraints.
2. Select Port "ce" and drag it to "G9" in Package View, as shown in Figure 4-5.
3. Location for Port "ce" is displayed as G9.

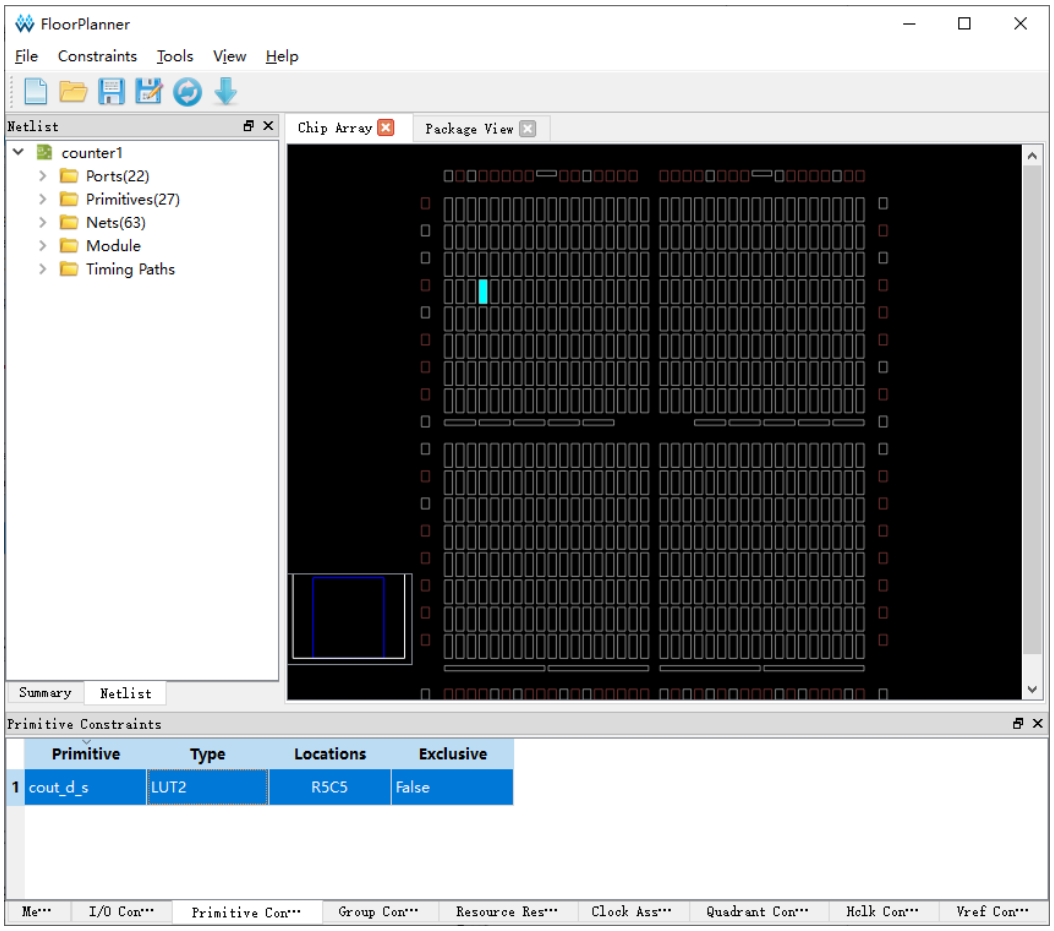
Figure 4-5 Drag to Package View to Create I/O Constraints



4.2.3 Edit Primitive Constraints

1. You can right-click the menu in "Primitive Constraints" and select "Select Primitives", then "Select Primitives" dialog box pops up. You can select Primitive "cout_d_s" and click "OK".
2. Select the created primitive constraints and drag it to "R5C5" in Chip Array, as shown in Figure 4-6.
3. Location for primitive "cout_d_s" is displayed as R5C5.

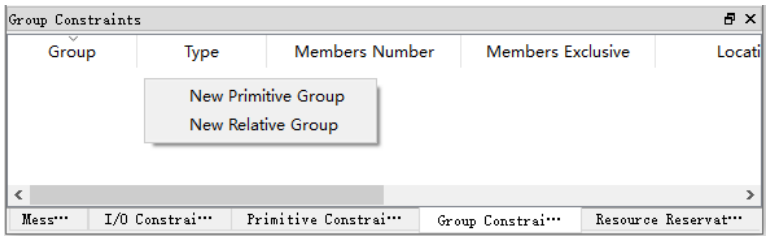
Figure 4-6 Drag to Chip Array to Create Primitive Constraints



4.2.4 Edit Group Constraints

As shown in Figure 4-7, you can create Primitive Group and Relative Group by right-clicking in Group Constraints.

Figure 4-7 Group Constraints Right-clicking



Create Primitive Group Constraints

1. Right-click "Group Constraints" and click "New Primitive Group", then "Edit Primitive Group" pops up.
2. Enter "grp1" and click "  ", then "Select Primitives" pops up.
3. Select "n14_s0" and "n14_s"; click "OK", then add them to Members

list.

4. Enter "R9C7" in "Locations", as shown in Figure 4-8.
5. Click "OK" in "New Primitive Group" diaog box to create primitive group constraints, as shown in Figure 4-9.

Figure 4-8 Create Primitive Group Constraints

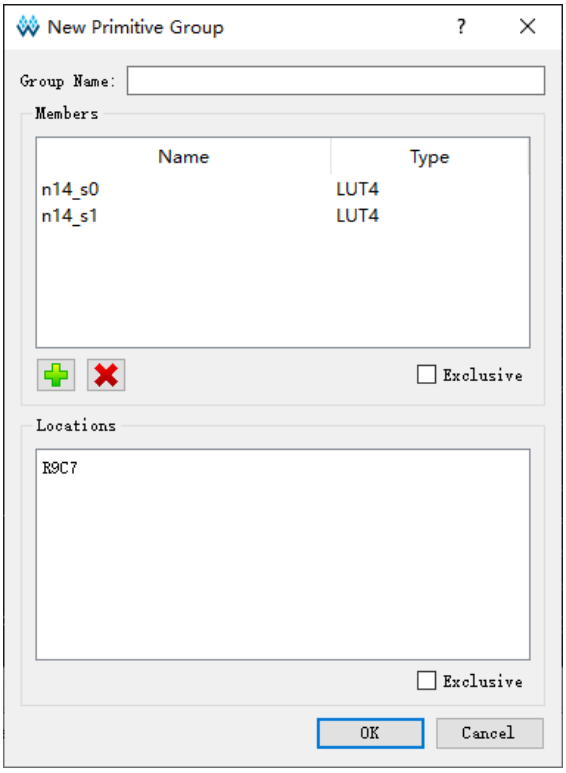
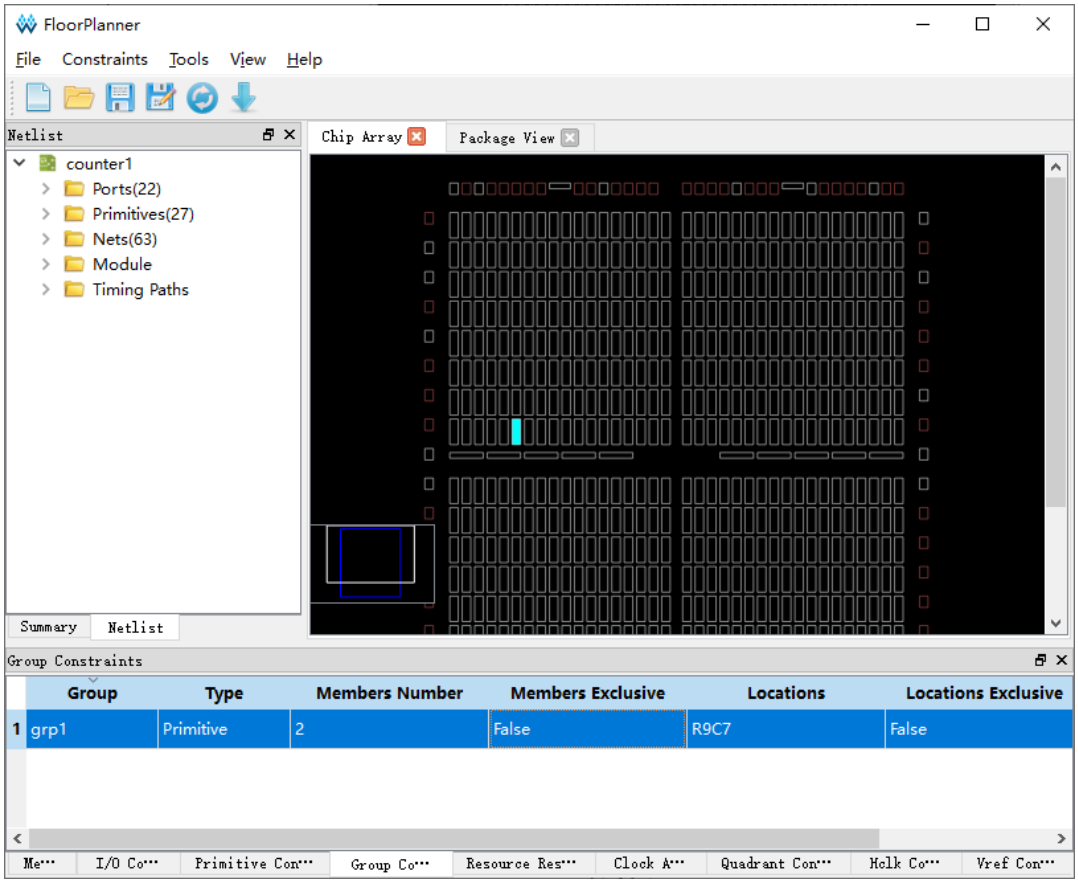


Figure 4-9 Primitive Group Constraints



Note!

The location in Primitive Group Constraints can only be entered manually or copied from Chip Array, and cannot be generated by dragging

Create Relative Group Constraints

1. Right-click "Group Constraints" and click "New Relative Group", and "New Relative Group" pops up.
2. Enter "rel_grp" and click "", and "Select Primitive" pops up.
3. Select the primitives "cout_d_s" and "n14_s0" in "Select Primitive" and click "OK", then add them to the Member list.
4. Add "R0C0" and "R4C5" to the Primitives, as shown in Figure 4-10.
5. Click "OK" in "New Relative Group" to create relative primitive group constraints, as shown in Figure 4-11.

Figure 4-10 Create Relative Group Constraints

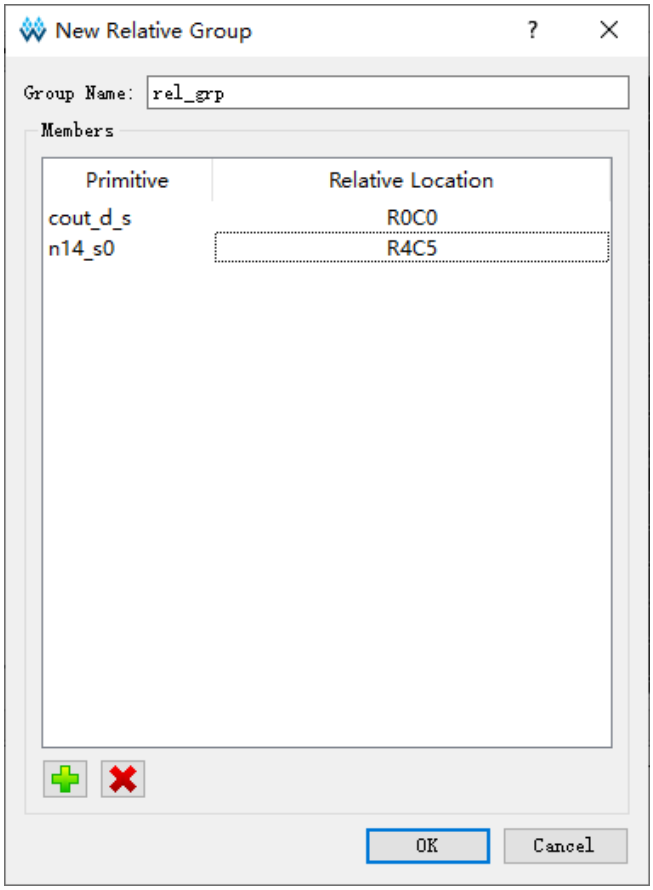
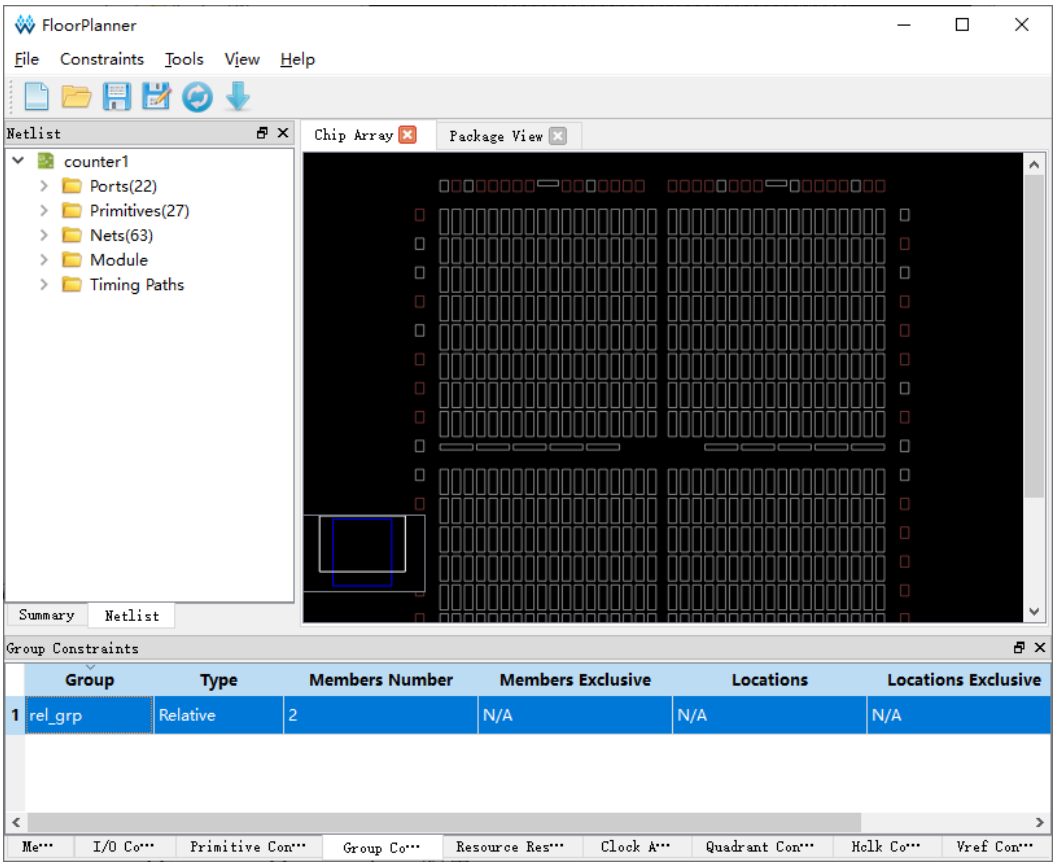


Figure 4-11 Relative Group Constraints



4.2.5 Eidt Resource Reservation Constraints

1. Right-click "Resource Reservation" and click "Reserve Resources" to add resource reservation constraints, as shown in Figure 4-12.
2. Select the created resource reservation constraints and drag it to a location in Chip Array. As shown in Figure 4-13, drag to BSRAM_R10[1] to generate constraints.

Figure 4-12 Create Resource Reservation

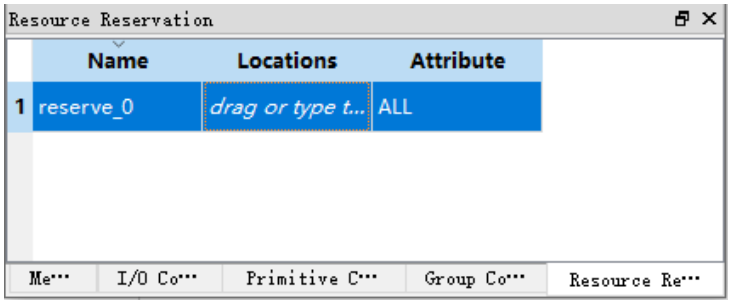
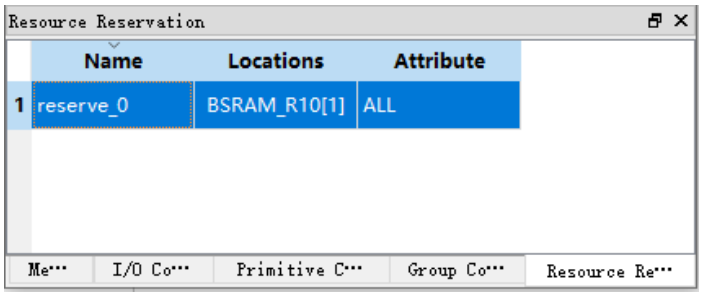


Figure 4-13 Resource Reservation



4.2.6 Edit Clock Assignment

1. Right-click "Clock Assignment" and select "Clock Assignment", then "Clock Assignment" dialog box pops up.
2. Click "  " and "Select Net" dialog box pops up. Select a Net and click "OK".
3. Select clock type and set signal type, as shown in Figure 4-14.
4. Click "OK" to add constraints to Clock Assignment, as shown in Figure 4-15.

Figure 4-14 Create Clock Assignment Constraints

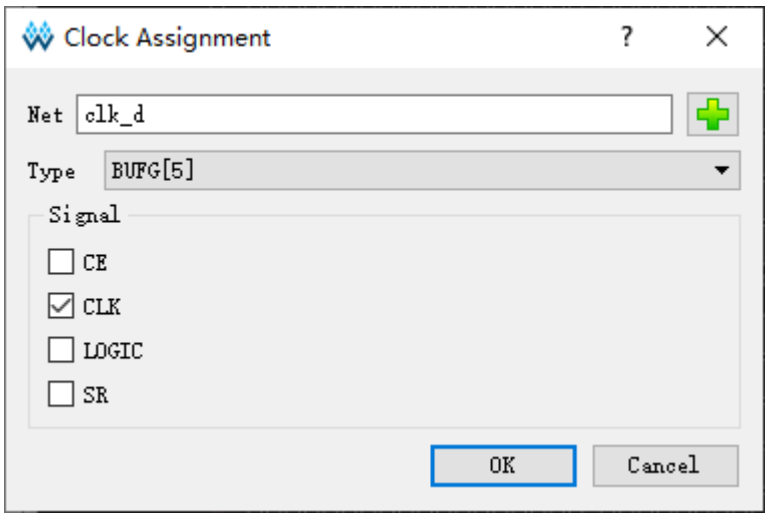
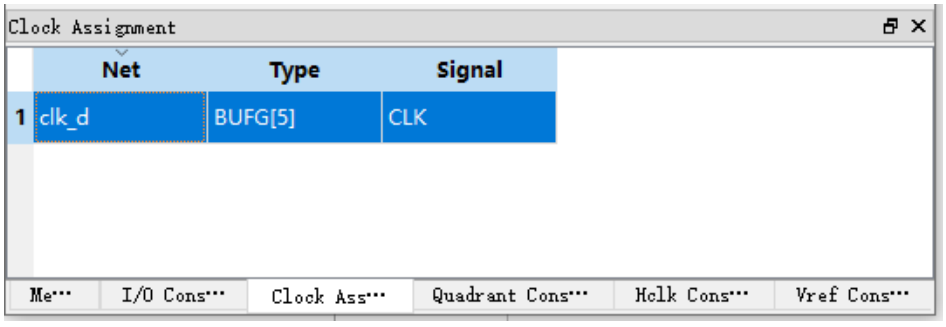


Figure 4-15 Clock Assignment Constraints



4.2.7 Edit Quadrant Constraints

Quadrant Constraints only support DCS and DQCE constraints.

1. Right-click "Quadrant Constraints" and select "Select Dcs/Dqce", then "Quadrant Constraints" dialog box pops up.
2. Click "" and "Dcs/Dqce" pops up. Select "Instance" and click "OK" in Dcs/Dqce.
3. Select the quadrant in "Position", as shown in Figure 4-16.
4. Click "OK" to add this constraint to Quadrant Constraints, as shown in Figure 4-17.

Figure 4-16 Create Quadrant Constraints

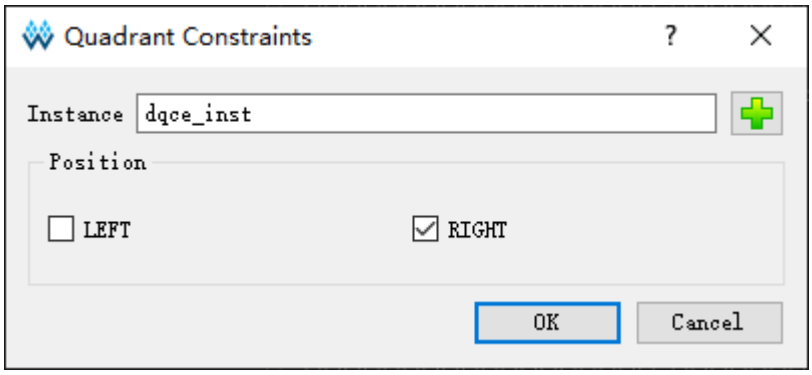
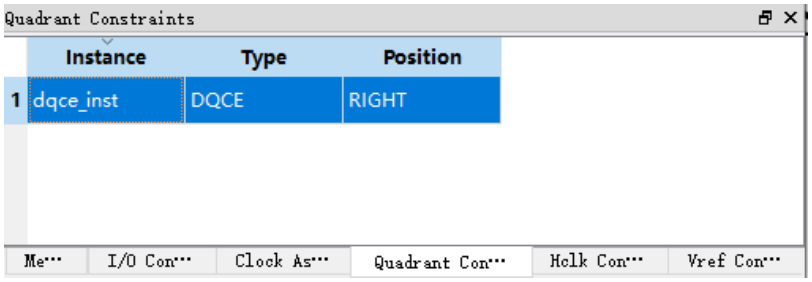


Figure 4-17 Quadrant Constraints



4.2.8 Edit Hclk Constraints

Hclk Constraints only support CLKDIV and DLLDLY constrains.

The steps are as follows.

1. Right-click "Hclk Constraints" and select "Select Hclk", then "Hclk Constraints" pops up.
2. Click "" and "Hclk Constraints" dialog box pops up, then click "OK".
3. Select a position in "Position", as shown in Figure 4-18.

4. Click "OK" to add the constraints to Hclk Constraints, as shown in Figure 4-19.

Figure 4-18 Create Hclk Constraints

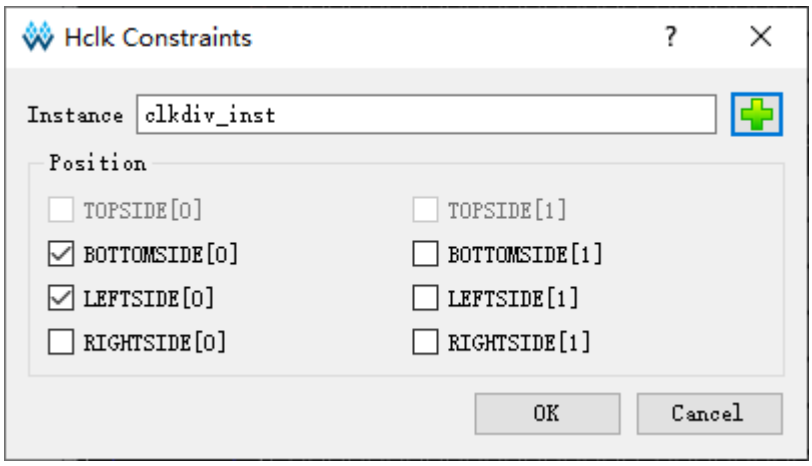
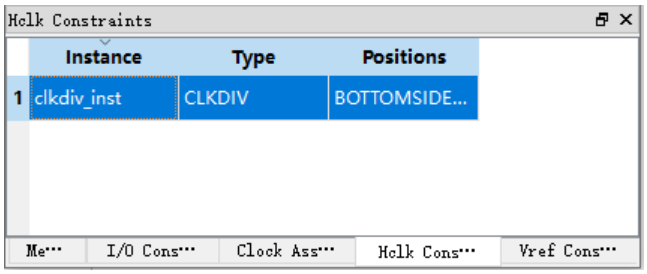


Figure 4-19 Hclk Constraints

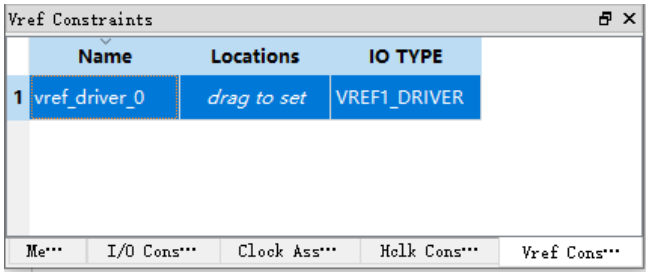


4.2.9 Edit Vref Constraints

Drag to Chip Array to create Vref Constraints.

1. Right-click Vref Constraints and select "Define Vref Driver" to add the constraints to Vref Constraints, as shown in Figure 4-20.
2. Zoom in Chip Array to macrocell mode. Select the created Vref Constraints and drag it to B7 in Chip Array. The location of the Vref Constraints is displayed as "B7", as shown in Figure 4-22.

Figure 4-20 Create Vref Constraints



You can customize Vref constraint name, but duplicate names are not allowed; if there are duplicate names, you will be prompted, as shown in Figure 4-21.

Figure 4-21 Prompt

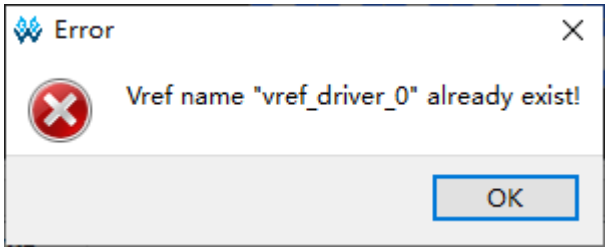
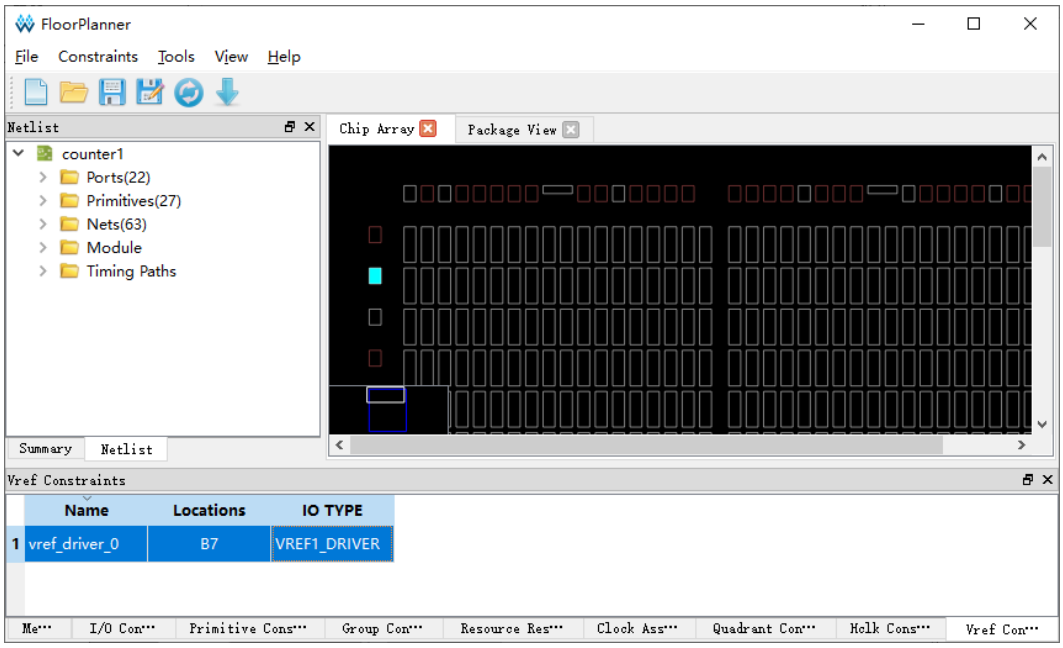


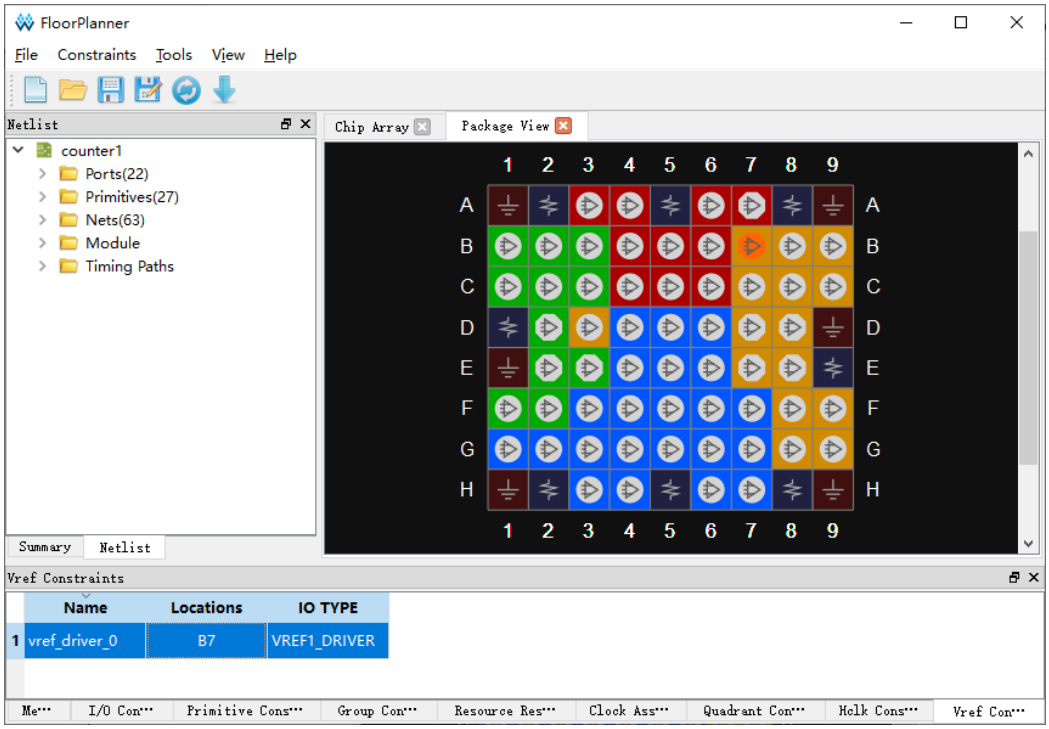
Figure 4-22 Drag to Chip Array to Generate Vref Constraints Location



Drag to Package View to create Vref constraints.

1. Right-click Vref Constraints and select "Define Vref Driver" to add the constraints to Vref Constraints, as shown in Figure 4-20.
2. Select the newly created Vref Constraints and drag it to B7 in Package View. The location of the Vref Constraints is displayed as "B7", as shown in Figure 4-23.

Figure 4-23 Drag to Package View to Generate Vref Constraints Location



5 Timing Adjustment

FloorPlanner supports timing adjustment and helps users to realize timing closure by physical location constraints and key path modification, etc.

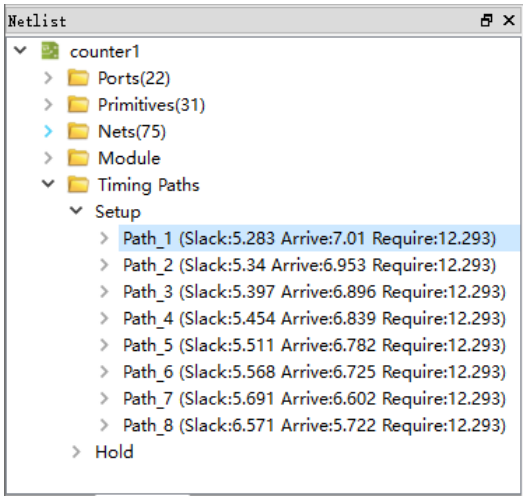
The steps to optimize timing using FloorPlanner are as follows.

1. Create a new project.
2. Run Synthesize to generate the netlist file with the .vg extension after synthesis.
3. Add physical constraints file and timing constraints file. Physical constraints and timing constraints are not a must, but they are recommended to be added for better project implementation.
4. Run Place & Route to generate posp and timing path files.
5. Read the timing report to check whether the max. frequency meets the requirements or not. If it is not, you need to use FloorPlanner to generate multi-constraints and multi-iterations to realize timing closure.
6. Run Place & Route to start FloorPlanner. The information about critical path is listed in "Netlist > Timing Paths", including Slack, Arrival time, Required time, etc., as shown in Figure 5-1.

Note!

In debugging, you do not need to start FloorPlanner repeatedly. You can reload the routing & placement file and the timing path file by clicking "Reload".

Figure 5-1 Read Timing Path



7. In debugging, you need to find the critical path by modifying the design or placement to realize timing closure. In FloorPlanner, you can adjust locations to realize timing closure. The steps are as follows.
   - Check the critical path signal flow.
     In timing closure debugging, the critical path signal flow is an important factor. Right-click Place View > All Instance in Chip Array to show the project place view. Select a critical path in the "Netlist", right-click and select "Highlight", as shown in Figure 5-2. The signal flow of this path can be observed in Chip Array, as shown in Figure 5-3.
   - Adjust improper locations.
     As shown in Figure 5-3, the locations are centralized, and only one locates relatively far. The winding path with a large span can influence the timing. You can adjust the improper location by dragging to optimize the winding path, as shown in Figure 5-4.
8. Rerun Place & Route to view the timing result. If the frequency does not meet the requirements, repeat from step 5 to step 7.

Figure 5-2 Highlight Key Path

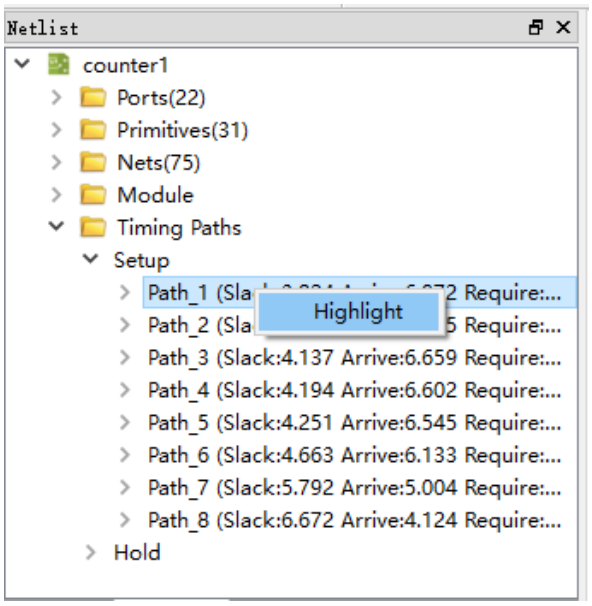


Figure 5-3 Key Path Signal Flow

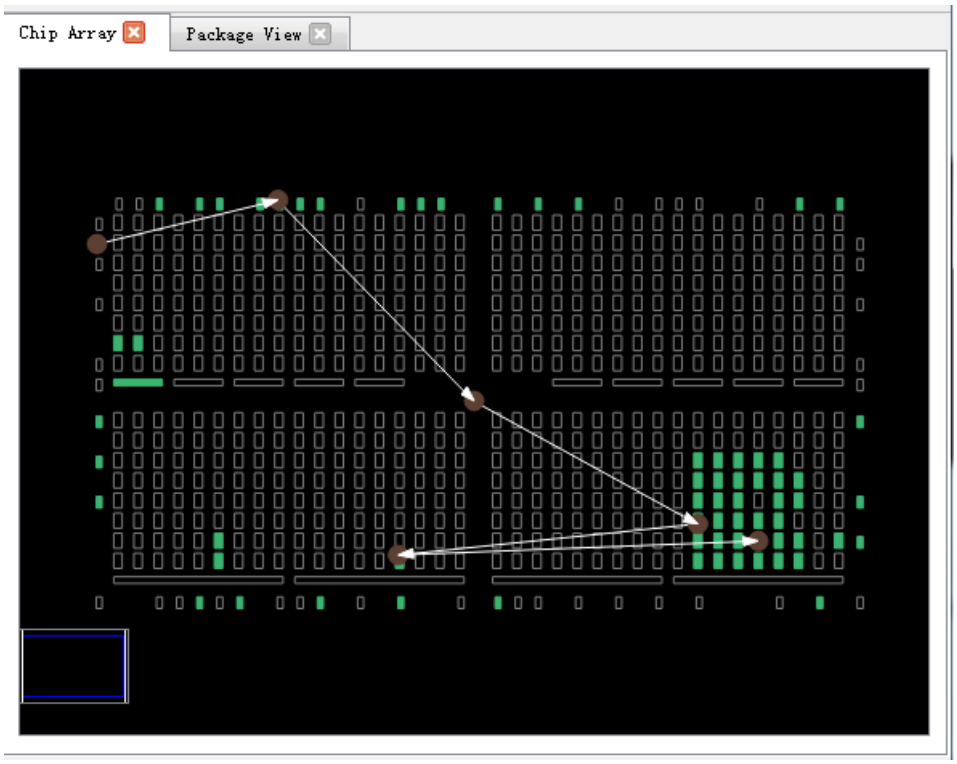
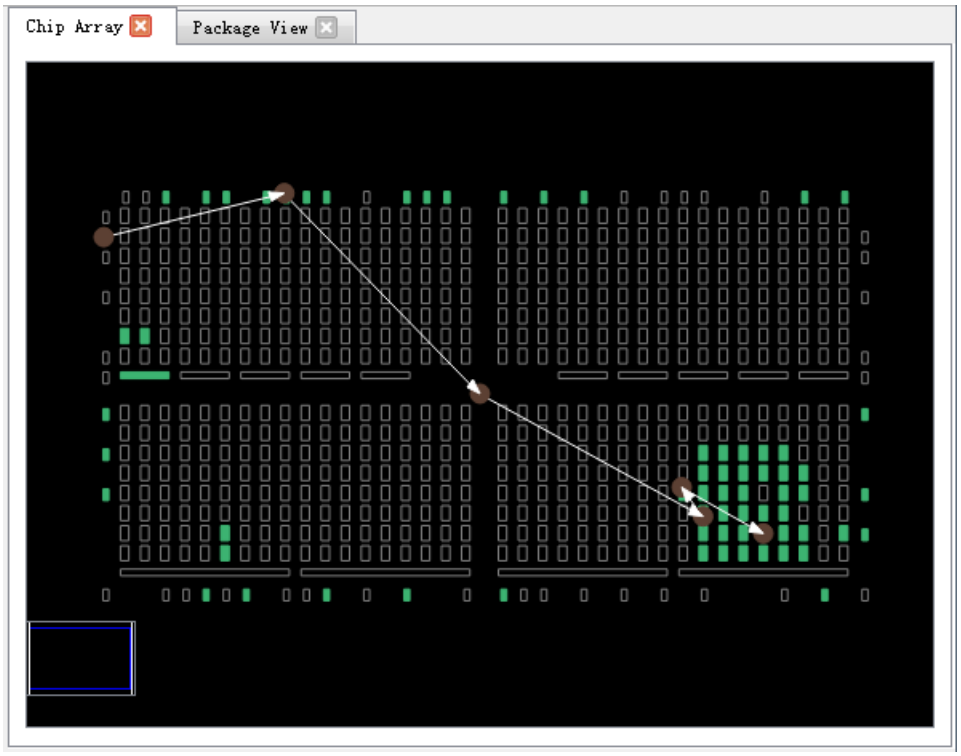


Figure 5-4 Path after Adjustment



Appendix A Physical Constraints Syntax Definition

A.1 I/O Constraints

The IO constraints can constrain port and Buffer to the specified IOB location.

Syntax

"IO_LOC" """obj_name""" obj_location ["exclusive"] ";"

Constraints Elements

obj_name

Obj_name can be the name of port and Buffer.

obj_location

Obj_location is the IOB location, such as "A11", "B12", etc. If multiple locations are specified, they need to be separated by commas, such as "A11, B2".

exclusive

Exclusive is optional, which indicates that the obj_location in the constraints can only place the primitives specified by obj_name after locations constraints.

Note!

If obj_name is the escaped name format (begin with backslash and end with space), the obj_name must be quoted on both sides.

Examples

Example 1

IO_LOC "io_1" A1;

// io_1 should be located to the pin A1.

Example 2

IO_LOC "io_1" A1, B14, A15;

// io_1 should be located to the pin A1, pin B14, or pin A15, one of the three locations will be taken for the placement.

Example 3

IO_LOC "io_2" A1 exclusive;

// io_2 should be located to the pin A1, and pin A1 can only be used by io_2.

Example 4

IO_LOC "io_2" A1, B14, A15 exclusive;

// io_2 should be located to pin A1, B14, or A15, and all these locations can only be used by io_2.

A.2 PORT Constraints

Port attributes constraints can set attribute values for ports, such as IO_TYPE, PULL_MODE and DRIVE, etc. You can see *DS102, GW2A series of FPGA Products Data Sheet* for the details.

Syntax

IO_PORT “port_name” attribute = attribute_value;

Multiple attributes can be set in a constraint statement. Each attribute can be separated by spaces.

Constraints Elements

It needs to constrain the port name, attribute and attribute value.

Examples

Example 1

IO_PORT "port_1" IO_TYPE = LVTTL33;

// Set the IO_TYPE as "LVTTL33".

Example 2

IO_PORT "port_2" IO_TYPE = LVTTL33 PULL_MODE =KEEPER;

// Set the IO_TYPE as the LVTTL33, PULL_MODE value is "KEEPER".

Example 3

IO_PORT "port_3" IO_TYPE = LVDS25;

// Buffer at port_3 is IBUF, and convert the IBUF to TLVDS_IBUF via the constraints.

A.3 Primitive Constraints

Primitive Constraints are used to place the instances to the specified GRIDs. LUT/BSRAM/SSRAM/DSP/PLL/DQS instances can be constrained using Primitive Constraints.

Syntax

"INS_LOC" """ obj_name""" obj_location ["exclusive"];"

Constraints Elements

obj_name

The instance name

obj_location

obj_location includes:

- A signal location is specified to LUT, such as, RxCy[0-3][A-B];
- A range of the locations are specified to the multiple rows or columns:
  - Include multiple CLS or LUT: "RxCy", "RxCy[0-3]"
  - Specify multiple rows: "R[x:y]Cm", "R[x:y]Cm[0-3]", "R[x:y]Cm[0-3][A-B]"
  - Specify multiple columns: "RxC[m:n]", "RxC[m:n][0-3]", "RxC[m:n][0-3][A-B]"
  - Specify multiple rows and columns: "R[x:y]C[m:n]", "R[x:y]C[m:n][0-3]", "R[x:y]C[m:n][0-3][A-B]"

Note!

Multiple ins_locations can be included in a constraint statement, and they are separated by ",".

PLL Constraints Location

For the "PLL_L" or "PLL_R" of the PLL constraints locations, if more than one PLL are placed on the left side, it can be set to "PLL_L[0]", "PLL_L[1]" ...; If more than one PLL are placed on the right side, it can be set to "PLL_R[0]", "PLL_R[1]" ...

BSRAM Constraints Location

The BSRAM constraints location is "BSRAM_R10[0]" (the first BSRAM at row 10), "BSRAM_R10[1]"….

DSP Constraints Location

The DSP constraints location is "DSP_R19[0]" (the first DSP Block at row 19), "DSP_R19[1]"… If it specifies a macro, it can be marked as: DSP_R19[0][A] or DSP_R19[0][B].

exclusive

Exclusive is optional, which indicates that the obj_location in the constraints can only place the instance specified by obj_name after locations constraints.

Examples

Example 1

INS_LOC "lut_1" R2C3, R5C10[0][A];

// lut_1 is constrained at the R2C3 and the first CLS of the R5C10 in the first LUT.

Example 2

INS_LOC "ins_2 " R5C6[2] exclusive;

// ins_2 is constrained at the third CLS of the R5C6, and only the instance can be placed at this location.

Example 3

INS_LOC "ins_3" R[2:6]C1;

// ins_1 is constrained between the row 2 and the row 6 and in the column 1.

Example 4

INS_LOC "ins_4" R[1:4]C[2:6] exclusive;

// ins_3 is constrained between row 2 and row 5, between column 3 and column 7. This location can only be occupied by this instance.

Example 5

INS_LOC "ins_5" R[1:4]C[2:6][1];

// ins_4 is constrained between row 2 and row 5, and in the second CLS of a GRID between column 3 and column 7.

Example 6

INS_LOC "reg_name" B14;

// It is constrained to the IOB B14 by REGISTER/IOLOGIC INS_LOC constraint.

Example 7

INS_LOC "pll_name" PLL_L;

// It is constrained to the PLL left by INS_LOC constraint.

Example 8

INS_LOC "bsram_name" BSRAM_R10[2];

// It is constrained to the third BSRAM in row 10 by INS_LOC constraint.

Example 9

INS_LOC "dsp_name" DSP_R19[2];

// It is constrained to the third DSP in row 19 by INS_LOC constraint.

A LUT1/LUT2/LUT3/LUT4 can be placed in LUT4. A LUT5 needs to occupy two LUT4s (one CLS). A LUT6 needs to occupy four LUT4s (two CLSs). A LUT7 needs to occupy four CLSs (one GRID). A LUT8 needs to occupy eight CLSs (two GRIDs). Therefore, for different instance constraints, the minimum unit of the constraint location is also different. For BSRAM/SSRAM/DSP (one DSP includes two MACROs and one MACRO includes two UNITs), the example is as follows.

Example 10

LUT4 Constraints

INS_LOC "lut4_name" R5C15[1][A];

// lut4_name is constrained to the second LUT in the first CLS of the R5C15.

Example 11

CLS Constraints

INS_LOC "lut5_name" R5C15[3];

// lut5_name is constrained to the fourth CLS of the R5C15.

Example 12

CLS Constraints

INS_LOC "lut6_name" R5C15[0];

// lut6_name is constrained to the first CLS of the R5C15 (the CLS[0] and CLS[1] will be occupied).

Example 13

GRID Constraints

INS_LOC "lut7_name" R5C15;

// lut7_name is constrained to the R5C15, and the LUT7 will occupy one GRID.

Example 14

GRID Constraints

INS_LOC "lut8_name" R5C15;

// lut8_name is constrained to the R5C15; lut8_name will occupy R5C15 and the R5C16.

Example 15

DSP MACRO Constraints

INS_LOC "mult_name" DSP_R19[1][A];

// mult_name is constrained to the first macro of the second DSP in row 19.

A.4 Group Constraints

The group constraints include Primitive Group Constraints and Relative Group Constraints.

A.4.1 Primitive Group Constraints

Primitive Group Constraint is used to define a group constraint. A group is a collection of various instance objects. The instances such as LUT, DFF, etc., or Buffer, IOLOGIC, etc. can be added to a group using the Primitive Group constraints. And the location constraints of all objects in

the group can be achieved by constraining the location of the group.

Syntax

Definition of GROUP:

GROUP group_name = { “obj_names ” } [exclusive];

Add the instance to the group:

GROUP group_name += { “obj_names ” } [exclusive];

The location of the group is constrained:

GRP_LOC group_name group_location[exclusive];

Note!

If group_name is the escaped name format (begin with backslash and end with space), the quotes at two sides of group_name are necessary.

Constraints Elements

group_name

Define a name as the name of the group.

obj_name

Obj_name is used to add the specified instance to the group.

group_location

Specify the constraints location of the group, and the group_location can at the IOB and the GRID.

exclusive

The "exclusive" is optional, which is at the end of the group definition or the location constraints;

An object can be included in multiple groups, but the object can only be included in the group that the "exclusive" is added;

The "exclusive" indicates that the constraints location can only be occupied by the objects in the group.

Examples

Example 1

GROUP group_1 = { "ins_1" "ins_2" "ins_3" "ins_4" };

// Create a group named group_1 and add the ins_1, ins_2, ins_3, ins_4 to the group.

Example 2

GROUP group_2 = { "ins_5" "ins_6" "ins_7" } exclusive;

// Create a group named group_2 and the ins_5, ins_6, ins_7 only can be added to this group.

Example 3

GROUP group_1 += { "io_1" "io_2"};

// Add io_1, io_2 to group_1.

Example 4

GRP_LOC group_1 R3C4, A14, B4;

// The objects in group_1 can be placed at R3C4, A14, B4.

Example 5

GRP_LOC group_2 R[1:3]C[1:4] exclusive;

// The Instance in group_2 can be placed in the range of R[1:3]C[1:4], and the instances in group_2 can only be placed in the range.

A.4.2 Relative Group Constraints

The instance relative location constraints can be realized using the Relative Group Constraints.

Syntax

Define Relative Group Constraints:

REL_GROUP group_name = { “obj_names ” };

Add the instance to the defined group:

REL_GROUP group_name += { “obj_names ” };

The instance relative location is constrained in the group:

INS_RLOC “obj_name” relative_location;

Constraints Elements

obj_name

The name of the constraint object.

relative_location

The description of the relative locations in row and column.

Example

REL_GROUP grp_1 = { "ins_1" "ins_2" "ins_3" "ins_4" };

INS_RLOC "ins_1" R0C0;

INS_RLOC "ins_2" R2C3;

INS_RLOC "ins_3" R3C5;

// Define a group constraint named grp_1 and add the ins_1, ins_2, ins_3, ins_4 to grp_1. The ins_1 is the relative location origin R0C0, the ins_2 is constrained to the R2C3 relative to the ins_1, and the ins_3 is constrained to the R3C5 relative to ins_1.

A.5 Resource Reservation Constraints

The specified location or range can be reserved using the Resource Reservation constraints.

Syntax

"LOC_RESERVE" location [res_obj] ";"

Examples

Example 1

LOC_RESERVE R2C3[0][A] -LUT;

LOC_RESERVE R2C3[0][A] -REG;

Example 2

LOC_RESERVE IOR3, IOR6, R2C3, R3C4;

Example 3

LOC_RESERVE R[2:5]C[3:6], R3C[8:9];

// The locations constraints in the above examples will be reserved during placement.

A.6 Vref Constraints

The chip supports the external reference voltage, which is valid for the BANK. The Vref Constraints can be used to constrain the name and location of the input pin of the external reference voltage.

Note!

- The input pin location where the external reference voltage can be set must have IOLOGIC resource.
- Vref Constraints and PORT constraints are valid when used together. When a single-ended input or inout port with IO Type SSTL/HSTL, the Vref attribute can be set to the created Vref Constraints, indicating that the reference voltage of this port uses the external reference voltage input from the Vref Constraints location.

Syntax

"USE_VREF_DRIVER" vref_name [location]";"

Constraints Elements

vref_name

Customized VREF pin name

location

Any IO location with IOLOGIC in the device can be used as a location for the VREF pin constraints.

Examples

Example 1

USE_VREF_DRIVER vref_pin;

IO_PORT “port_1” IO_TYPE = SSTL25_I VREF=vref_pin;

IO_PORT “port_2” IO_TYPE = SSTL25_I VREF=vref_pin;

// Define a VREF pin named "vref_pin" and set the port_1 and port_2 to vref_pin.

Example 2

USE_VREF_DRIVER vref_pin C7;

IO_PORT “port_1” IO_TYPE = SSTL25_I VREF=vref_pin;

IO_PORT “port_2” IO_TYPE = SSTL25_I VREF=vref_pin;

// Define a VREF pin named "vref_pin" and constrain it to C7. Set the VREF of port_1 and port_1 as vref_pin, and port_1 and port_1 will be placed in the bank where C7 locates.

A.7 Quadrant Constraints

The Quadrant Constraints is used to constrain objects such as DCS/DQCE to a specified quadrant.

Syntax

INS_LOC “obj_name” quadrant;

Constraints Elements

obj_name

The name of the constraint object.

quadrant

LittleBee® family: GW1N-9, GW1NR-9, GW1N-9C, GW1NR-9C can constrain 4 quadrants of "TOPLEFT", "TOPRIGHT", "BOTTOMLEFT", "BOTTOMRIGHT"; other devices can only constrain 2 quadrants of "LEFT", "RIGHT".

Arora family can constrain 4 quadrants of "TOPLEFT", "TOPRIGHT", "BOTTOMLEFT", "BOTTOMRIGHT".

Example

INS_LOC "dcs_name" LEFT;

// Constrain the DCS dcs_name to the LEFT quadrant.

A.8 Clock Assignment Constraints

The clock assignment constrains a specific net to the global clock wire or non-wire clock in the design. There are eight BUFGs and eight BUFSs in each quadrant of the chip resources. It can constrain the global clock wire for specific fanout (CLK/CE/SR/LOGIC) of the net.

- BUFG[0-7] represents the eight BUFGs.
- BUFS represents BUFS.
- LOCAL_CLOCK means this net is not to route the clock wire.

The CLK signal is the signal connected to the clock pin. The CE signal is the signal connected to the clock enable pin. The SR signal is the signal connected to the SET/RESET/CLEAR/PRESET pins, and the LOGIC is the signal connected to logic input pins.

Syntax

CLOCK_LOC “net_name” global_clocks = fanout ;

Constraints Elements

net_name

The net name

global_clocks

BUFG[0-7] represents the eight BUFGs.

BUFS represents BUFS.

LOCAL_CLOCK means this net is not to route clock wire.

fanout

CLK: fanout is the net of the clock pin.

CE: fanout is the net of the clock enable.

SR: fanout is the net of SET/RESET (synchronous reset signal), CLEAR/PRESET (asynchronous reset signal).

LOGIC: fanout is the net other than the fanout above.

The sign "|" can be used to separate multiple specified fanout.

Note!

If LOCAL_CLOCK is selected for LOCAL_CLOCK, fanout is not available.

Examples

Example 1

CLOCK_LOC "net" BUFG[0] = CLK;

// Constrain the net fanout as the clock pin net routing to the first BUFG.

Example 2

CLOCK_LOC "net" BUFG = CLK|CE;

NET_LOC "net" BUFG = CLK|CE;

// Constrain the net fanout as the clock pin/clock enable net routing to BUFG.

Example 3

CLOCK_LOC "net" BUFS = CE;

NET_LOC "net" BUFS = CE;

// Constrain the net fanout as the clock enable net routing to BUFS.

Example 4

CLOCK_LOC "net" LOCAL_CLOCK;

// Constrain the net not to route the clock line.

A.9 Hclk Constraints

The CLKDIV/DLLDLY can be constrained to the relevant locations via the CLKDIV/DLLDLY constraints. The constraints locations of CLKDIV/DLLDLY are different from the ones of other general instances. The "TOPSIDE", "BOTTOMSIDE", "LEFTSIDE", and "RIGHTSIDE" indicate the four sides of the constraints location.

Syntax

INS_LOC "obj_name" location;

Constraints Elements

obj_name

The instance name of the CLKDIV/DLLDLY is the obj_name.

location

"TOPSIDE[0-1]"

"BOTTOMSIDE[0-1]"

"LEFTSIDE[0-1]"

"RIGHTSIDE[0-1]"

Example

INS_LOC "clkdiv_name" TOPSIDE[0];

// Place the clkdiv_name to TOPSIDE[0].

A.10 Other Constraints

A.10.1 JTAGSEL_N net Constaint

When the internal logic of the FPGA is used to control JTAGSEL_N functions, i.e., during the second download without power off, pull down JTAGSEL_N so that JTAG can be switched to the configuration function, and net's physical constraints of JTAGSEL_N need to be added. For the details, you can refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

Syntax

NET_LOC "obj_name" V_JTAGSEL_N;

Constraint Element

obj_name

Any net of the internal logic as obj_name.

Example

NET_LOC "netname" V_JTAGSELN;

// The netname net is used to control the functions of JTAGSEL_N.

A.10.2 RECONFIG_N net Constaint

When the internal logic of the FPGA is used to control RECONFIG_N functions, i.e., during the second download without power off, pull down RECONFIG_N so that JTAG can be switched to the configuration reset function, and net's physical constraints of RECONFIG_N need to be added. For the details, you can refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

Syntax

NET_LOC "obj_name" V_RECONFIGN;

Constraint Element

obj_name

Any net of internal logic as obj_name.

Application examples

Example

NET_LOC "netname" V_RECONFIGN;

// Use this netname to control the RECONFIG_N function.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