GW1N series of FPGA Products

Package & Pinout User Guide

UG103-2.6E, 01/20/2022

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Revision History

Date	Version	Description
03/03/2016	1.05E	Initial version.
04/16/2020	2.0E	GW1N-2/GW1N-2B/GW1N-6 removed.
07/08/2020	2.1E	● GW1N-9 MG100 added. ● GW1N-9 QN48F added.
07/30/2020	2.1.1E	● "Table 3-60 Other Pins in GW1N-9 UG332" updated; ● View of GW1N-9 QN48F Pins Distribution added.
12/31/2020	2.2E	The new device of GW1N-2 added.
01/22/2021	2.2.1E	GW1N-2 QN48/QN48M added.
03/02/2021	2.2.2E	GW1N-2 MG132 added.
04/19/2021	2.3E	The new device of GW1N-1P5 added.
05/20/2021	2.4E	● GW1N-1P5 LQ100 added; ● GW1N-2 MG132/LQ100/LQ144 added, and MG132 renamed to MG132H, QN48M renamed to QN48H. ● GW1N-9 MG100T added; ● GW1N-1 LQ100X removed.
07/16/2021	2.4.1E	GW1N-2 MG121/MG121X added.
08/26/2021	2.4.2E	EQ144 and EQ176 package outlines updated.
10/28/2021	2.5E	● GW1N-2 MG49 and GW1N-1P5 FN48X added; ● GWN1-1 QN32, QN48, LQ100, and LQ144 removed.
01/20/2022	2.6E	● GW1N-2 QN32X, QN88, and CS42H added; ● GW1N-1P5 FN48X removed; GW1N-1P5 QN48X added.

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1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1N series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guidelines are available on GOWINSEMI website at www.gowinsemi.com:

1. UG290, Gowin FPGA Products Programming and Configuration User Guide
2. DS100, GW1N series of FPGA Products Datasheet
3. UG107, GW1N-1 Pinout
4. UG167, GW1N-1S Pinout
5. UG171, GW1N-2 Pinout
6. UG105, GW1N-4 Pinout
7. UG114, GW1N-9 Pinout
8. UG174, GW1N-1P5 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies that are used in this manual are described in Table 1-1.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
CS	WLCSP
QN	QFN
FN	QFN
CM	WLCSP
MG	MBGA
LQ	LQFP
EQ	ELQFP
PG	PBGA256
UG	UBGA

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly via the following channels.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW1N series of FPGA Products are the first-generation products of GOWINSEMI® (LittleBee®) family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

The GW1N series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW1N series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package and Max. User I/O Information, and LVDS Pairs

Package	Pitch(mm)	Size(mm)	Max. User I/O (LVDS Pairs)					
			GW1N-1S	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
CS30	0.4	2.3 x 2.4	23	24	-	-	-	-
QN32	0.5	5 x 5	-	-	-	-	24（3）	-
QN32X	0.5	5 x 5	-	-	-	21（1）	-	-
FN32	0.4	4 x 4	25	-	-	-	-	-
CS42	0.4	2.4 x 2.9	-	-	-	24（7）	-	-
CS42H	0.4	2.4 x 2.9	-	-	-	21（3）	-	-
QN48	0.4	6 x 6	-	-	-	40（12）	40（9）	40（12）
QN48H	0.4	6 x 6	-	-	-	30（8）	-	-
QN48F	0.4	6 x 6	-	-	-	-	-	39（11）
QN48X	0.5	7 x 7	-	-	39（10）	-	-	-
CM64	0.5	4.1 x 4.1	-	-	-	-	-	55（16）
CS72	0.4	3.6 x 3.3	-	-	-	-	57（19）	-
CS81M	0.4	4.1 x 4.1	-	-	-	-	-	55（15）
QN88	0.4	10 x 10	-	-	-	57（17）	70（11）	70（19）
LQ100	0.5	14 x 14	-	-	80（16）	80（15）	79（13）	79（20）
LQ100X	0.5	14 x 14	-	-	80（16）	80（15）	-	-
MG49	0.5	3.8 x 3.8	-	-	-	42（11）	-	-

Package	Pitch(mm)	Size(mm)	Max. User I/O (LVDS Pairs)					
			GW1N-1S	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
MG100	0.5	5 x 5	-	-	-	-	-	87（25）
MG100T	0.5	5 x 5	-	-	-	-	-	87（17）
MG121	0.5	6 x 6	-	-	-	100（28）	-	-
MG121X	0.5	6 x 6	-	-	-	100（28）	-	-
MG132	0.5	8 x 8	-	-	-	104（29）	-	-
MG132H	0.5	8 x 8	-	-	-	94（29）	-	-
MG132X	0.5	8 x 8	-	-	-	104（29）	105（23）	-
LQ144	0.5	20 x 20	-	-	-	113（28）	119（22）	120（28）
LQ144X	0.5	20 x 20	-	-	-	113（28）	-	-
EQ144	0.5	20 x 20	-	-	-	-	-	120（28）
MG132X	0.5	8 x 8	-	-	-	-	105（23）	-
MG160	0.5	8 x 8	-	-	-	-	131（25）	131（38）
UG169	0.8	11 x 11	-	-	-	-	-	129（38）
LQ176	0.4	20 x 20	-	-	-	-	-	147（37）
EQ176	0.4	20 x 20	-	-	-	-	-	147（37）
MG196	0.5	8 x 8	-	-	-	-	-	113（35）
PG256	1.0	17 x 17	-	-	-	-	207（32）	207（36）
PG256M	1.0	17 x 17	-	-	-	-	207（32）	-
UG256	0.8	14 x 14	-	-	-	-	-	207（36）
UG332	0.8	17 x 17	-	-	-	-	-	273（43）

Note!

- In this manual, abbreviations are employed to refer to the package types. See section 1.3 Abbreviations and Terminology;
- "⇔" indicates that the various device pins are compatible when the package types are the same;
- The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. The table shows the data when the four JTAG mode pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O is increased by one.

2.3 Dedicated Pins

Table 2-2 GW1N Pins

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCO4	VCCO5	VCCX
VSS	NC		

2.4 Pin Quantity

2.4.1 Quantity of GW1N-1S Pins

Table 2-3 Quantity of GW1N-1S Pins

Pin Type		GW1N-1S	
		FN32	CS30
I/O Single ended/Differential pair [1]	BANK0	5/2	5/2
	BANK1	10/5	10/5
	BANK2	10/5	8/3
Max. User I/O[2]		25	23
Differential Pair		12	10
VCC/VCCPLL		1	1
VCCO0		1	1
VCCO1		1	1
VCCO2		1	1
VSS		2	2
JTAGSEL_N		1	1

Note!

- [1]The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;

2.4.2 Quantity of GW1N-1 Pins

Table 2-4 Quantity of GW1N-1 Pins

Pin Type		GW1N-1
		CS30
I/O Single ended/Differential pair[1]	BANK0	0/0
	BANK1	10/4
	BANK2	2/1
	BANK3	11/5
Max. User I/O[2]		24
Differential Pair		10
VCC		1
VCCO0		0
VCCO1		0
VCCO2		0
VCCO3		0
VCCO0/VCCO3[3]		1
VCCO1/VCCO2[3]		2
VSS		2
MODE0		1
MODE1		0
MODE2		0
JTAGSEL_N		0
NC		0

Note!

- [1]The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing.

2.4.3 Quantity of GW1N-2 Pins

Table 2-5 Quantity of GW1N-2 Pins

Pin Type		GW1N-2																				
		CS42	MG132X[4]	MG132X[5]	LQ100X[4]	LQ100X[5]	LQ144X[4]	LQ144X[5]	QN48	QN48H	MG132H	MG132[4]	MG132[5]	LQ100X[4]	LQ100X[5]	LQ144X[4]	LQ144X[5]	MG121X[4]	MG121X[5]	MG121[4]	MG121[5]	MG49
Single-ended I/O / Differential pair/ LVDS [1]	BANK0	6/3/1	25/12/7	25/12/7	19/8/4	19/8/4	28/13/7	28/13/7	10/4/1	12/5/2	25/11/7	25/12/7	25/12/7	19/8/4	19/8/4	28/13/7	28/13/7	24/11/7	24/11/7	24/11/7	24/11/7	14/7/4
	BANK1	0/0/0	26/13/7	26/13/7	21/10/3	21/10/3	28/14/7	28/14/7	10/5/5	0/0/0	16/8/7	26/13/7	26/13/7	21/10/3	21/10/3	28/14/7	28/14/7	26/13/7	26/13/7	26/13/7	26/13/7	12/6/3
	BANK2	6/3/0	28/14/8	28/14/8	20/10/3	20/10/3	29/14/7	29/14/7	8/4/1	8/4/1	28/14/8	28/14/8	28/14/8	20/10/3	20/10/3	29/14/7	29/14/7	26/12/7	26/12/7	26/12/7	26/12/7	8/4/2
	BANK3	4/2/2	7/3/2	7/3/2	6/3/2	6/3/2	8/4/2	8/4/2	4/2/2	4/2/2	7/3/2	7/3/2	7/3/2	6/3/2	6/3/2	8/4/2	8/4/2	7/3/2	7/3/2	7/3/2	7/3/2	4/2/1
	BANK4	2/1/1	8/4/2	8/4/2	6/3/1	6/3/1	10/5/2	10/5/2	2/1/1	2/1/1	8/4/2	8/4/2	8/4/2	6/3/1	6/3/1	10/5/2	10/5/2	7/3/2	7/3/2	7/3/2	7/3/2	4/2/1
	BANK5	6/3/3	10/5/3	10/5/3	8/4/2	8/4/2	10/5/3	10/5/3	6/3/2	4/2/2	10/5/3	10/5/3	10/5/3	8/4/2	8/4/2	10/5/3	10/5/3	10/5/3	10/5/3	10/5/3	10/5/3	0/0/0
Max. User I/O [2]		24	104	104	80	80	113	113	40	30	94	104	104	80	80	113	113	100	100	100	100	42
Differential Pair		17	51	51	38	38	55	55	19	19	45	51	51	38	38	55	55	47	47	47	47	21
True LVDS Output		7	29	29	15	15	28	28	12	8	29	29	29	15	15	28	28	28	28	28	28	11
VCC		1	0	4	0	2	0	4	1	0	4	4	0	0	2	0	4	4	0	4	0	1
VCCO0		0	3	3	2	2	3	3	1	1	3	3	3	2	2	3	3	1	1	1	1	1
VCCO1		0	3	0	2	0	3	0	1	0	2	0	3	2	0	3	0	0	1	0	1	1
VCCO2		0	3	3	2	2	3	3	0	0	3	3	3	2	2	3	3	1	1	1	1	0
VCCO3		0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0
VCCO4		0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0
VCCO5		0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0
VCCX		1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

Pin Type	GW1N-2																				
	CS42	MG132X[4]	MG132X[5]	LQ100X[4]	LQ100X[5]	LQ144X[4]	LQ144X[5]	QN48	QN48H	MG132H	MG132[4]	MG132[5]	LQ100X[4]	LQ100X[5]	LQ144X[4]	LQ144X[5]	MG121X[4]	MG121X[5]	MG121[4]	MG121[5]	MG49
VCC/VCCX	0	4	0	2	0	4	0	0	0	0	0	4	2	0	4	0	0	4	0	4	0
VCC/VCCO1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
VCCO1/VCCX	0	0	3	0	2	0	3	0	0	0	3	0	0	2	0	3	1	0	1	0	0
VCCO2/VCCX	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
VCCO2/VCCO3/CCO4/VCCO5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
VCCD/VCCO1/VCCOD	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VCCD/VCCOD	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
VCCO3/CCO4/VCCO5	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
VCCO0/VCCO2[3]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VSS	2	10	10	8	8	12	12	2	2	10	10	10	8	8	12	12	10	10	10	10	2
MODE0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
MODE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MODE2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
JTAGSEL_N	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NC	0	1	1	0	0	2	2	0	0	0	1	1	0	0	2	2	0	0	0	0	0

Continued

Pin Type		GW1N-2			
		QN32[4]	QN32[5]	QN88	CS42H
Single-ended I/O / Differential pair/ LVDS [1]	BANK0	8/3/0	8/3/0	19/9/5	9/2/0
	BANK1	2/1/1	2/1/1	5/2/1	6/3/3
	BANK2	9/4/0	9/4/0	18/9/4	3/0/0

Pin Type		GW1N-2			
		QN32[4]	QN32[5]	QN88	CS42H
	BANK3	2/1/0	2/1/0	5/2/2	1/0/0
	BANK4	0/0/0	0/0/0	4/2/2	1/0/0
	BANK5	0/0/0	0/0/0	6/3/3	1/0/0
Max. User I/O [2]		21	21	57	21
Differential Pair		9	9	27	5
True LVDS Output		1	1	17	3
VCC		2	0	4	1
VCCO0		0	2	2	1
VCCO1		0	0	1	1
VCCO2		2	2	2	1
VCCO3		1	1	1	0
VCCO4		0	0	1	0
VCCO5		0	0	1	0
VCC/VCCX		0	2	0	0
VCCO0/VCCX[3]		2	0	0	0
VCCO1/VCCO4/VCCO5		1	1	0	0
VCCO3/VCCO4/VCCO5		0	0	0	1
VCCD/VCCOD		0	0	1	1
VCCX		0	0	2	2
VSS		2	2	5	3
MODE0		0	0	1	0
MODE1		0	0	1	0
MODE2		0	0	1	0
JTAGSEL_N		1	1	1	0

Pin Type	GW1N-2			
	QN32[4]	QN32[5]	QN88	CS42H
NC	0	0	0	0

Note!

- [1]The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing;
- [4] Package for LV version;
- [5] Package for UV version.

2.4.4 Quantity of GW1N-1P5 Pins

Table 2-6 Quantity of GW1N-1P5 Pins

Pin Type		GW1N-1P5					
		LQ100X[1]	LQ100X[2]	LQ100[1]	LQ100[2]	QN48X[1]	QN48X[2]
Single-ended I/O /Differential pair/ LVDS [3]	BANK0	19/8/4	19/8/4	19/8/4	19/8/4	9/4/0	9/4/0
	BANK1	20/10/3	20/10/3	20/10/3	20/10/3	10/5/5	10/5/5
	BANK2	20/10/3	20/10/3	20/10/3	20/10/3	10/5/1	10/5/1
	BANK3	6/3/2	6/3/2	6/3/2	6/3/2	2/1/1	2/1/1
	BANK4	8/4/2	8/4/2	8/4/2	8/4/2	4/2/1	4/2/1
	BANK5	6/3/2	6/3/2	6/3/2	6/3/2	4/2/2	4/2/2
Max. User I/O [4]		80	80	80	80	39	39
Differential Pair		38	38	38	38	19	19
True LVDS output		16	16	16	16	10	10
VCC		0	2	0	2	0	2
VCCO0		2	2	2	2	2	2
VCCO1		2	0	2	0	1	0
VCCO2		2	2	2	2	2	2
VCCO3		1	1	1	1	0	0
VCCO4/VCCO5[5]		1	1	1	1	0	0
VCCO3/VCCO4/VCCO5		0	0	0	0	1	1
VCCO1/VCCX		0	2	0	2	0	1
VCC/VCCX		2	0	2	0	2	0
VSS		8	8	8	8	0	0
MODE0		0	0	0	0	0	0
MODE1		0	0	0	0	0	0
MODE2		0	0	0	0	0	0
JTAGSEL_N		1	1	1	1	1	1
NC		1	1	1	1	0	0

Note!

- [1] UV version
- [2] LV version
- [3] The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [4] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [5] Pin multiplexing.

2.4.5 Quantity of GW1N-4 Pins

Table 2-7 Quantity of GW1N-4 Pins

Pin Type		GW1N-4									
		QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	PG256	PG256M
I/O Single end/ Different-ial pair[1]	BANK0	3/1/0	10/5/0	9/4/0	18/6/0	21/10/0	26/13/0	33/14/0	32/16/0	49/24/0	51/25/0
	BANK1	9/4/1	9/4/2	5/4/2011	6/2/2015	8/1/2016	28/13/5	12/5/2024	26/13/6	42/21/8	42/21/8
	BANK2	4/2/2	12/6/6	11/11/2022	9/7/2023	12/10/2026	26/13/11	38/18/12	43/20/13	72/36/16	70/35/16
	BANK3	7/2/0	8/3/1	6/4/2014	4/2/2012	7/2/2015	25/12/7	11/5/2024	12/6/2027	41/20/8	41/20/8
Max. User I/O [2]		24	40	57	70	79	105	119	131	207	207
Differential Pair		9	18	26	25	37	51	55	62	101	101
True LVDS output		3	9	19	11	13	23	22	25	32	32
VCC		2	2	3	4	4	4	4	4	8	8
VCCO0		1	0	1	1	2	3	2	2	4	4
VCCO1		1	0	1	1	2	3	2	2	3	3
VCCO2		1	0	1	2	2	3	2	2	4	4
VCCO3		1	0	1	1	2	3	2	2	3	3
VCCO0/VCCO3[3]		0	1	0	0	0	0	0	0	0	0
VCCO1/VCCO2[3]		0	1	0	0	0	0	0	0	0	0
VCCX		1	1	1	2	2	0	2	4	2	2
VSS		1	2	6	6	6	10	10	12	24	24
MODE0		0	0	1	1	1	0	1	1	1	1
MODE1		1	1	0	1	0	0	1	1	1	1
MODE2		0	0	0	0	0	0	0	1	1	1
JTAGSEL_N		0	1	1	1	1	1	1	1	1	1

Note!

- [1]The number of single-ended/ Differential I/O pins includes CLK pins and download pins;

- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3]Pin multiplexing.

2.4.6 Quantity of GW1N-9 Pins

Table 2-8 Quantity of GW1N-9 Pins

Pin Type		GW1N-9																	
		QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	PG256	UG256	UG332	QN48F	MG100T
I/O Single end/ Differe-ntial pair[1]	BANK0	4/2/0	12/6/0	14/7/0	0/0/0	9/4/0	22/11/0	18/9/0	18/9/0	20/10/0	28/13/0	17/8/0	17/8/0	30/15/0	36/16/0	46/23/0	46/23/0	9/4/0	12/6/0
	BANK1	13/6/3	12/6/4	14/7/5	25/6/4	24/12/4	16/8/5	32/16/8	32/16/8	34/17/9	38/19/12	36/17/7	36/17/7	26/13/11	56/28/10	58/29/12	68/34/11	9/3/2	22/5/1
	BANK2	12/6/6	18/9/9	14/7/7	23/9/11	26/13/12	32/15/14	40/19/14	40/19/14	43/21/19	30/15/15	54/26/20	54/26/20	35/17/16	70/35/16	52/26/12	90/45/20	12/6/6	32/15/14
	BANK3	11/4/3	13/5/3	13/5/4	22/4/4	20/9//4	17/7/6	30/13/6	30/13/6	34/16/10	33/15/11	40/18/10	40/18/10	22/9/8	49/23/10	51/25/12	69/34/12	9/4/3	21/4/2
Max. User I/O[2]		40	55	55	70	79	87	120	120	131	129	147	147	113	207	207	273	39	87
Differential Pair		18	26	26	30	38	41	57	57	64	62	69	69	54	102	103	136	17	30
True LVDS output		12	16	15	19	20	25	28	28	38	38	37	37	35	36	36	43	11	17
VCC		2	2	5	4	4	3	4	4	4	4	4	4	15	8	8	8	2	3
VCCX		1	2	4	2	2	1	2	2	4	5	4	4	8	2	1	2	1	1
VCCO0		0	0	1	1	2	1	2	2	2	3	3	3	4	4	4	3	1	1
VCCO1		0	0	1	1	2	1	2	2	2	4	3	3	6	3	4	4	0	1
VCCO2		0	0	1	2	2	1	2	2	2	3	3	3	4	4	4	5	0	1
VCCO3		0	0	1	1	2	0	2	2	2	4	3	3	6	3	3	3	1	1
VCCO0/VCCO3[3]		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VCCO1/VCCO2[3]		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
VCCO0/VCCO		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pin Type	GW1N-9																	
	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	PG256	UG256	UG332	QN48F	MG100T
2[3]																		
VCCO1/VCCO3[3]	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VSS	2	2	12	6	6	4	9	9	12	16	8	8	39	24	24	27	2	4
MODE0	0	0	0	1	1	0	1	1	1	0	1	1	0	1	0	1	1	0
MODE1	0	0	0	1	0	1	1	1	1	0	1	1	0	1	0	1	0	1
MODE2	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0	0
MODE1/MODE2[3]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
JTAGSEL_N	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
NC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	0	0

Note!

- [1]The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3]Pin multiplexing.

2.5 Introduction to the I/O BANK

GW1N-1/4/9 includes four I/O Banks.

GW1N-1S includes three I/O Banks.

GW1N-1P5/GW1N-2 includes six I/O Banks. GW1N-2 CS42 includes seven I/O Banks.

This manual provides an overview of the distribution view of the pins in the GW1N series of FPGA products. Please refer to 3 View of Pin Distribution for further details. Different IO Banks in the GW1N series FPGA products are marked with different colors.

User I/O, power, and ground are marked with different symbols and colors. The various symbols and colors used for various pins are defined as follows:

- "  " denotes I/Os in BANK0.
- "  " denotes I/Os in BANK1.
- "  " denotes I/Os in BANK2.
- "  " denotes I/Os in BANK3.
- "  " denotes I/Os in BANK4.
- "  " denotes I/Os in BANK5.
- "  " denotes I/Os in BANK6.
- "  " denotes VCC, VCCX, and VCCO. The filling color does not change.
- "  " denotes VCC. The filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW1N-1S Pins Distribution

3.1.1 View of FN32 Pins Distribution

Figure 3-1 View of GW1N-1S FN32 Pin Distribution (Top View)

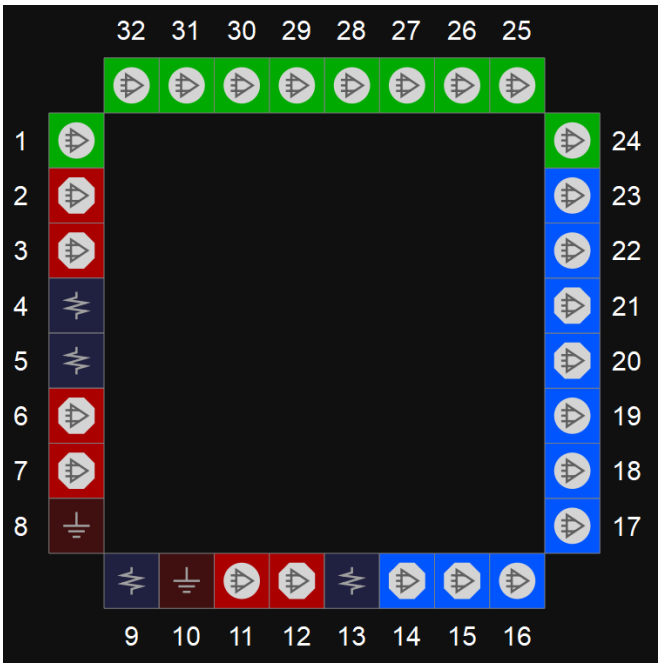


Table 3-1 Other Pins in GW1N-1S FN32

VCC/VCCPLL	9
VCCO0	5
VCCO1	4
VCCO2	13
VSS	8,10

3.1.2 View of CS30 Pins Distribution

Figure 3-2 View of GW1N-1S CS30 Pin Distribution (Top View)

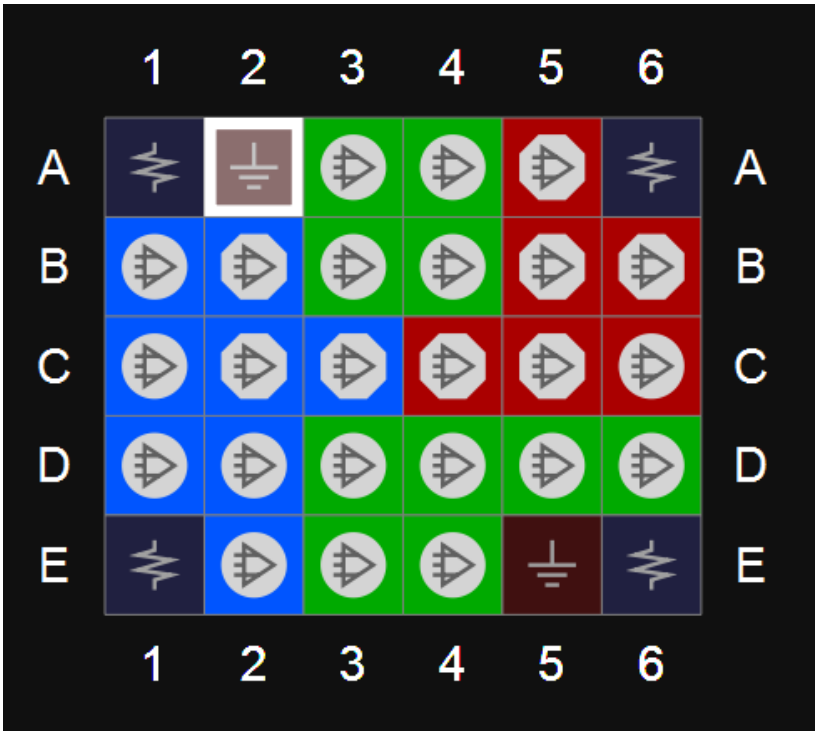


Table 3-2 Other Pins in GW1N-1S CS30

VCC/VCCPLL	E6
VCCO0	A6
VCCO1	A1
VCCO2	E1
VSS	A2,E5

3.2 View of GW1N-1 Pins Distribution

3.2.1 View of CS30 Pins Distribution

Figure 3-3 View of GW1N-1 CS30 Pin Distribution (Top View)

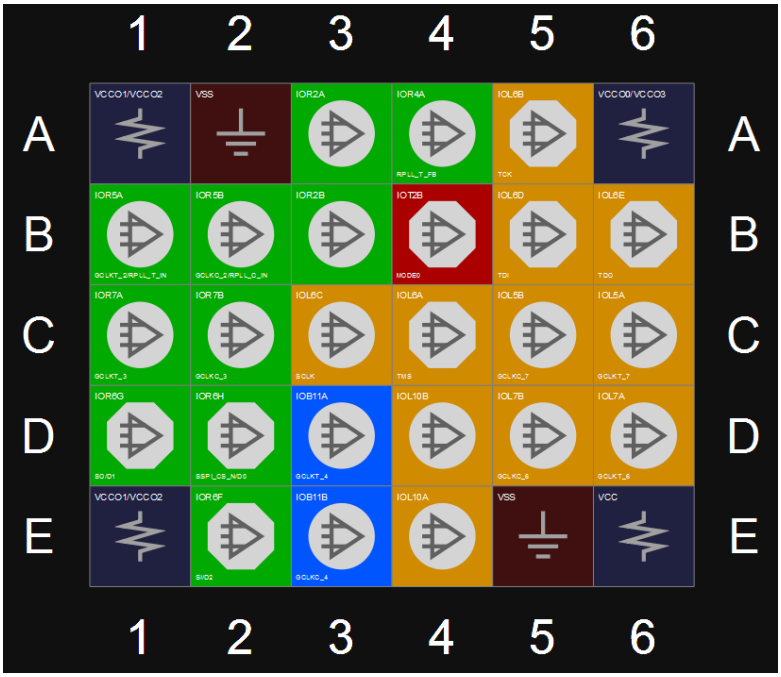


Table 3-3 Other Pins in GW1N-1 CS30

VCC	E6
VCCO0/VCCO3	A6
VCCO1/VCCO2	E1,A1
VSS	A2,E5

3.3 View of GW1N-2 Pins Distribution

3.3.1 View of CS42 Pins Distribution

Figure 3-4 View of GW1N-2 CS42 Pins Distribution (Top View)

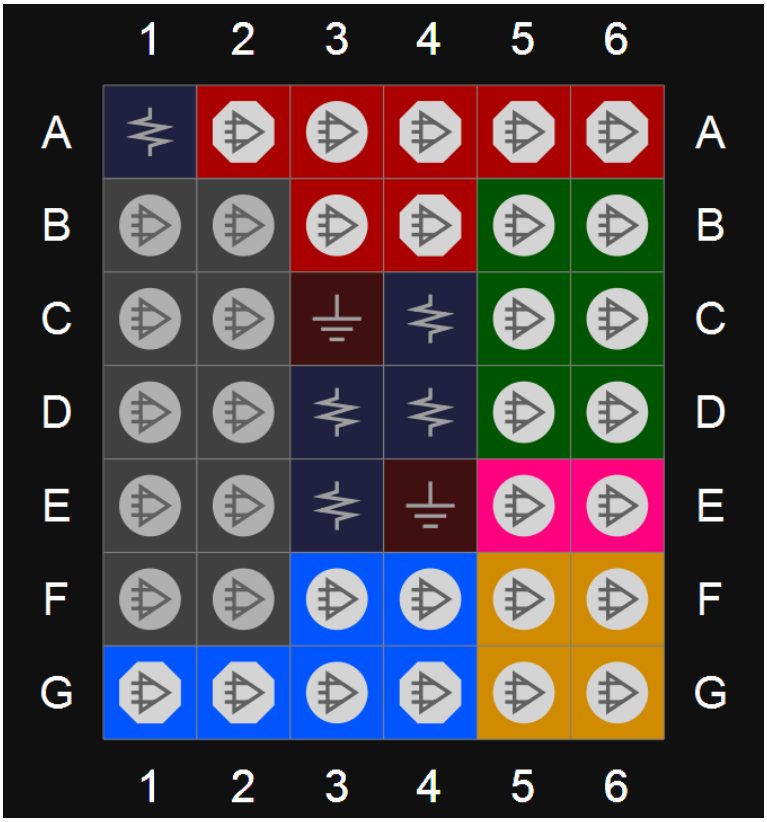


Table 3-4 Other Pins in GW1N-2 CS42

VCC	D4
VCCO0/VCCO2	A1
VCCO3/VCCO4/VCCO5	C4
VCCOD/VCCO1/VCCIOD	D3
VCCX	E3
VSS	C3,E4

3.3.2 View of MG132X Pins Distribution (UV Version)

Figure 3-5 View of GW1N-2 MG132X Pins Distribution (UV Version, Top View)

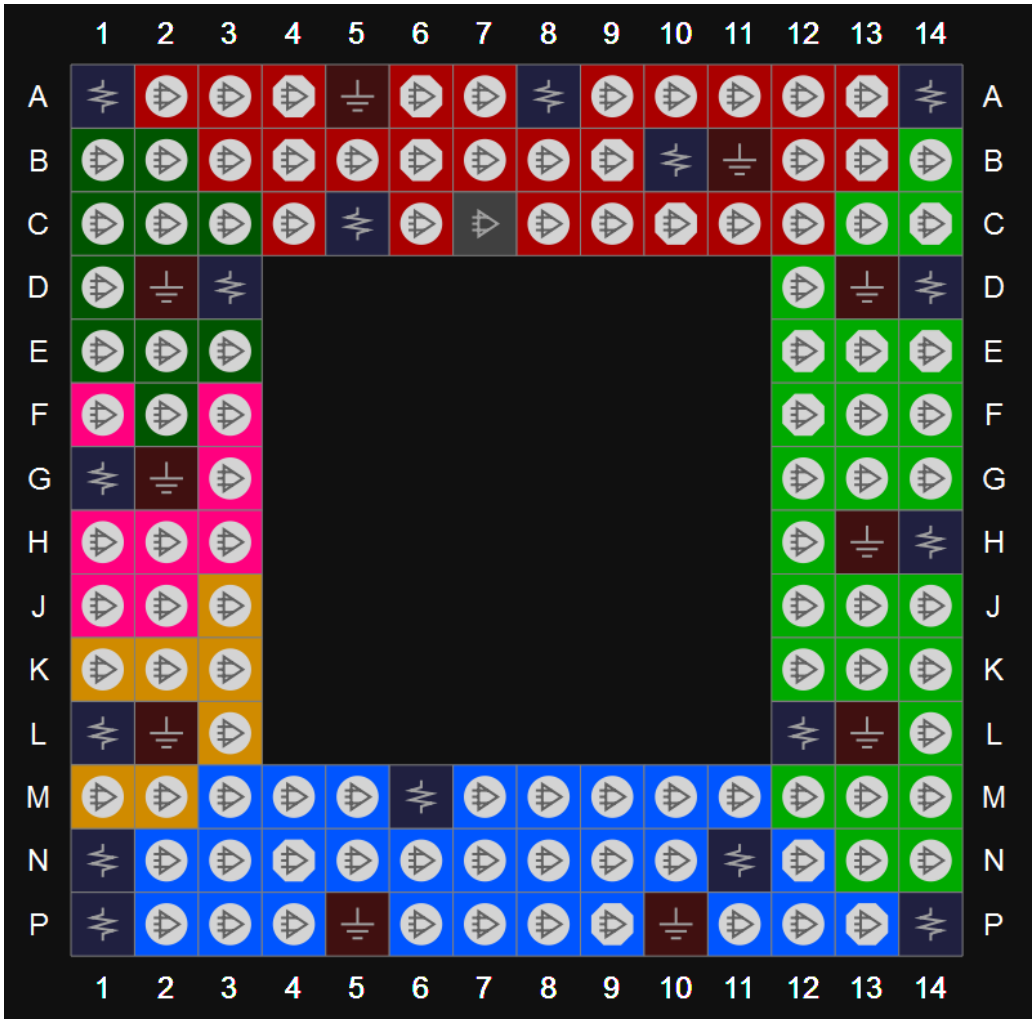


Table 3-5 Other Pins in GW1N-2 MG132X (UV Version)

VCC/VCCX	A1,A14,N1,P14
VCCO0	A8,B10,C5
VCCO1	D14,H14,L12
VCCO2	M6,N11,P1
VCCO3	L1
VCCO4	G1
VCC05	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,,P5,P10
NC	C7

3.3.3 View of MG132X Pins Distribution (LV Version)

Figure 3-6 View of GW1N-2 MG132X Pins Distribution (LV Version, Top View)

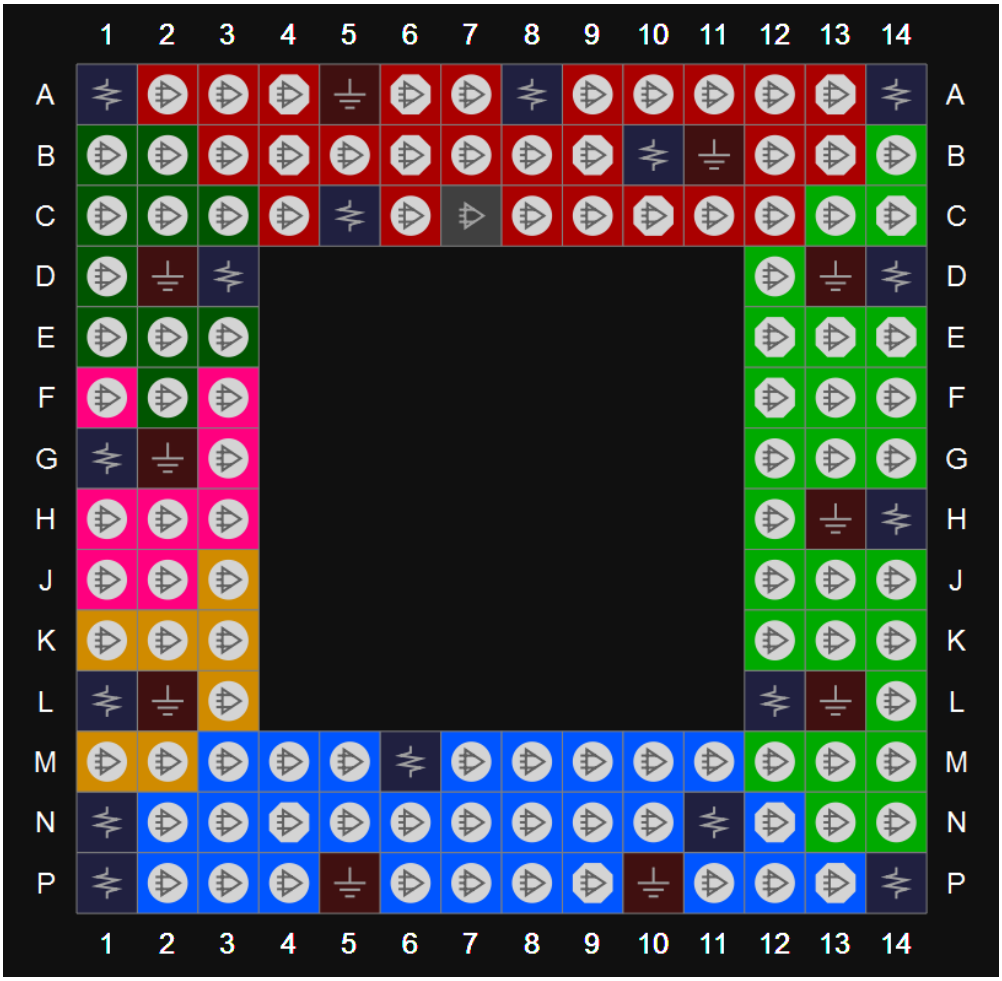


Table 3-6 Other Pins in GW1N-2 MG132X (LV Version)

VCC	A1,A14,N1,P14
VCCO0	A8,B10,C5
VCCO1/VCCX	D14,H14,L12
VCCO2	M6,N11,P1
VCCO3	L1
VCCO4	G1
VCC05	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,,P5,P10
NC	C7

3.3.4 View of LQ100X Pins Distribution (UV Version)

Figure 3-7 View of GW1N-2 LQ100X Pins Distribution (UV Version, Top View)

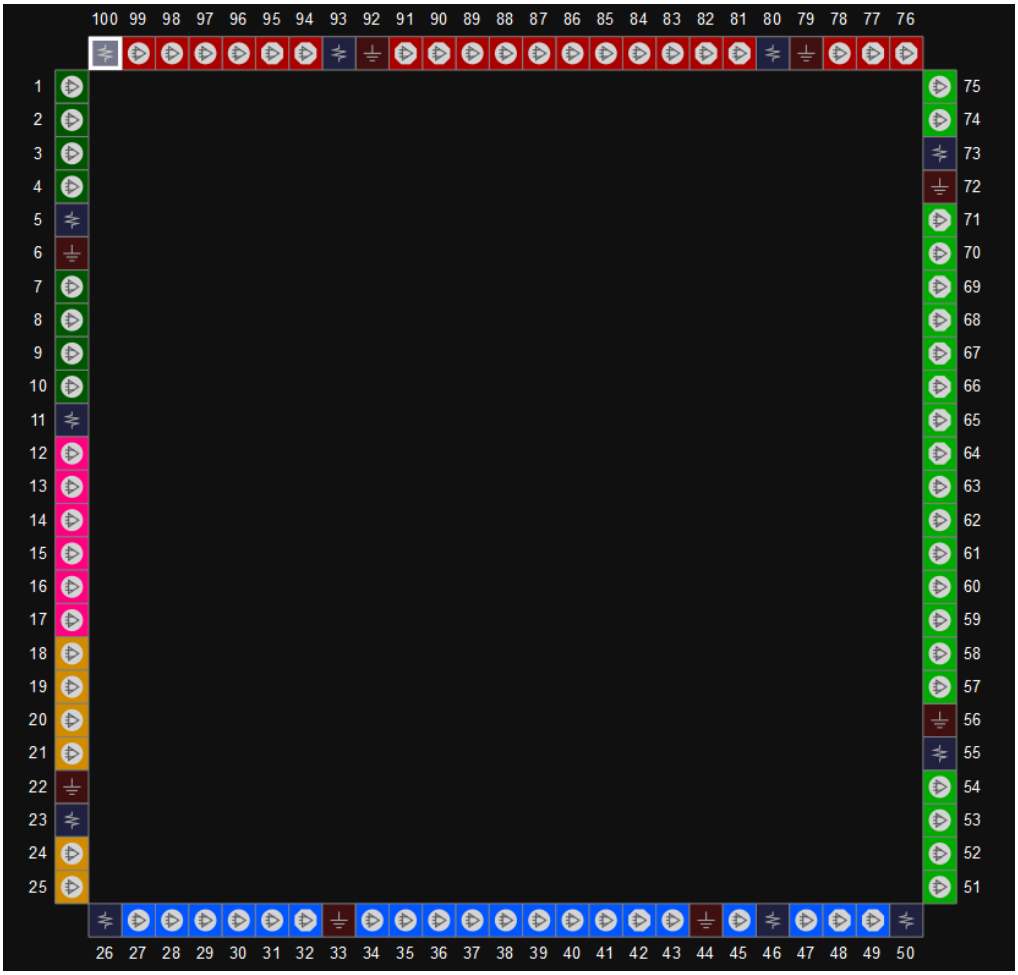


Table 3-7 Other Pins in GW1N-2 LQ100X (UV Version)

VCC/VCCX	100,50
VCCO0	80.93
VCCO1	55,73
VCCO2	26,46
VCCO3	23
VCCO4	11
VCCO5	5
VSS	6,22,33,44,56,72,79,92

3.3.5 View of LQ100X Pins Distribution (LV Version)

Figure 3-8 View of GW1N-2 LQ100X Pins Distribution (LV Version, Top View)

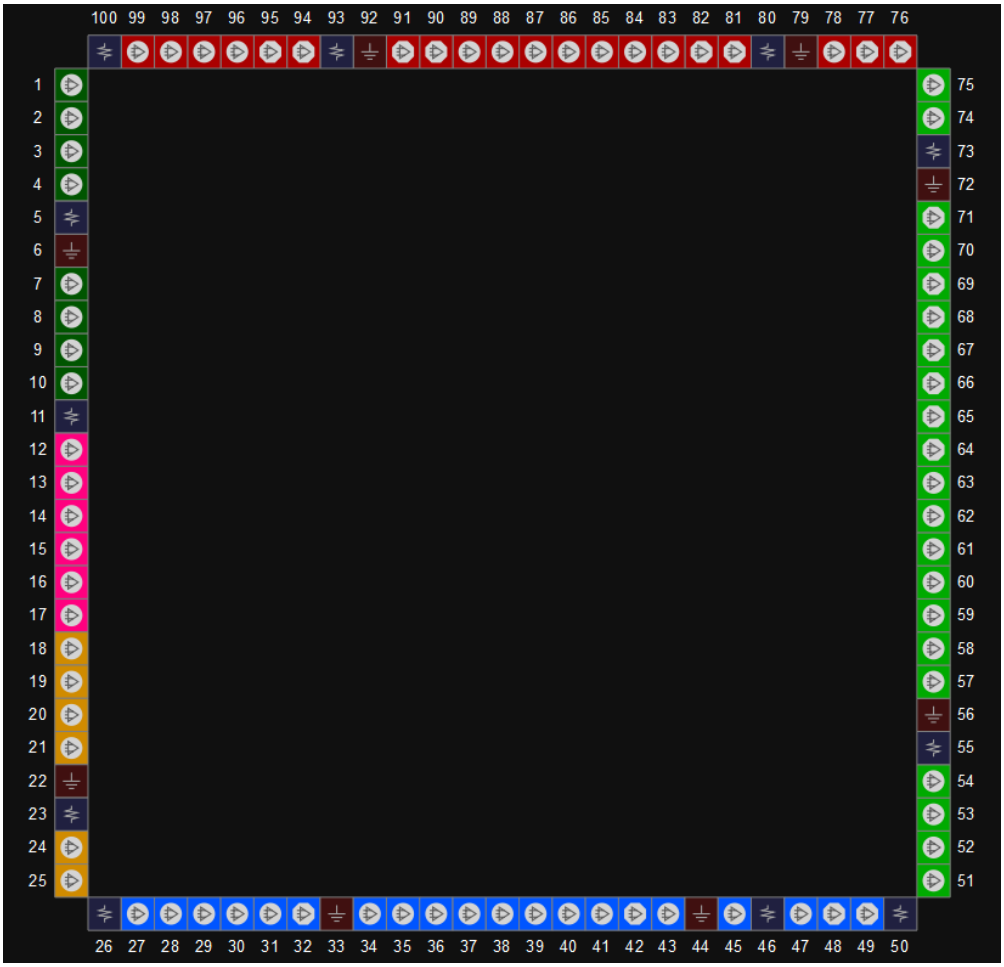


Table 3-8 Other Pins in GW1N-2 LQ100X (LV Version)

VCC	100,50
VCCO0	80.93
VCCO1/VCCX	55,73
VCCO2	26,46
VCCO3	23
VCCO4	11
VCCO5	5
VSS	6,22,33,44,56,72,79,92

3.3.6 View of LQ100 Pins Distribution (UV Version)

Figure 3-9 View of GW1N-2 LQ100 Pins Distribution (UV Version, Top View)

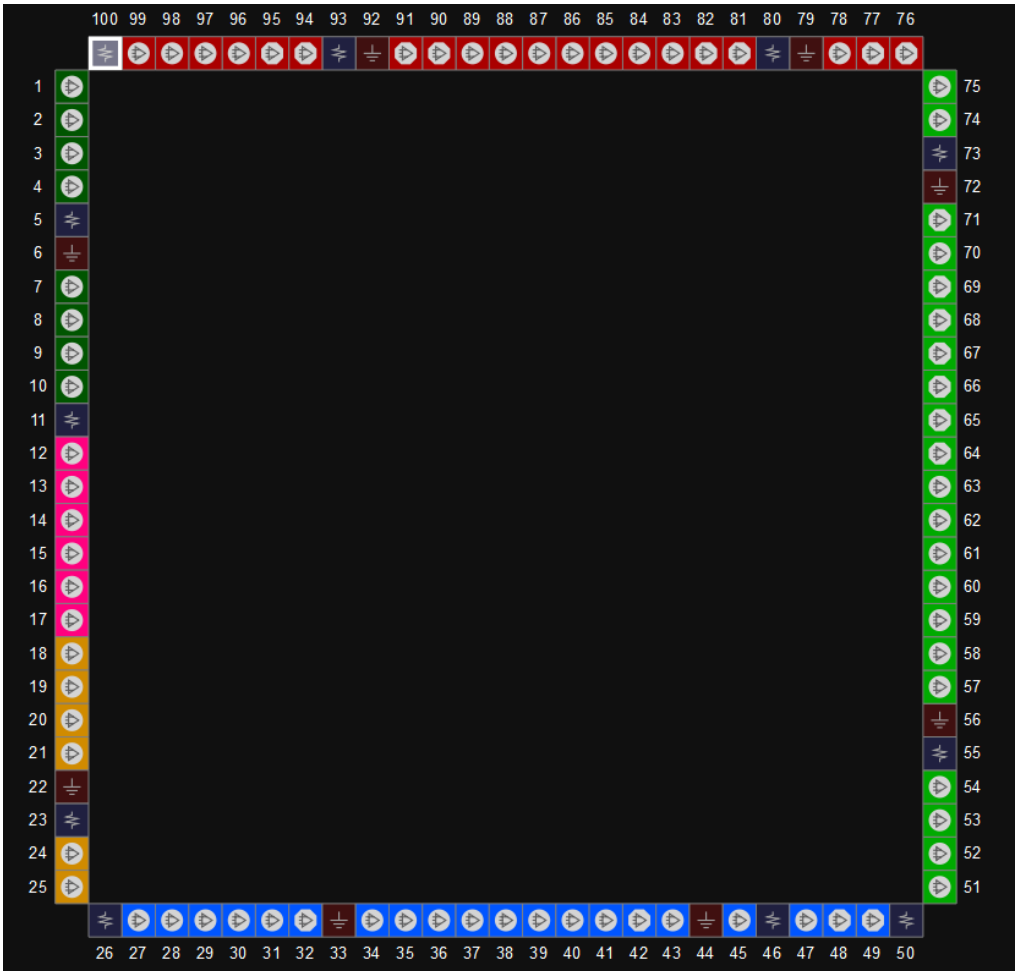


Table 3-9 Other Pins in GW1N-2 LQ100 (UV Version)

VCC/VCCX	100,50
VCCO0	80.93
VCCO1	55,73
VCCO2	26,46
VCCO3	23
VCCO4	11
VCCO5	5
VSS	6,22,33,44,56,72,79,92

3.3.7 View of LQ100 Pins Distribution (LV Version)

Figure 3-10 View of GW1N-2 LQ100 Pins Distribution (LV Version, Top View)

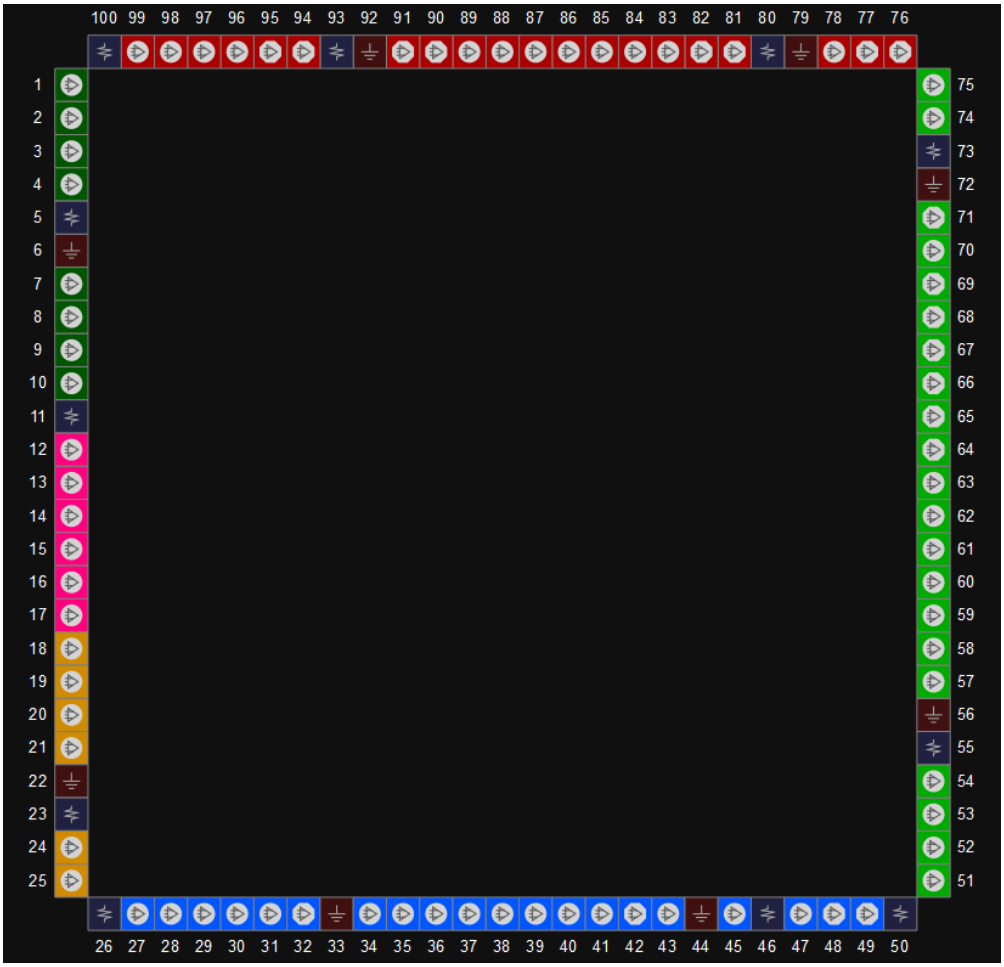


Table 3-10 Other Pins in GW1N-2 LQ100 (LV Version)

VCC	100,50
VCCO0	80.93
VCCO1/VCCX	55,73
VCCO2	26,46
VCCO3	23
VCCO4	11
VCCO5	5
VSS	6,22,33,44,56,72,79,92

3.3.8 View of LQ144X Pins Distribution (UV Version)

Figure 3-11 View of GW1N-2 LQ144X Pins Distribution (UV Version, Top View)

Table 3-11 Other Pins in GW1N-2 LQ144X (UV Version)

VCC/VCCX	144,36,72,108
VCCO0	118,123,135
VCCO1	79,88,102
VCCO2	37,51,66
VCCO3	30
VCCO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.3.9 View of LQ144X Pins Distribution (LV Version)

Figure 3-12 View of GW1N-2 LQ144X Pins Distribution (LV Version, Top View)

Table 3-12 Other Pins in GW1N-2 LQ144X (LV Version)

VCC	144,36,72,108
VCCO0	118,123,135
VCCO1/VCCX	79,88,102
VCCO2	37,51,66
VCCO3	30
VCCO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.3.10 View of LQ144 Pins Distribution (UV Version)

Figure 3-13 View of GW1N-2 LQ144 Pins Distribution (UV Version, Top View)

Table 3-13 Other Pins in GW1N-2 LQ144 (UV Version)

VCC/VCCX	144,36,72,108
VCCO0	118,123,135
VCCO1	79,88,102
VCCO2	37,51,66
VCCO3	30
VCCO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.3.11 View of LQ144 Pins Distribution (LV Version)

Figure 3-14 View of GW1N-2 LQ144 Pins Distribution (LV Version, Top View)

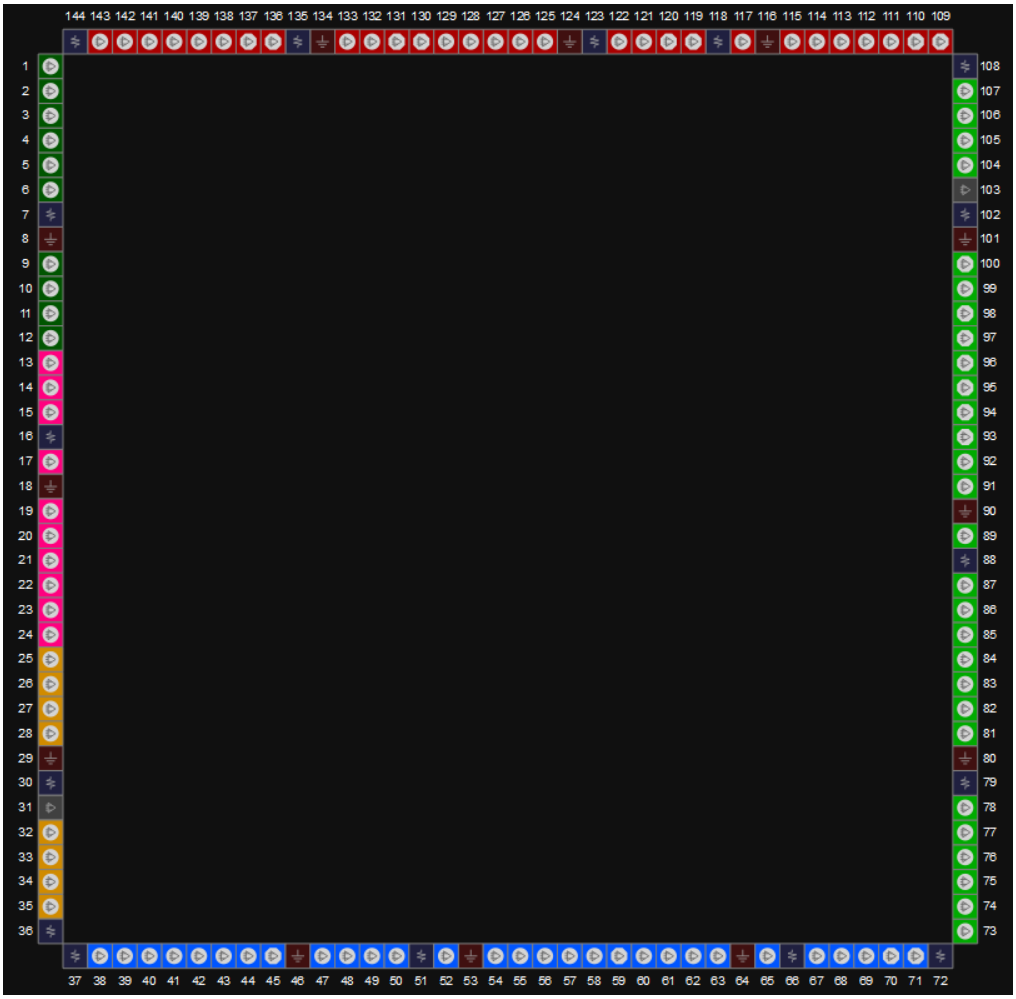


Table 3-14 Other Pins in GW1N-2 LQ144 (LV Version)

VCC	144,36,72,108
VCCO0	118,123,135
VCCO1/VCCX	79,88,102
VCCO2	37,51,66
VCCO3	30
VCCO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.3.12 View of QN48 Pins Distribution

Figure 3-15 View of GW1N-2 QN48 Pins Distribution (Top View)

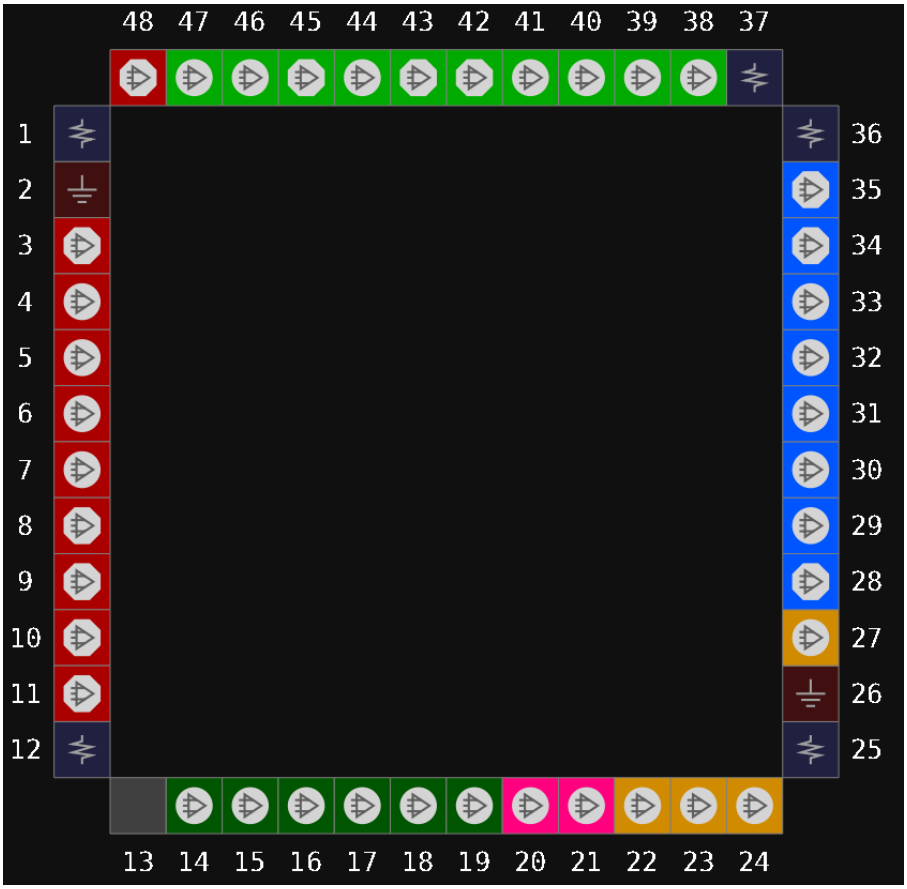


Table 3-15 Other Pins in GW1N-2 QN48

VCC	12
VCCO0	1
VCCO1	37
VCCO2/VCCX	36
VCCO3/VCCO4/VCCO5	25
VSS	2,26

3.3.13 View of QN48H Pins Distribution

Figure 3-16 View of GW1N-2 QN48H Pins Distribution (Top View)

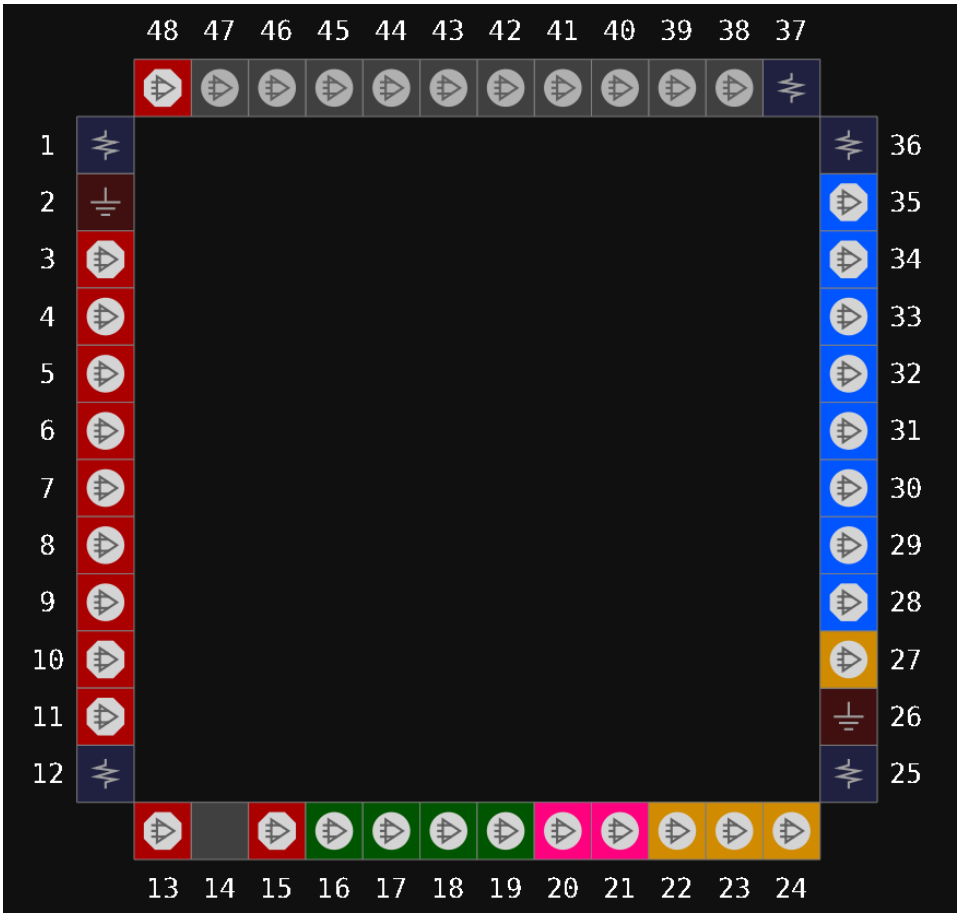


Table 3-16 Other Pins in GW1N-2 QN48H

VCC/VCCO1	37
VCCO0	12
VCCO2/VCCX	36
VCCO3/VCCO4/VCCO5	25
VCCD/VCCOD	1
VSS	2,26

3.3.14 View of MG132H Pins Distribution

Figure 3-17 View of GW1N-2 MG132H Pins Distribution (Top View)

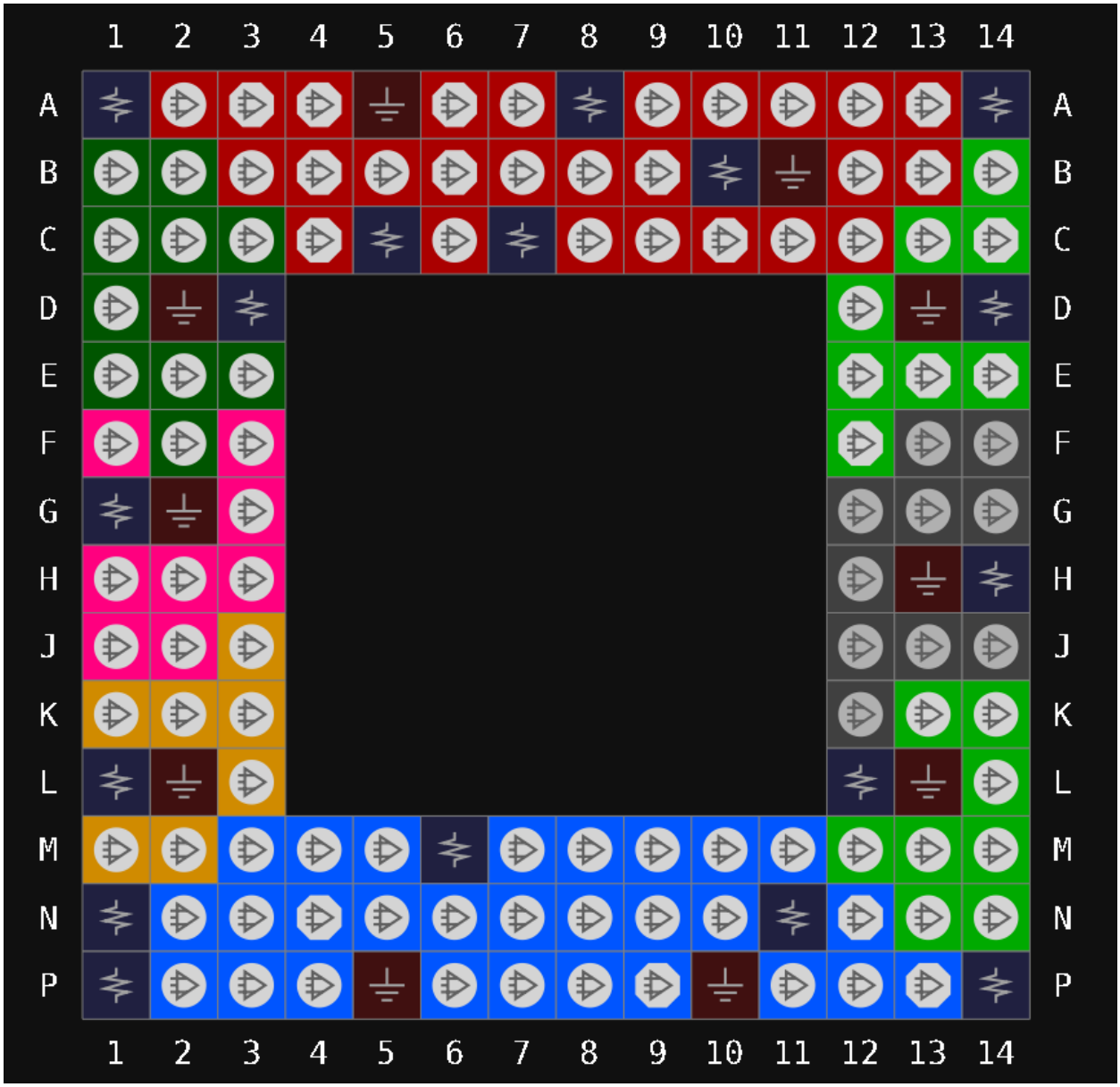


Table 3-17 Other Pins in GW1N-2 MG132H

VCC	A1,A14,N1,P14
VCCO0	A8,B10,C5
VCCO1	D14,L12
VCCO2	M6,N11,P1
VCCO3	L1
VCCO4	G1
VCCO5	D3
VCCX	H14
VCCD/VCCOD	C7
VSS	A5,B11,D2,D13,G2,H13,L2,L13,P5,P10

3.3.15 View of MG132 Pins Distribution (UV Version)

Figure 3-18 View of GW1N-2 MG132 Pins Distribution (UV Version, Top View)

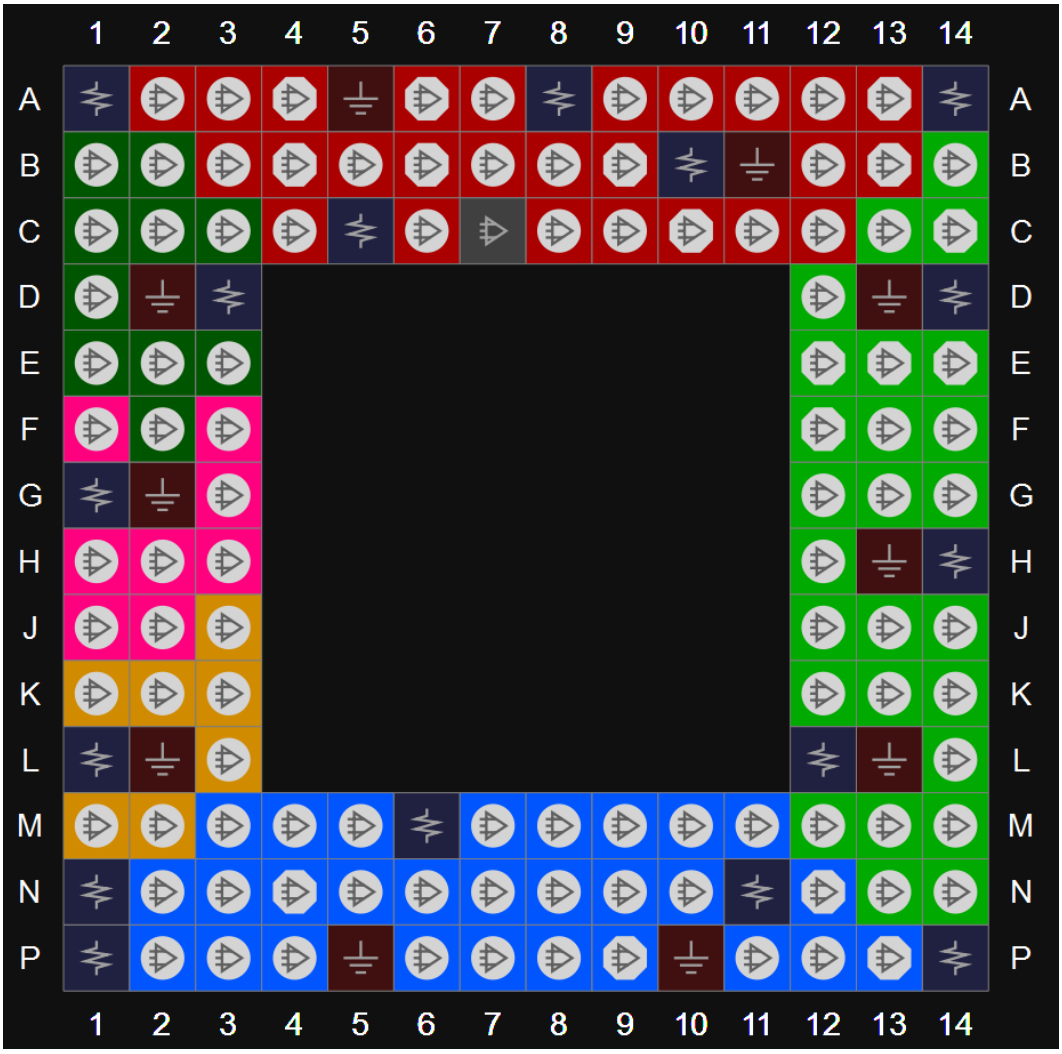


Table 3-18 Other Pins in GW1N-2 MG132 (UV Version)

VCC/VCCX	A1,A14,N1,P14
VCCO0	A8,B10,C5
VCCO1	D14,H14,L12
VCCO2	M6,N11,P1
VCCO3	L1
VCCO4	G1
VCCO5	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,P5,P10
NC	C7

3.3.16 View of MG132 Pins Distribution (LV Version)

Figure 3-19 View of GW1N-2 MG132 Pins Distribution (LV Version, Top View)

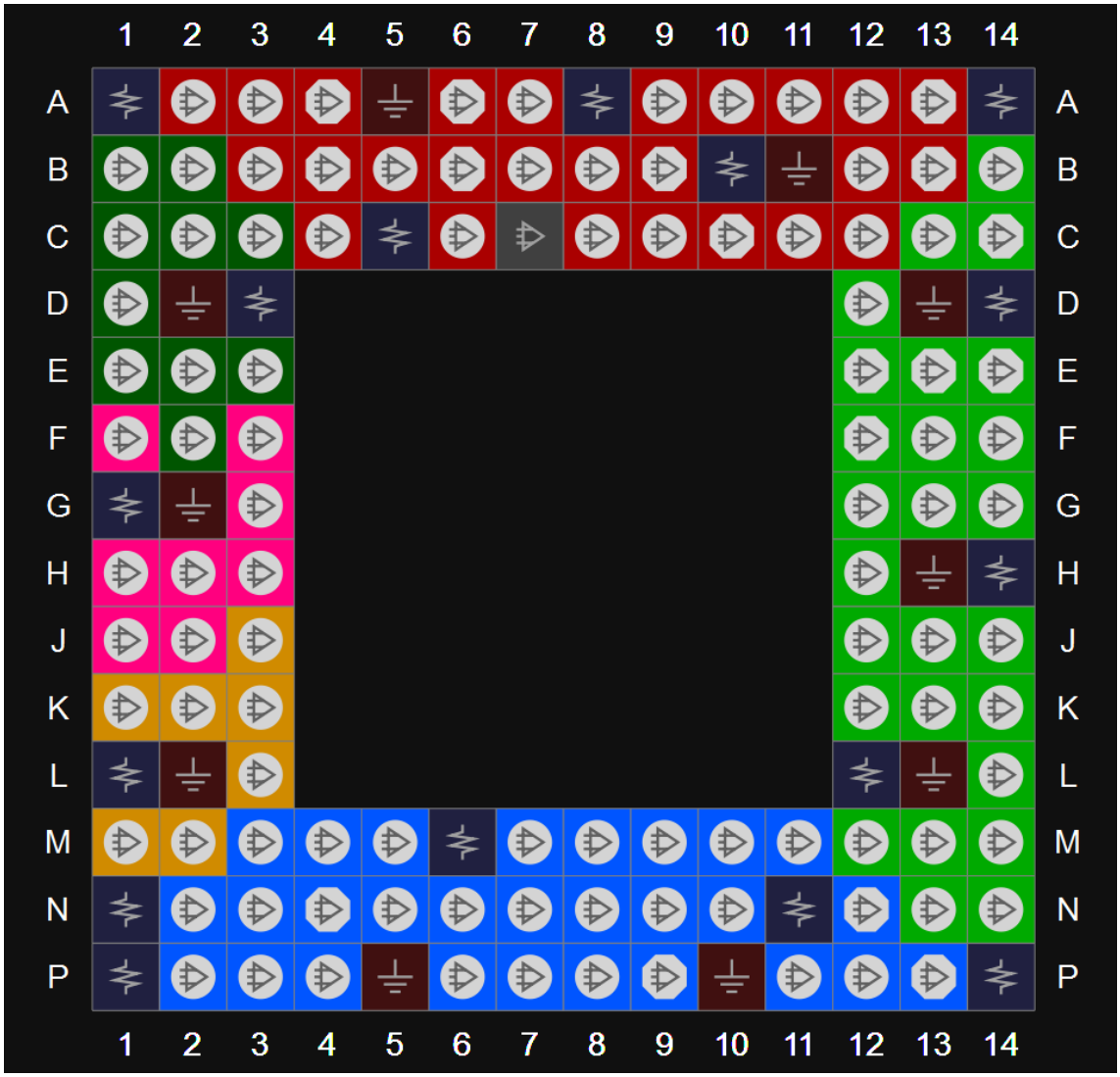


Table 3-19 Other Pins in GW1N-2 MG132 (LV Version)

VCC	A1,A14,N1,P14
VCCO0	A8,B10,C5
VCCO1/VCCX	D14,H14,L12
VCCO2	M6,N11,P1
VCCO3	L1
VCCO4	G1
VCCO5	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,P5,P10
NC	C7

3.3.17 View of MG121 Pins Distribution (LV Version)

Figure 3-20 View of GW1N-2 MG121 Pins Distribution (LV Version, Top View)

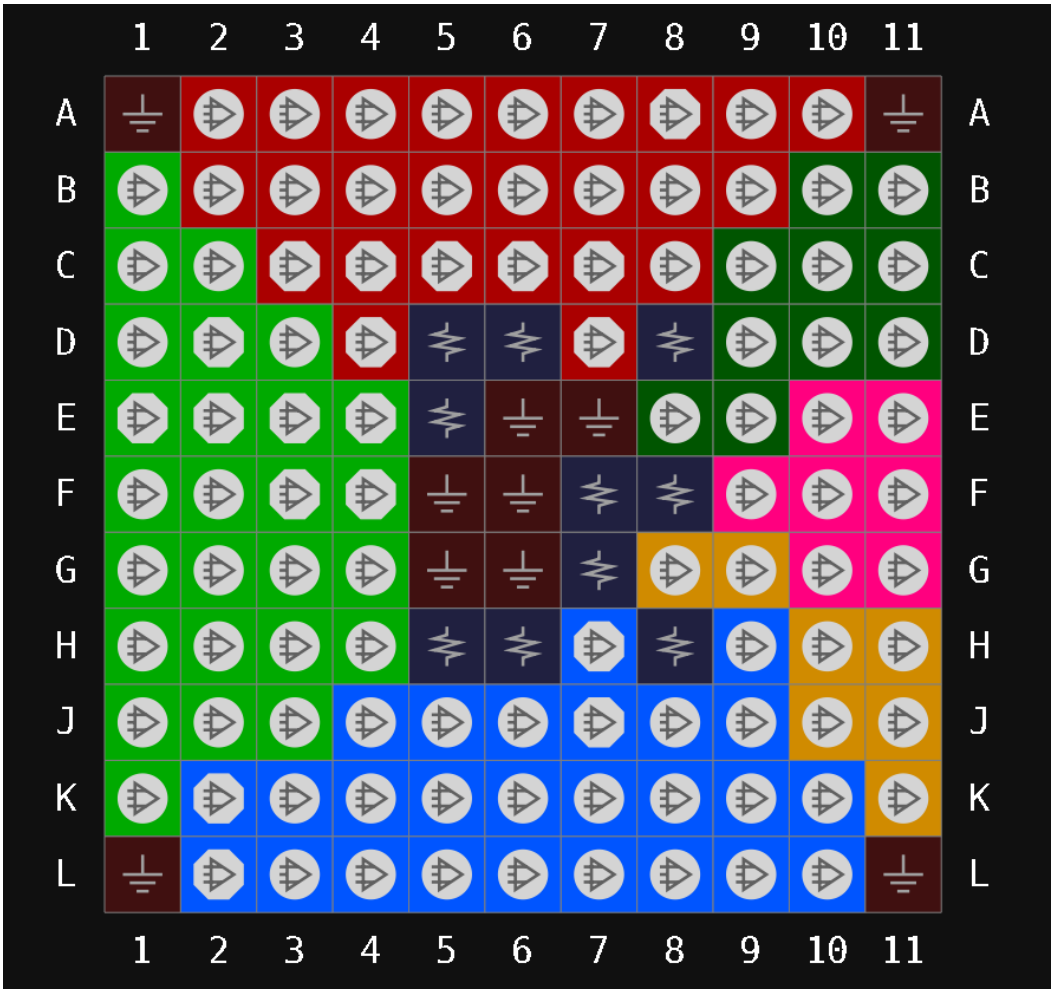


Table 3-20 Other Pins in GW1N-2 MG121 (LV Version)

VCC	F7,G7,D5,E5
VCCO0	D6
VCCO1/VCCX	H5
VCCO2	H6
VCCO3	H8
VCCO4	F8
VCCO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.3.18 View of MG121 Pins Distribution (UV Version)

Figure 3-21 View of GW1N-2 MG121 Pins Distribution (UV Version, Top View)

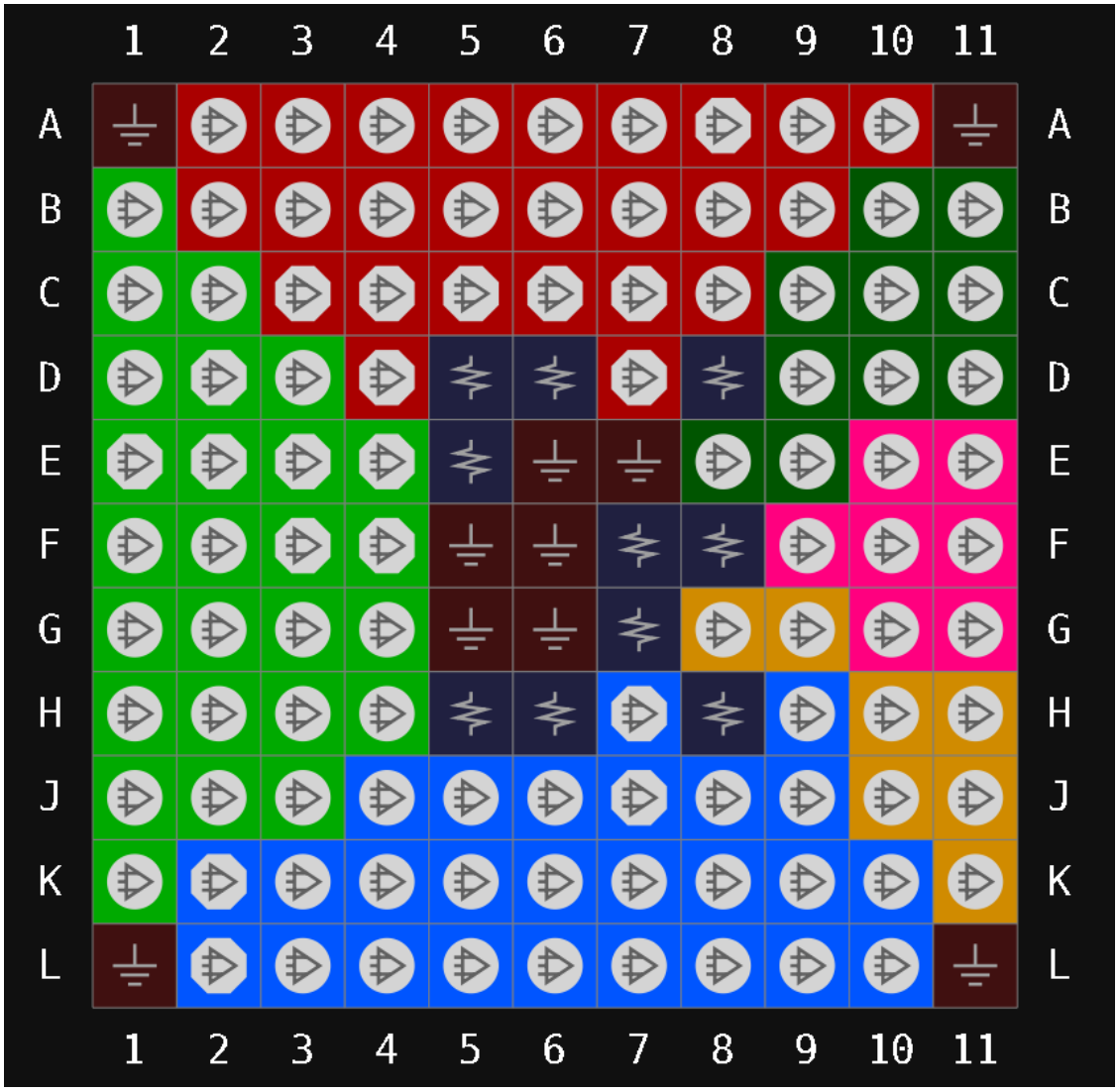


Table 3-21 Other Pins in GW1N-2 MG121 (UV Version)

VCC/VCCX	F7,G7,D5,E5
VCCO0	D6
VCCO1	H5
VCCO2	H6
VCCO3	H8
VCCO4	F8
VCCO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.3.19 View of MG121X Pins Distribution (LV Version)

Figure 3-22 View of GW1N-2 MG121X Pins Distribution (LV Version, Top View)

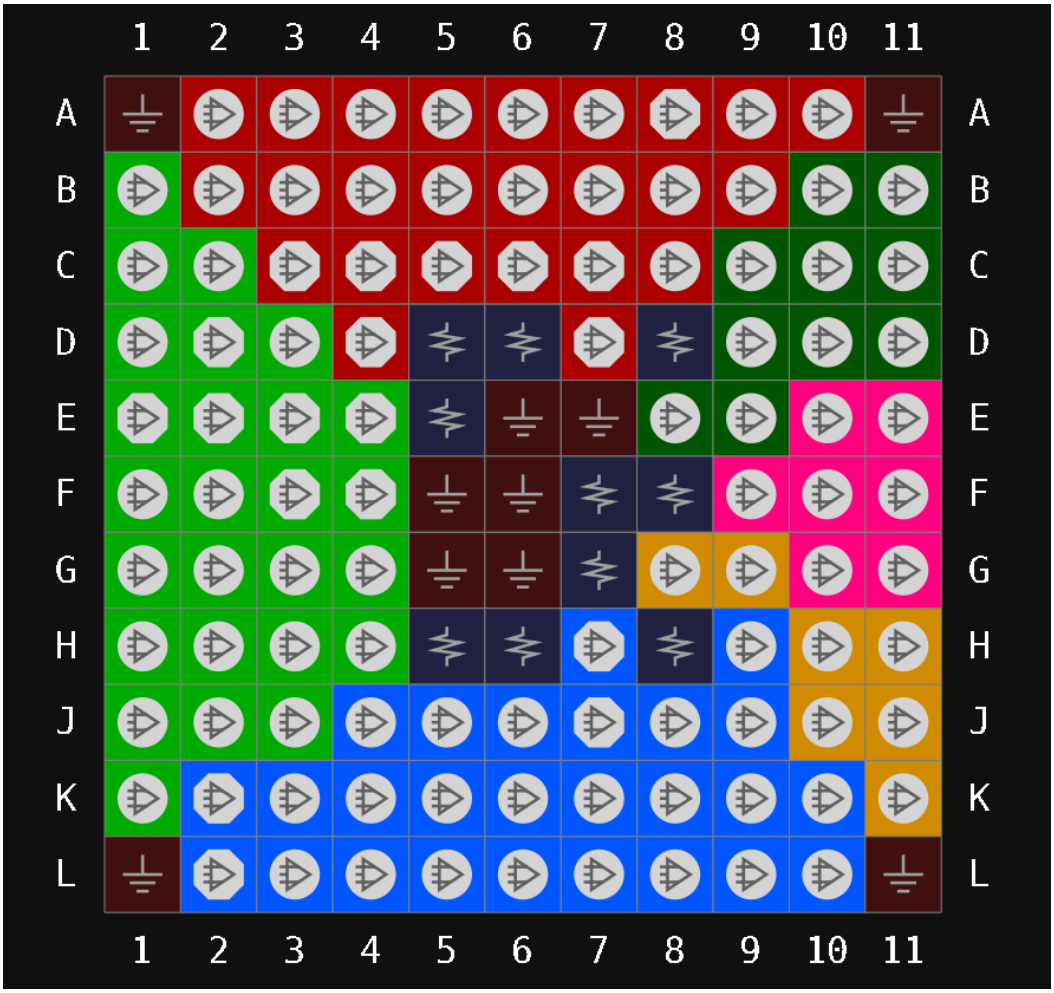


Table 3-22 Other Pins in GW1N-2 MG121X (LV Version)

VCC	F7,G7,D5,E5
VCCO0	D6
VCCO1/VCCX	H5
VCCO2	H6
VCCO3	H8
VCCO4	F8
VCCO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.3.20 View of MG121X Pins Distribution (UV Version)

Figure 3-23 View of GW1N-2 MG121X Pins Distribution (UV Version, Top View)

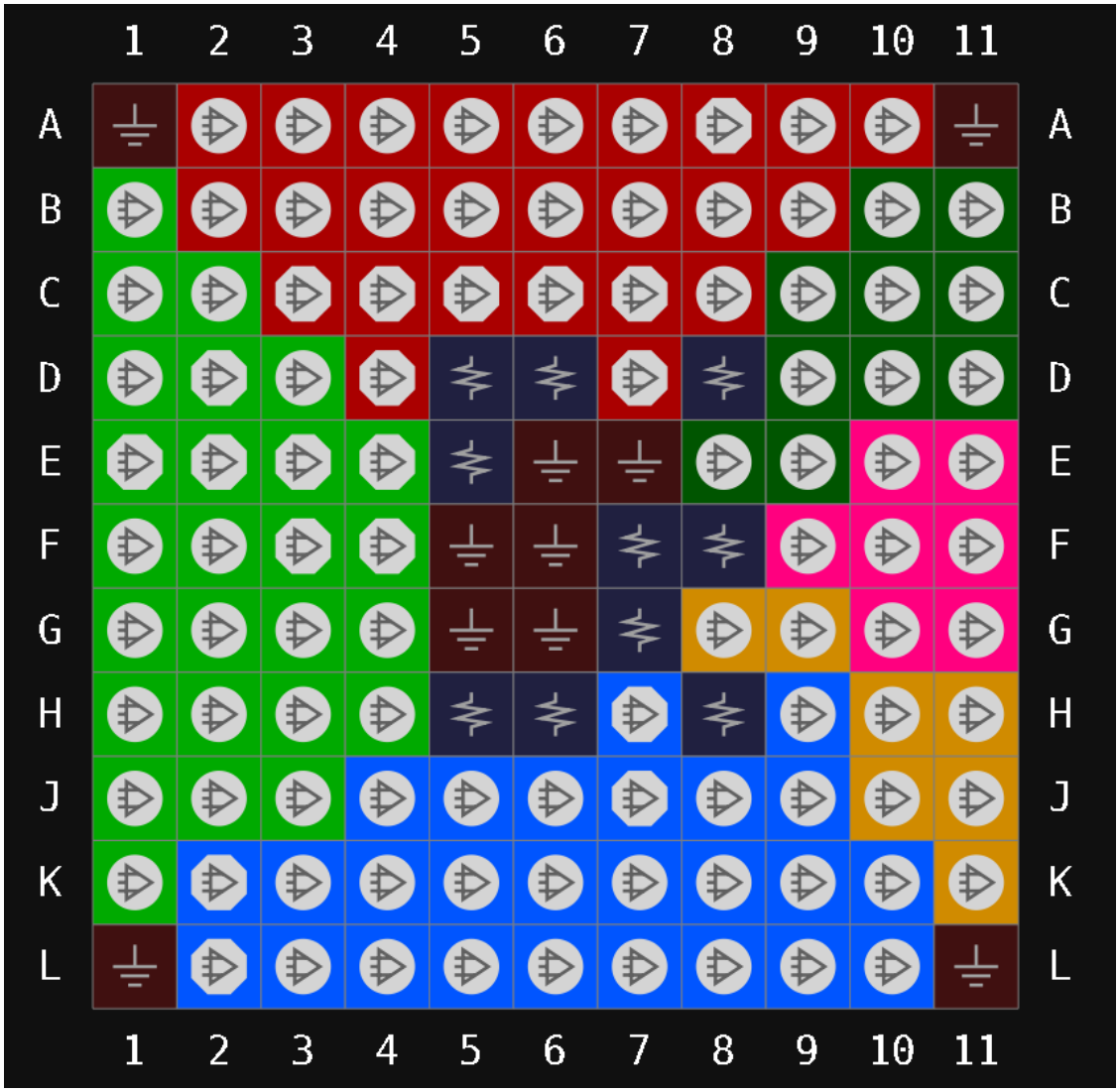


Table 3-23 Other Pins in GW1N-2 MG121X (UV Version)

VCC/VCCX	F7,G7,D5,E5
VCCO0	D6
VCCO1	H5
VCCO2	H6
VCCO3	H8
VCCO4	F8
VCCO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.3.21 View of MG49 Pins Distribution

Figure 3-24 View of GW1N-2 MG49 Pins Distribution (Top View)

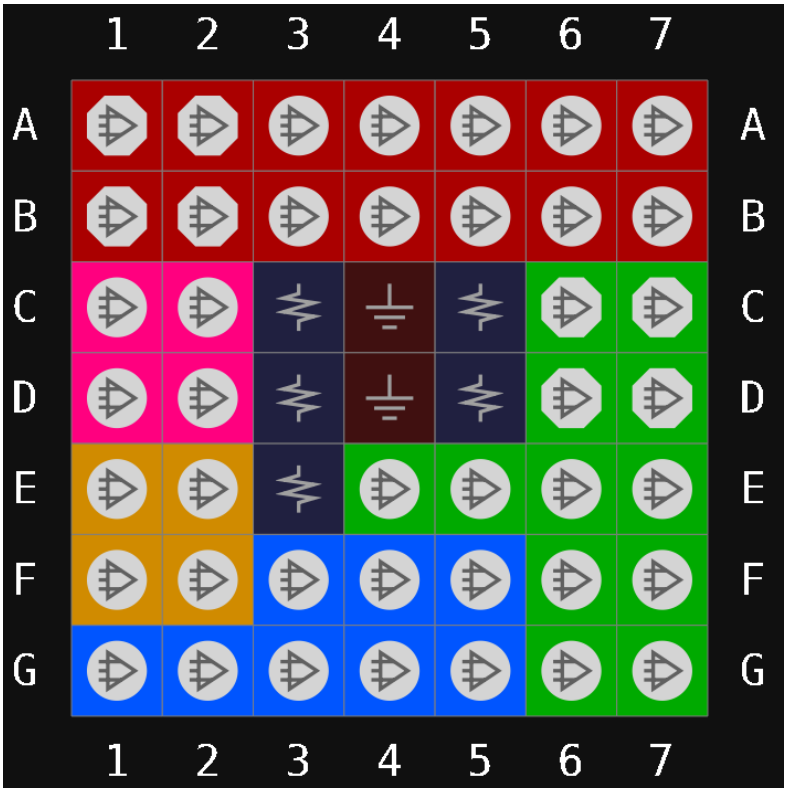


Table 3-24 Other Pins in GW1N-2 MG49

VCC	C3
VCCO0	C5
VCCO1	D5
VCCO2/VCCO3/VCCO4/ VCCO5	D3
VCCX	E3
VSS	C4，D4

3.3.22 View of QN32X LV Pins Distribution

Figure 3-25 View of GW1N-2 QN32X LV Pins Distribution (Top View)

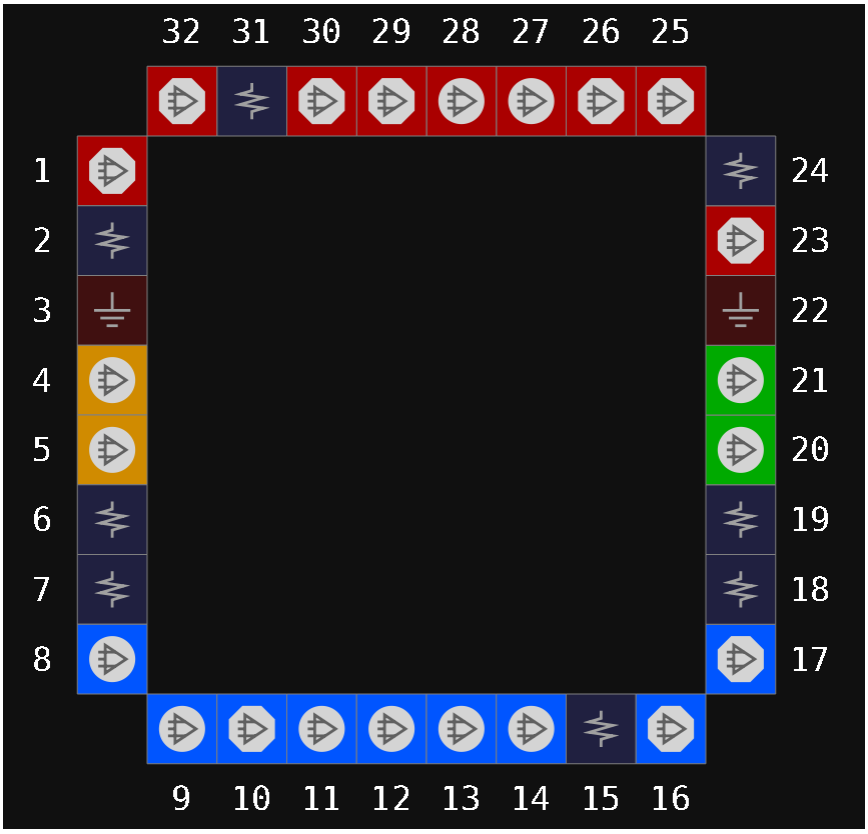


Table 3-25 Other Pins in GW1N-2 QN32X LV

VCC	2,18
VCCO2	7,15
VCCO3	6
VCCO1/VCCO4/ VCCO5	19
VCCO0/VCCX	24,31
VSS	3,22

3.3.23 View of QN32X UV Pins Distribution

Figure 3-26 View of GW1N-2 QN32X UV Pins Distribution (Top View)

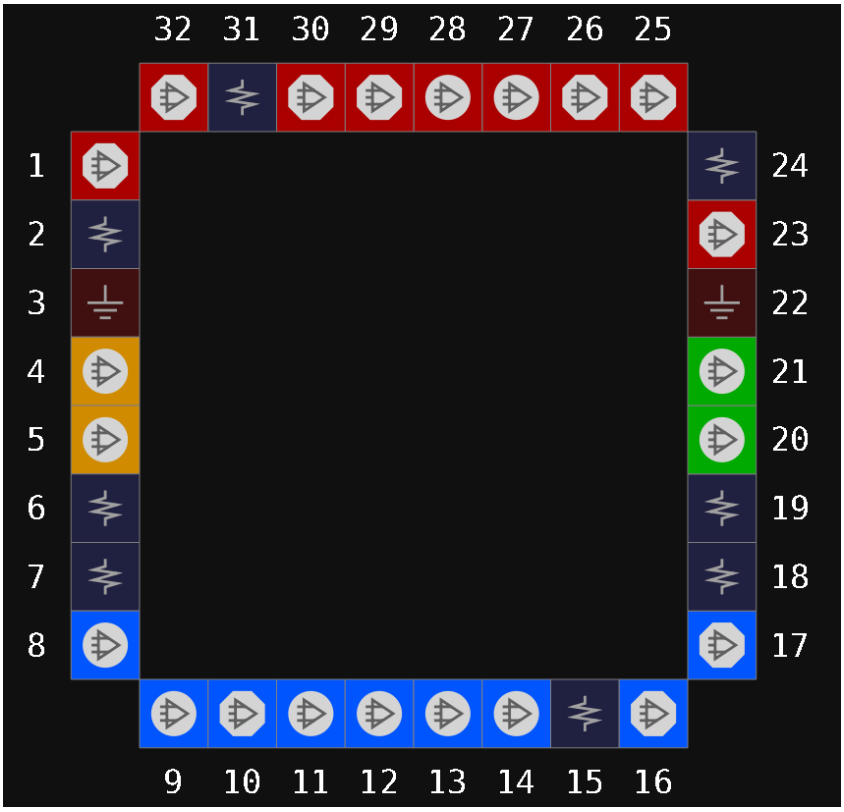


Table 3-26 Other Pins in GW1N-2 QN32X UV

VCCO0	24,31
VCCO2	7,15
VCCO3	6
VCCO1/VCCO4/ VCCO5	19
VCC/VCCX	2,18
VSS	3,22

3.3.24 View of QN88 Pins Distribution

Figure 3-27 View of GW1N-2 QN88 Pins Distribution (Top View)

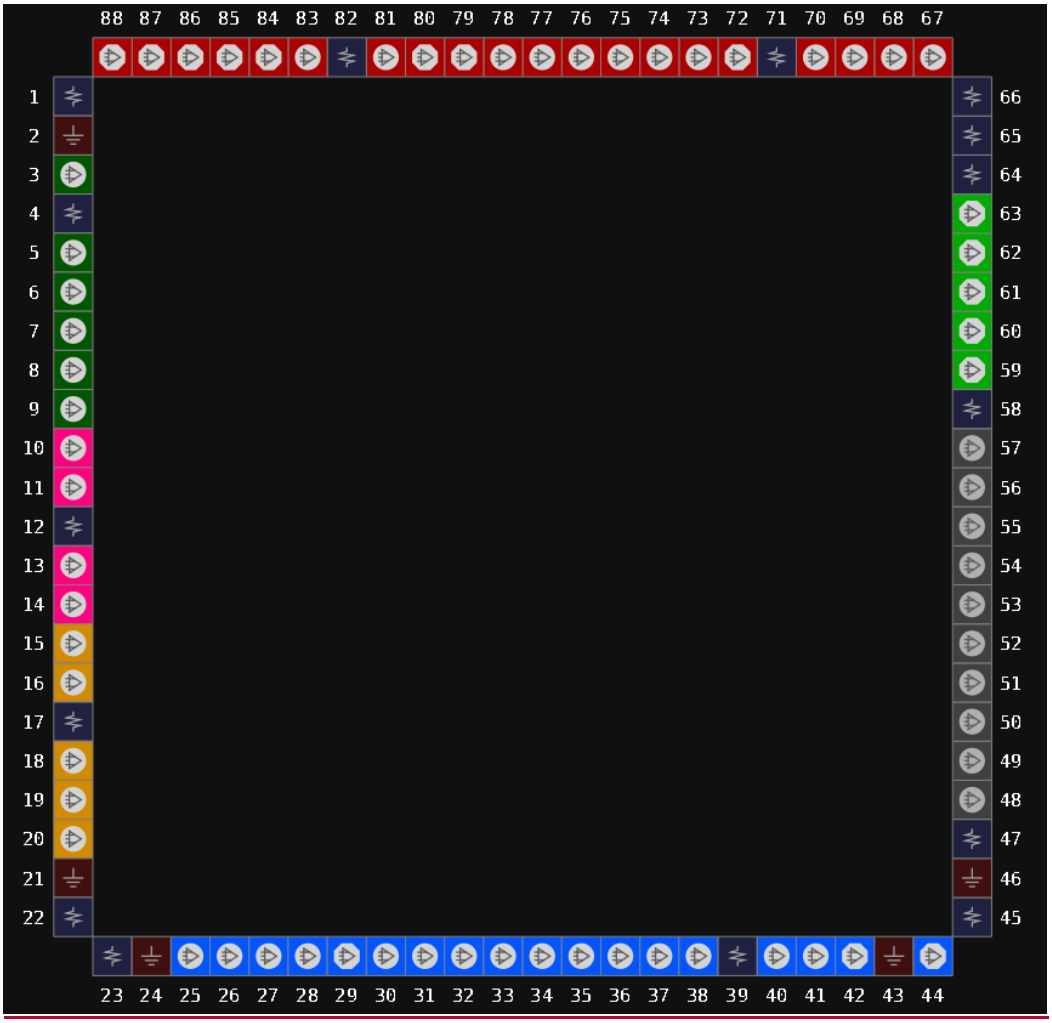


Table 3-27 Other Pins in GW1N-2 QN88

VCC	1,22,45,66
VCCO0	71,82
VCCO1	65
VCCO2	23,39
VCCO3	17
VCCO4	12
VCCO5	4
VCCX	47,64
VCCD/VCCOD	58
VSS	2,21,24,43,46

3.3.25 View of CS42H Pins Distribution

Figure 3-28 View of GW1N-2 CS42H Pins Distribution (Top View)

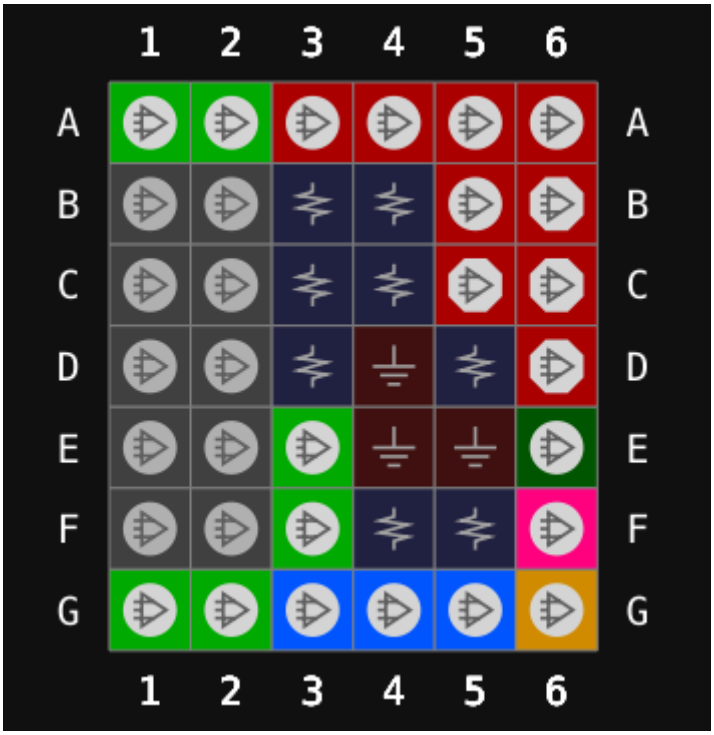


Table 3-28 Other Pins in GW1N-2 CS42H

VCC	D3
VCCO0	B4
VCCO1	B3
VCCO2	F5
VCCO3/ VCCO4/ VCCO5	C4
VCCX	D5,F4
VCCD/VCCOD	C3
VSS	D4,E4,E5

3.4 View of GW1N-1P5 Pins Distribution

3.4.1 View of LQ100X Pins Distribution (LV Version)

Figure 3-29 View of GW1N-1P5 LQ100X Pins Distribution (LV Version, Top View)

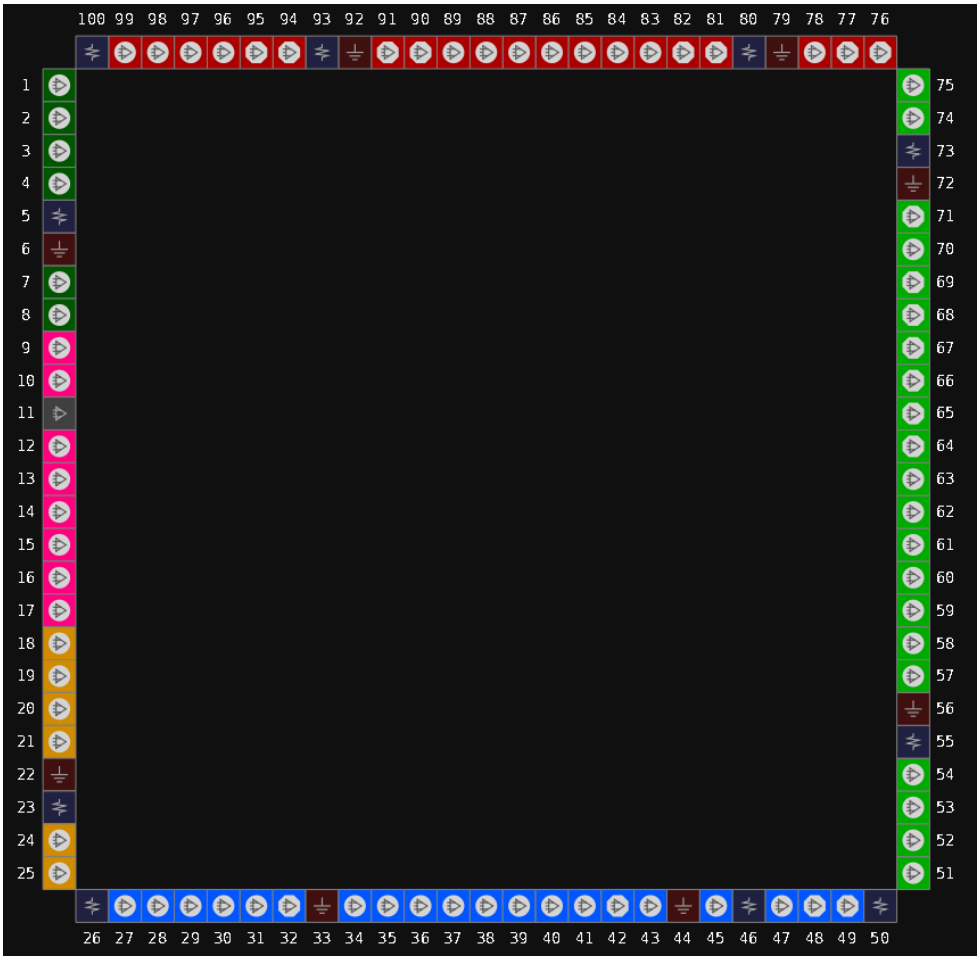


Table 3-29 Other Pins in GW1N-1P5 LQ100X (LV Version)

VCC	100,50
VCCO0	80,93
VCCO2	26,46
VCCO3	23
VCCO4/VCCO5	5
VCCO1/VCCX	55,73
VSS	6,22,33,44,56,72,79,92
NC	11

3.4.2 View of LQ100X Pins Distribution (UV Version)

Figure 3-30 View of GW1N-1P5 LQ100X Pins Distribution (UV Version, Top View)

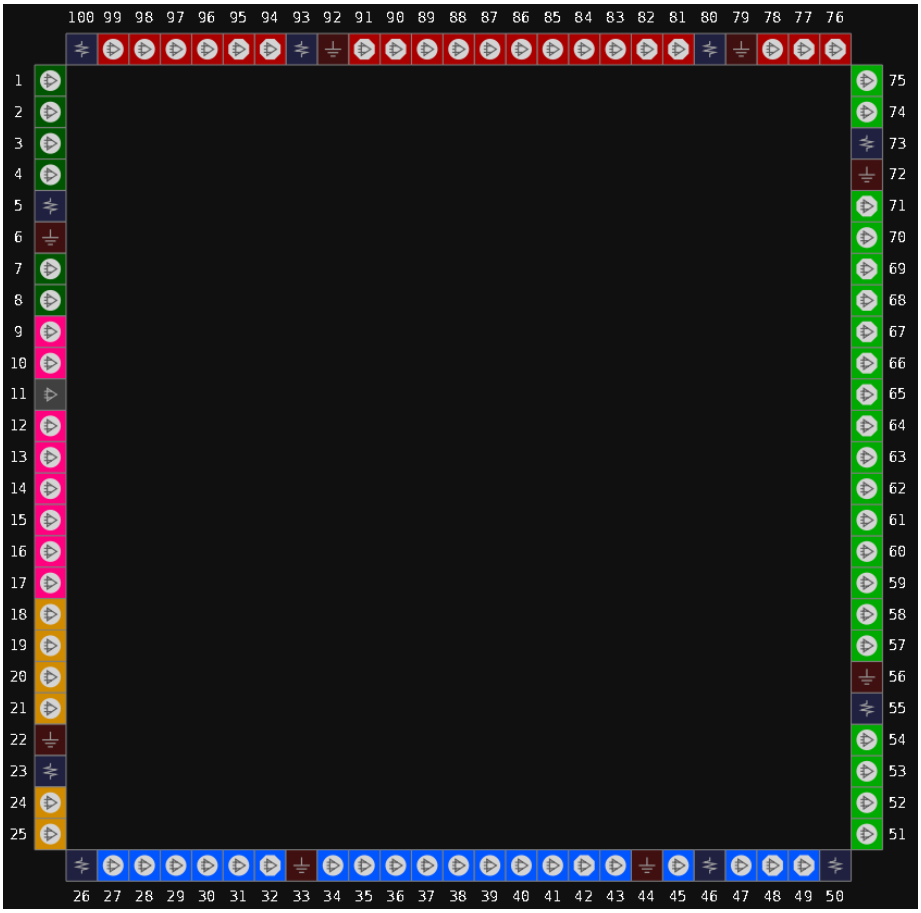


Table 3-30 Other Pins in GW1N-1P5 LQ100X (UV Version)

VCCO0	80,93
VCCO1	55,73
VCCO2	26,46
VCCO3	23
VCCO4/VCCO5	5
VCC/VCCX	100,50
VSS	6,22,33,44,56,72,79,92
NC	11

3.4.3 View of LQ100 Pins Distribution (LV Version)

Figure 3-31 View of GW1N-1P5 LQ100 Pins Distribution (LV Version, Top View)

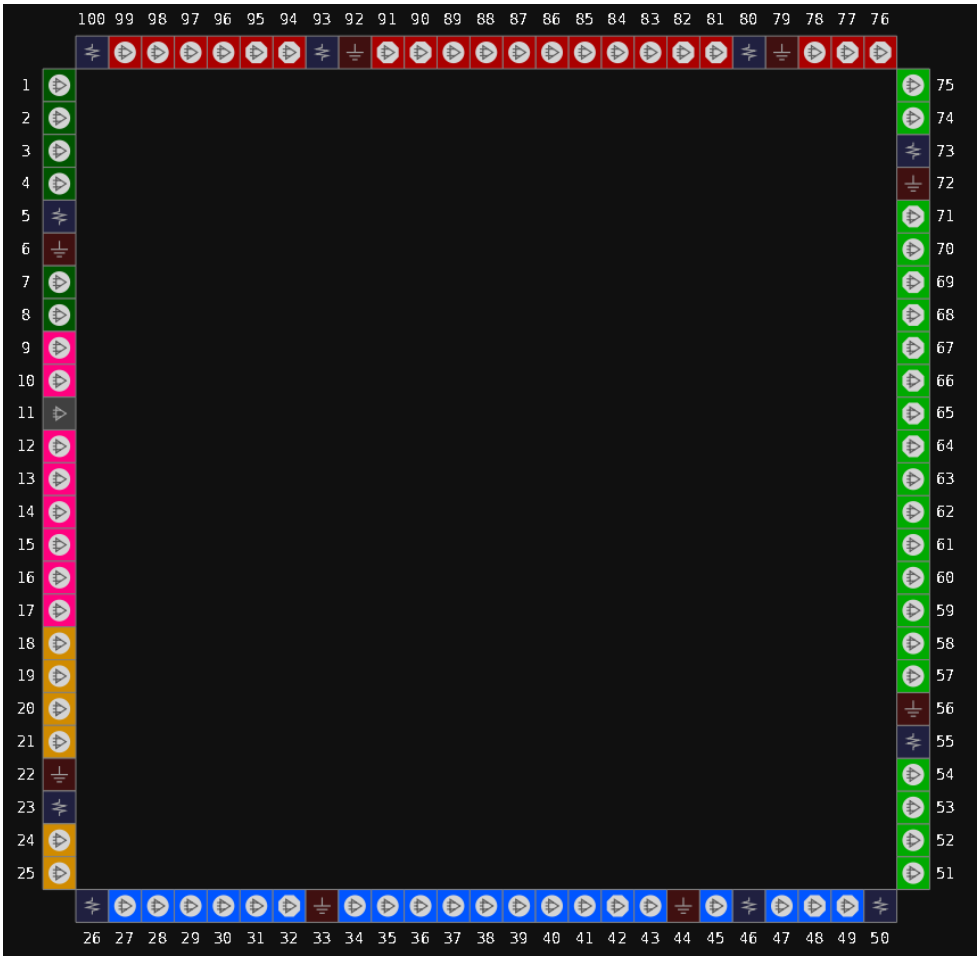


Table 3-31 Other Pins in GW1N-1P5 LQ100 (LV Version)

VCC	100,50
VCCO0	80,93
VCCO2	26,46
VCCO3	23
VCCO4/VCCO5	5
VCCO1/VCCX	55,73
VSS	6,22,33,44,56,72,79,92
NC	11

3.4.4 View of LQ100 Pins Distribution (UV Version)

Figure 3-32 View of GW1N-1P5 LQ100 Pins Distribution (UV Version, Top View)

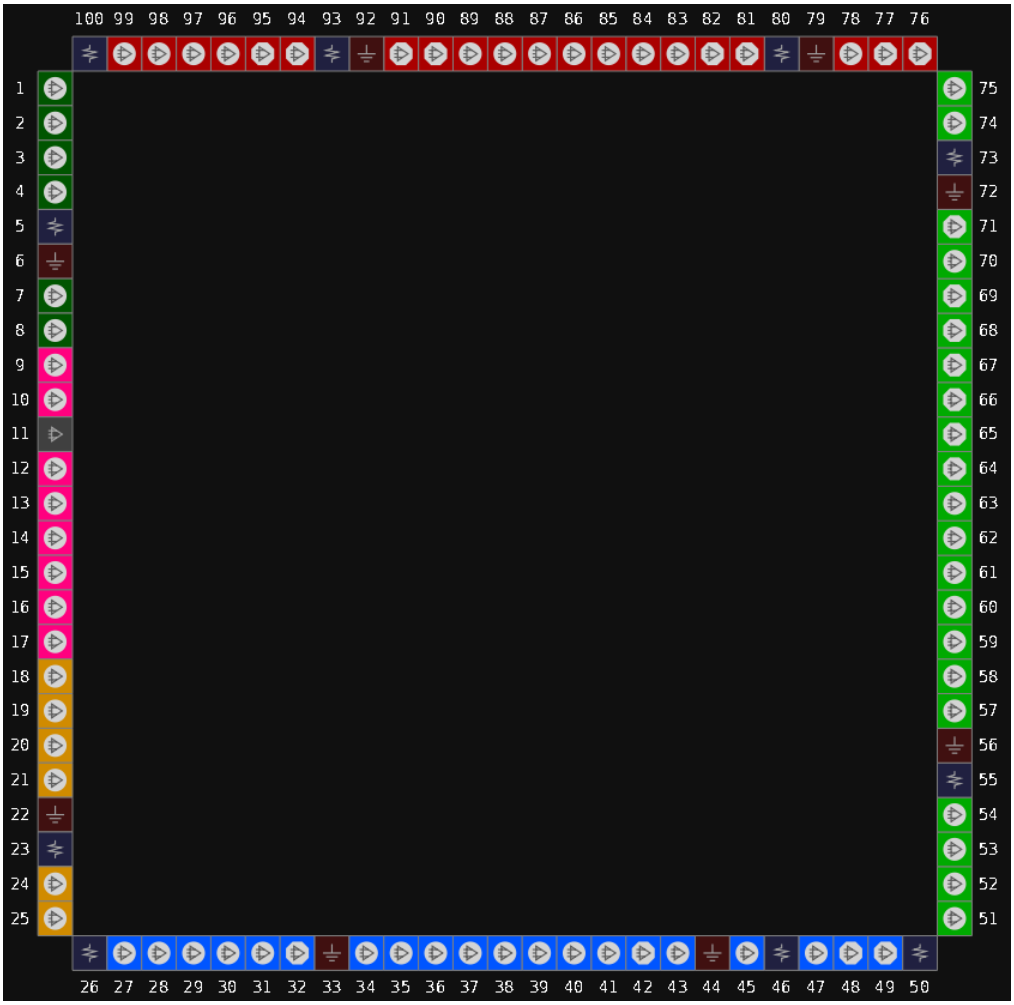


Table 3-32 Other Pins in GW1N-1P5 LQ100 (UV Version)

VCCO0	80,93
VCCO1	55,73
VCCO2	26,46
VCCO3	23
VCCO4/VCCO5	5
VCC/VCCX	100,50
VSS	6,22,33,44,56,72,79,92
NC	11

3.4.5 View of QN48X Pins Distribution (LV Version)

Figure 3-33 View of GW1N-1P5 QN48X Pins Distribution (LV Version, Top View)

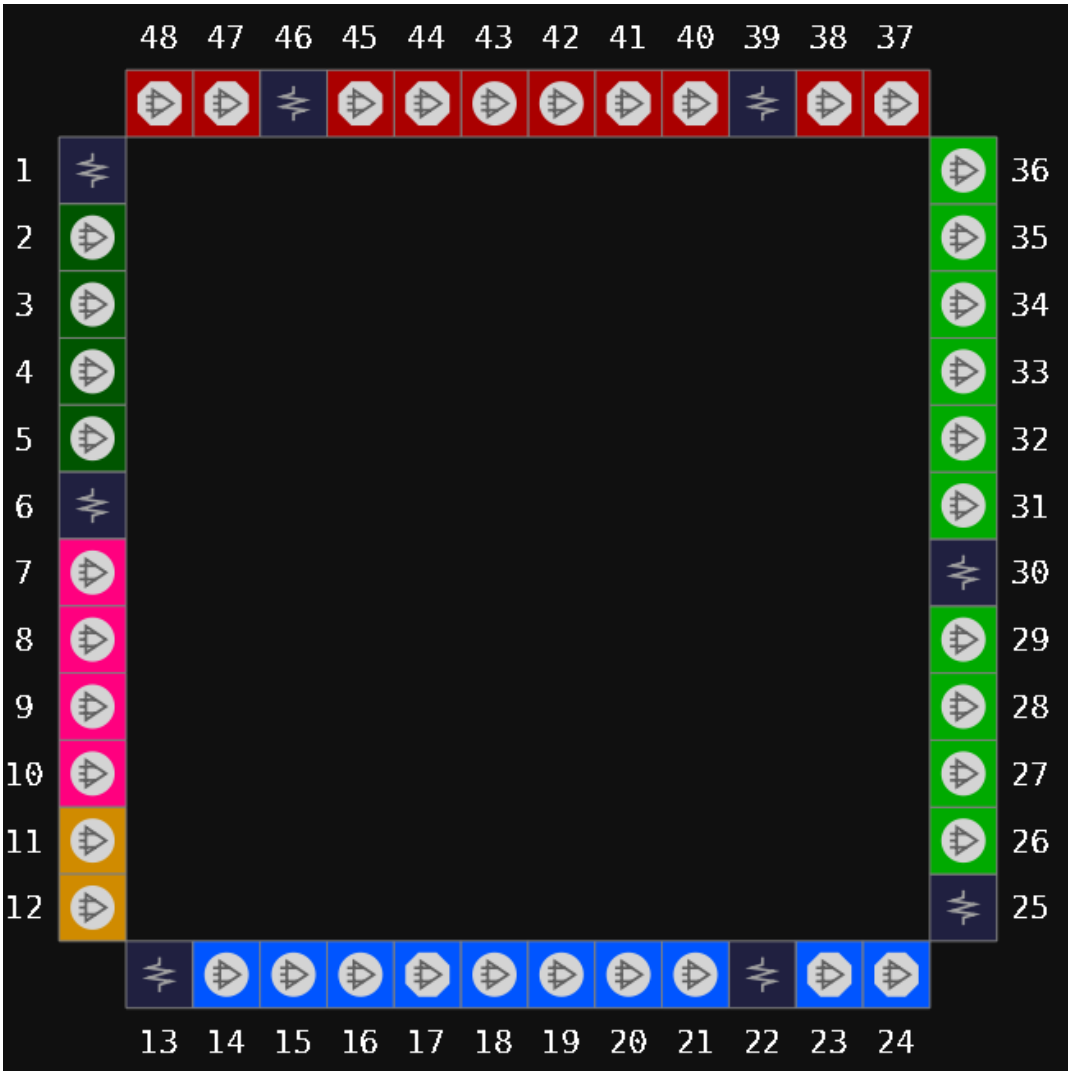


Table 3-33 Other Pins in GW1N-1P5 QN48X (LV Version)

VCC	1,25
VCCO0	39,46
VCCO2	13,22
VCCO3/VCCO4/VCCO5	6
VCCO1/VCCX	30

3.4.6 View of QN48X Pins Distribution (UV Version)

Figure 3-34 View of GW1N-1P5 QN48X Pins Distribution (UV Version, Top View)

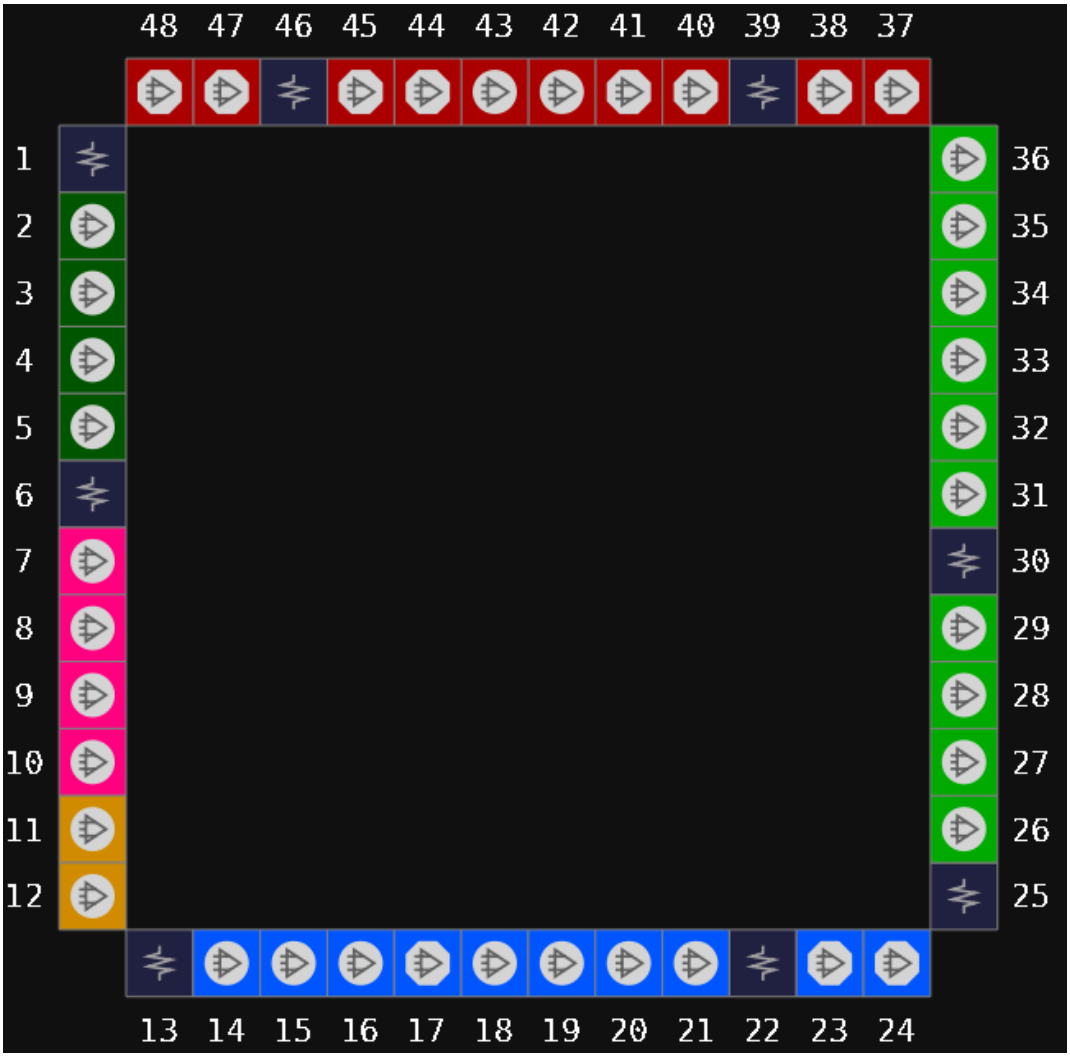


Table 3-34 Other Pins in GW1N-1P5 QN48X (UV Version)

VCC/VCCX	1,25
VCCO0	39,46
VCCO1	30
VCCO2	13,22
VCCO3/VCCO4/VCCO5	6

3.5 View of GW1N-4 Pins Distribution

3.5.1 View of QN32 Pins Distribution

Figure 3-35 View of GW1N-4 QN32 Pins Distribution (Top View)

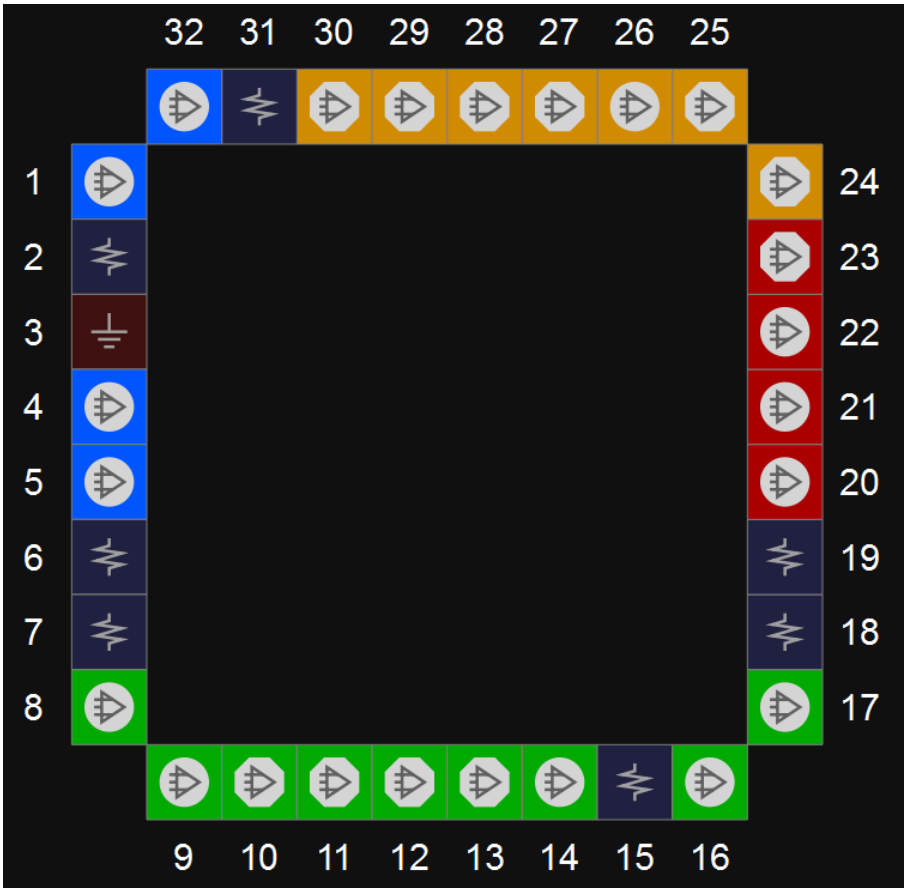


Table 3-35 Other Pins in GW1N-4 QN32

VCC	2, 18
VCCO0	19
VCCO1	7
VCCO2	6
VCCO3	31
VCCX	15
VSS	3

3.5.2 View of QN48 Pins Distribution

Figure 3-36 View of GW1N-4 QN48 Pins Distribution (Top View)

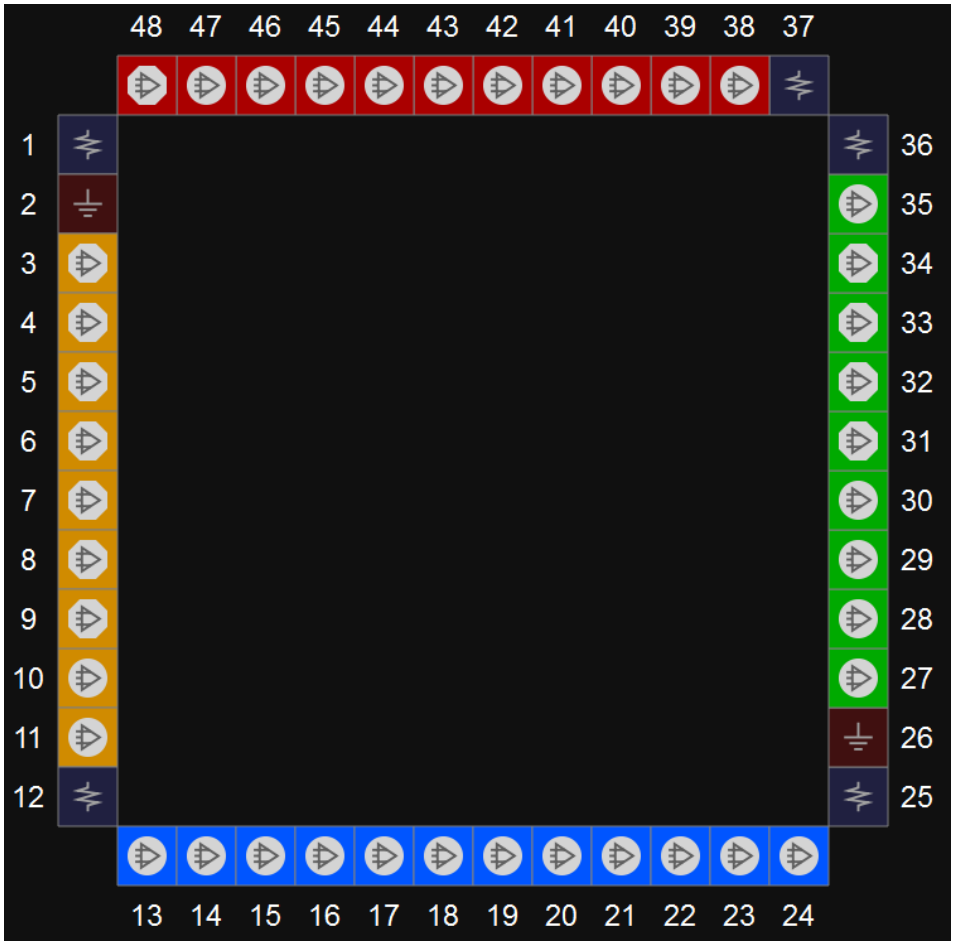


Table 3-36 Other Pins in GW1N-4 QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2, 26

3.5.3 View of CS72 Pins Distribution

Figure 3-37 View of GW1N-4 CS72 Pins Distribution (Top View)

Table 3-37 Other Pins in GW1N-4 CS72

VCC	A2，A8，H8
VCCO0	A5
VCCO1	D1
VCCO2	H5
VCCO3	E9
VCCX	H2
VSS	A1，A9，D9，E1，H1，H9

3.5.4 View of QN88 Pins Distribution

Figure 3-38 View of GW1N-4 QN88 Pins Distribution (Top View)

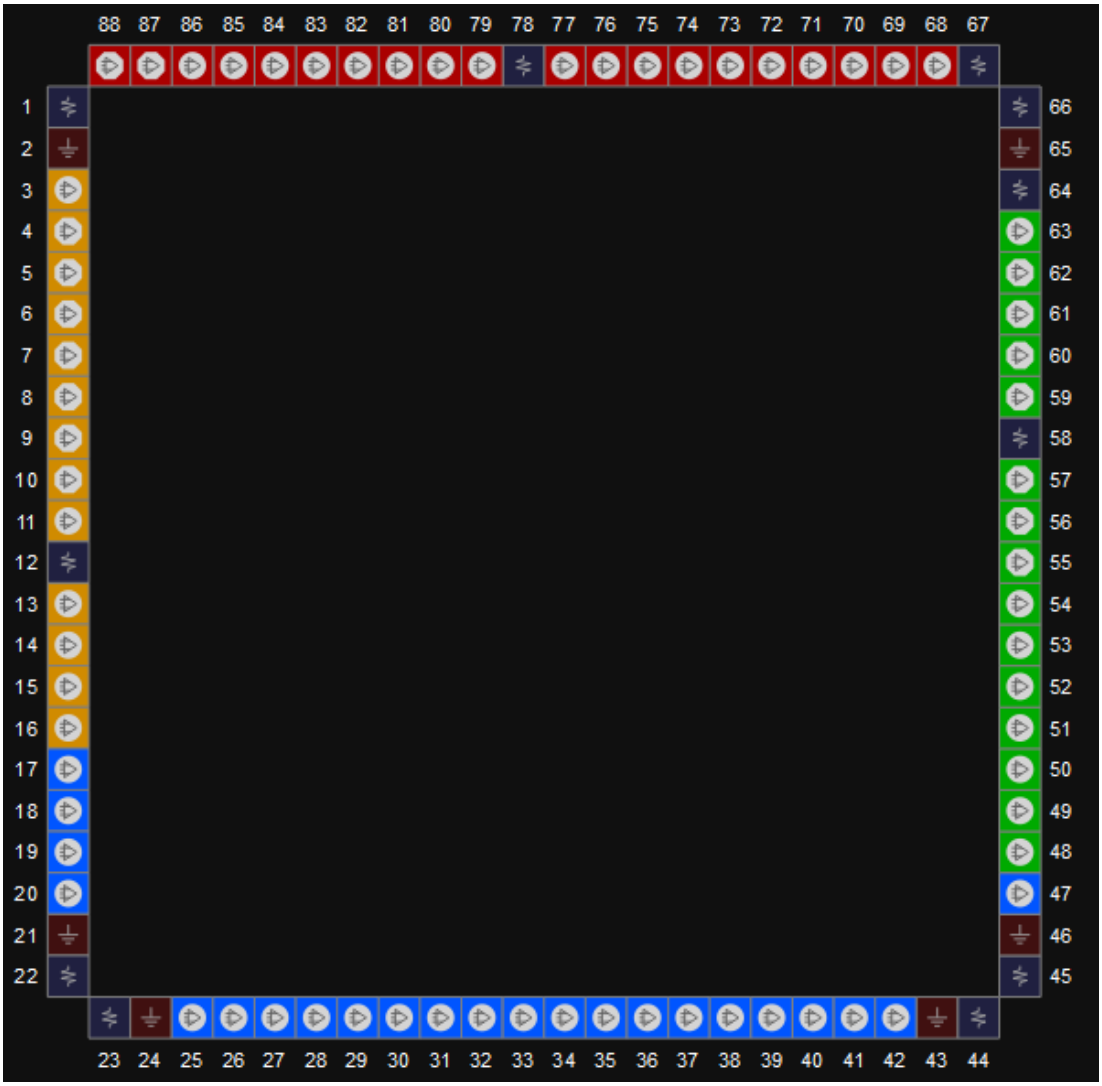


Table 3-38 Other Pins in GW1N-4 QN48

VCC	1, 22, 45, 66
VCCO0	67
VCCO1	58
VCCO2	23, 44
VCCO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

3.5.5 View of LQ100 Pins Distribution

Figure 3-39 View of GW1N-4 LQ100 Pins Distribution (Top View)

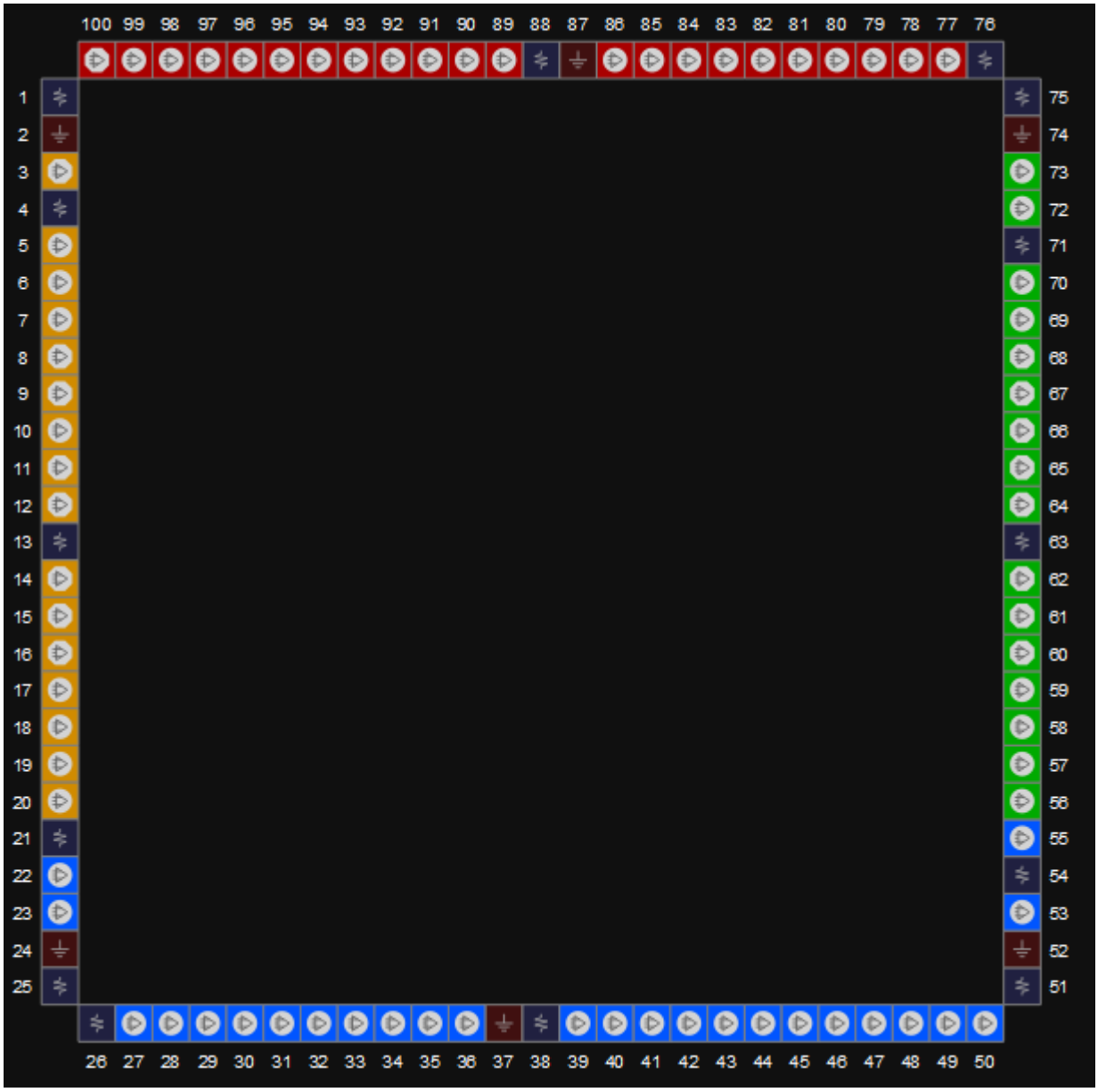


Table 3-39 Other Pins in GW1N-4 LQ100

VCC	1, 25, 51, 75
VCCO0	76, 88
VCCO1	54, 63
VCCO2	26, 38
VCCO3	4, 13
VCCX	21, 71
VSS	2, 24, 37, 52, 74, 87

3.5.6 View of MG132X Pins Distribution

Figure 3-40 View of GW1N-4 MG132X Pins Distribution (Top View)

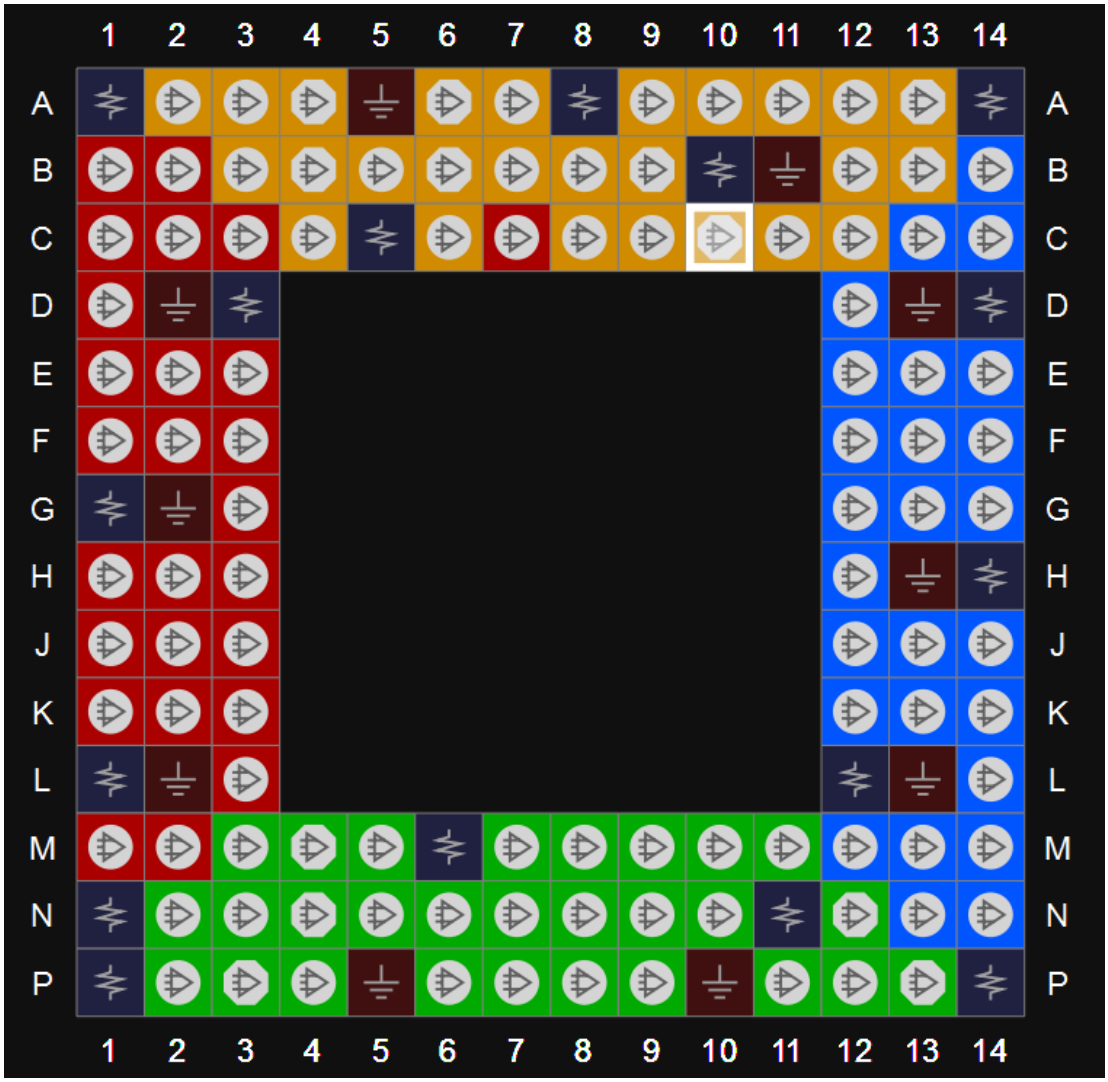


Table 3-40 Other Pins in GW1N-4 MG132X

VCC	A1,A14,N1,P14
VCCO0	D3,G1,L1
VCCO1	M6,N11,P1
VCCO2	D14,H14,L2
VCCO3	A8,B10,C5
VSS	A5,B11,D13,D2,G2,H13,L13,L2,P10,P5

3.5.7 View of LQ144 Pins Distribution

Figure 3-41 View of GW1N-4 LQ144 Pins Distribution (Top View)

Table 3-41 Other Pins in GW1N-4 LQ144

VCC	1, 36, 73, 108
VCCO0	109, 127
VCCO1	77, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 103
VSS	2, 17, 33,35, 53, 74, 89, 105,107, 125

3.5.8 View of MG160 Pins Distribution

Figure 3-42 View of GW1N-4 MG160 Pins Distribution (Top View)

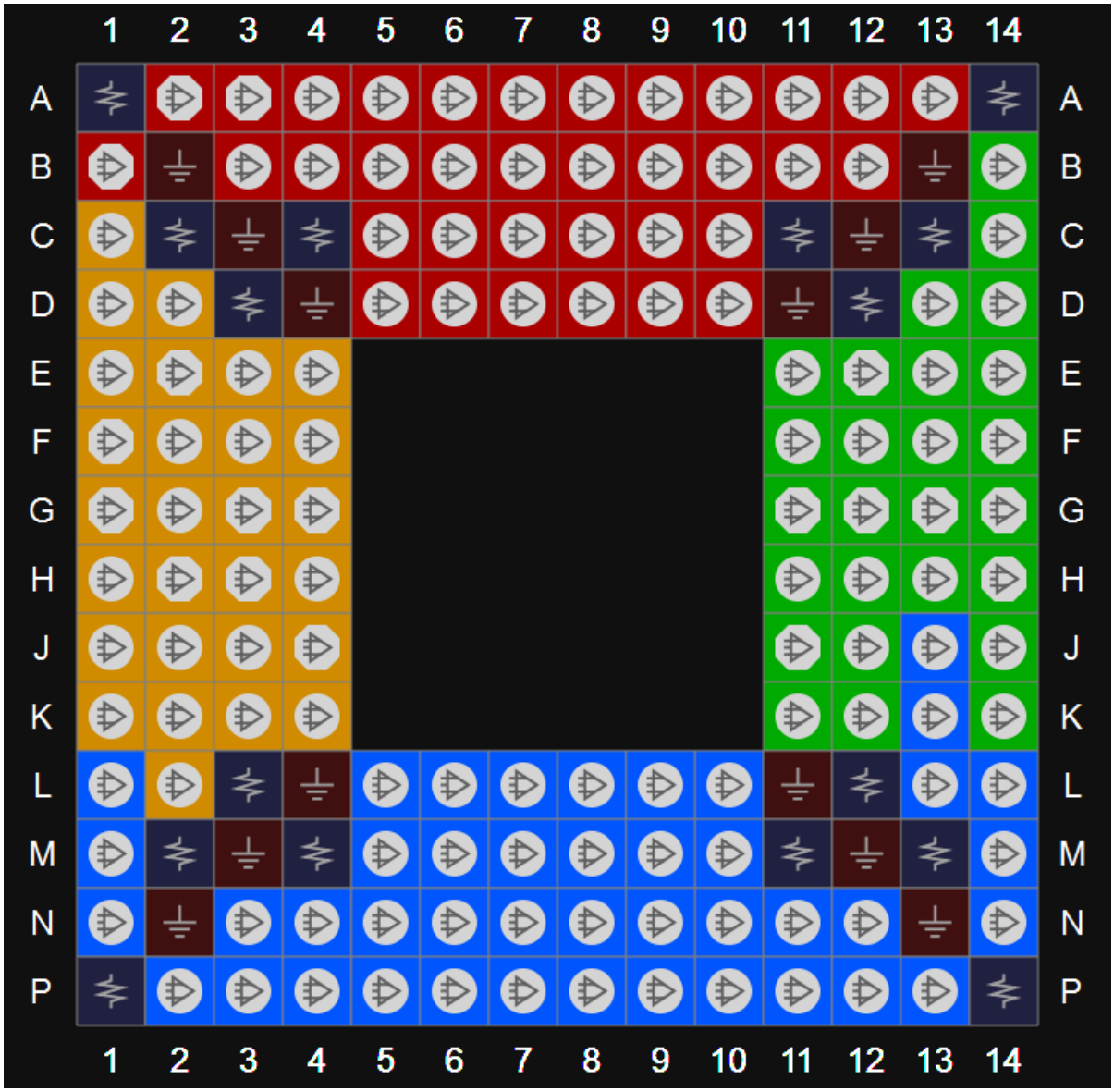


Table 3-42 Other Pins in GW1N-4/MG160

VCC	A1, A14, P1, P14
VCCO0	C4, C11
VCCO1	D12, L12
VCCO2	M4, M11
VCCO3	D3, L3
VCCX	C2, C13, M2, M13
VSS	B2, B13, C3, C12, D4, D11, L4, L11, M3, M12, N2, N13

3.5.9 View of PG256 Pins Distribution

Figure 3-43 View of GW1N-4 PG256 Pins Distribution (Top View)

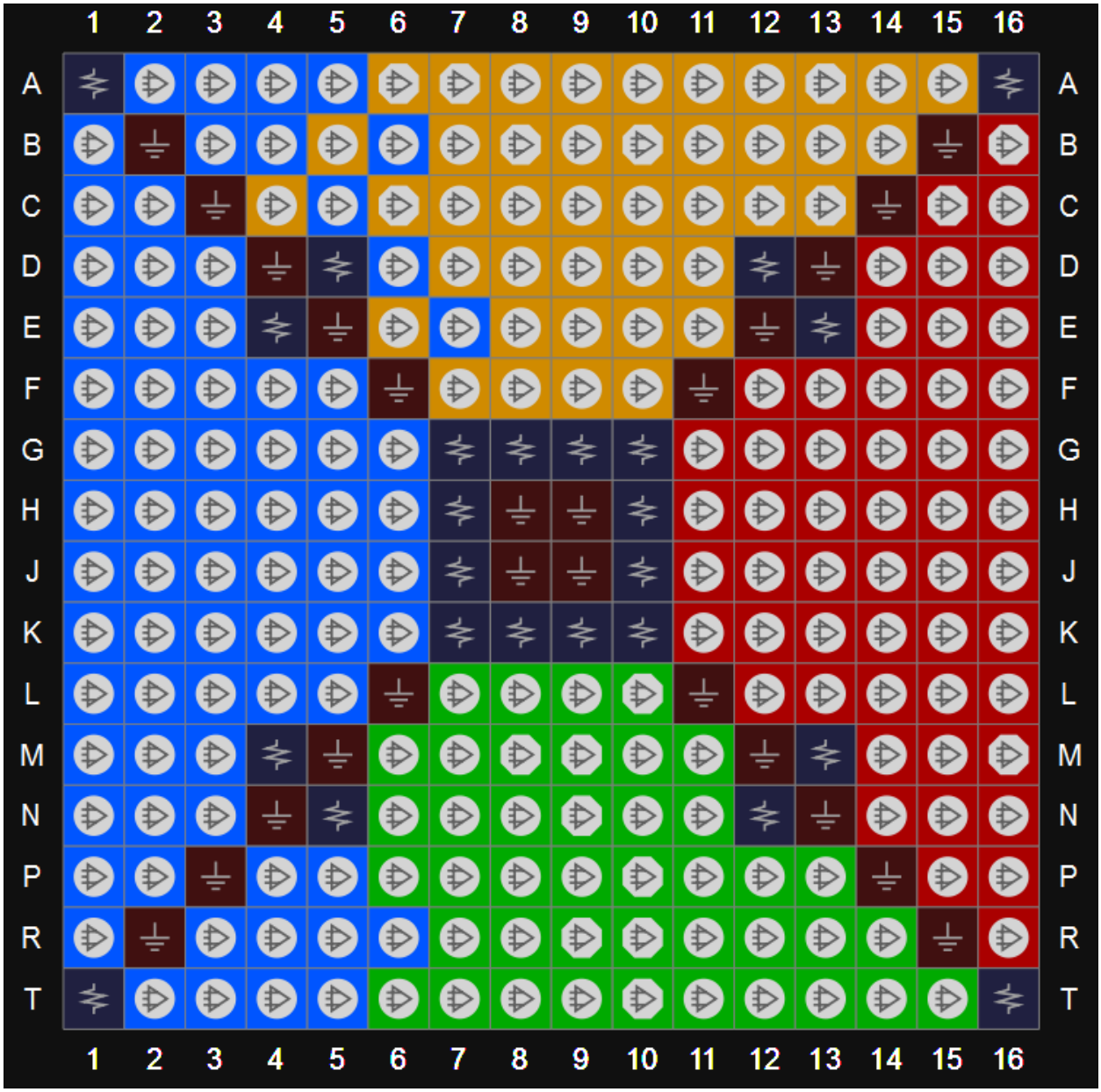


Table 3-43 Other Pins for GW1N-4 PG256

VCC	A1，A16，G7，G10，K7，K10，T1，T16
VCCO0	E13，J10，M13，H10
VCCO1	K8，N5，N12
VCCO2	E4，H7，M4，J7
VCCO3	D12，D5，G9
VCCX	G8，K9
VSS	B2，B15，C3，C14，D4，D13，E5，E12，F6，F11，H8，H9，J8，J9，L6，L11，M5，M12，N4，N13，P3，P14，R2，R15

3.5.10 View of PG256M Pins Distribution

Figure 3-44 View of GW1N-4 PG256M Pins Distribution (Top View)

Table 3-44 Other Pins in GW1N-4 PG256M

VCC	F10，G11，H10，H8，J7，J9，K6，L7
VCCO0	A14，A3，F8，F9
VCCO1	C16，J11，P16
VCCO2	L8，L9，T3,T14
VCCO3	C1，H6，P1
VCCX	H11，J6
VSS	A1，A16，B15，B2，F7，G10，G6，G7，G8，G9，K10，K11，K7，K8，K9，L10，R2，R15，T1，H9，H7，J10，J8

3.6 View of GW1N-9 Pins Distribution

3.6.1 View of QN48 Pins Distribution

Figure 3-45 View of GW1N-9 QN48 Pins Distribution (Top View)

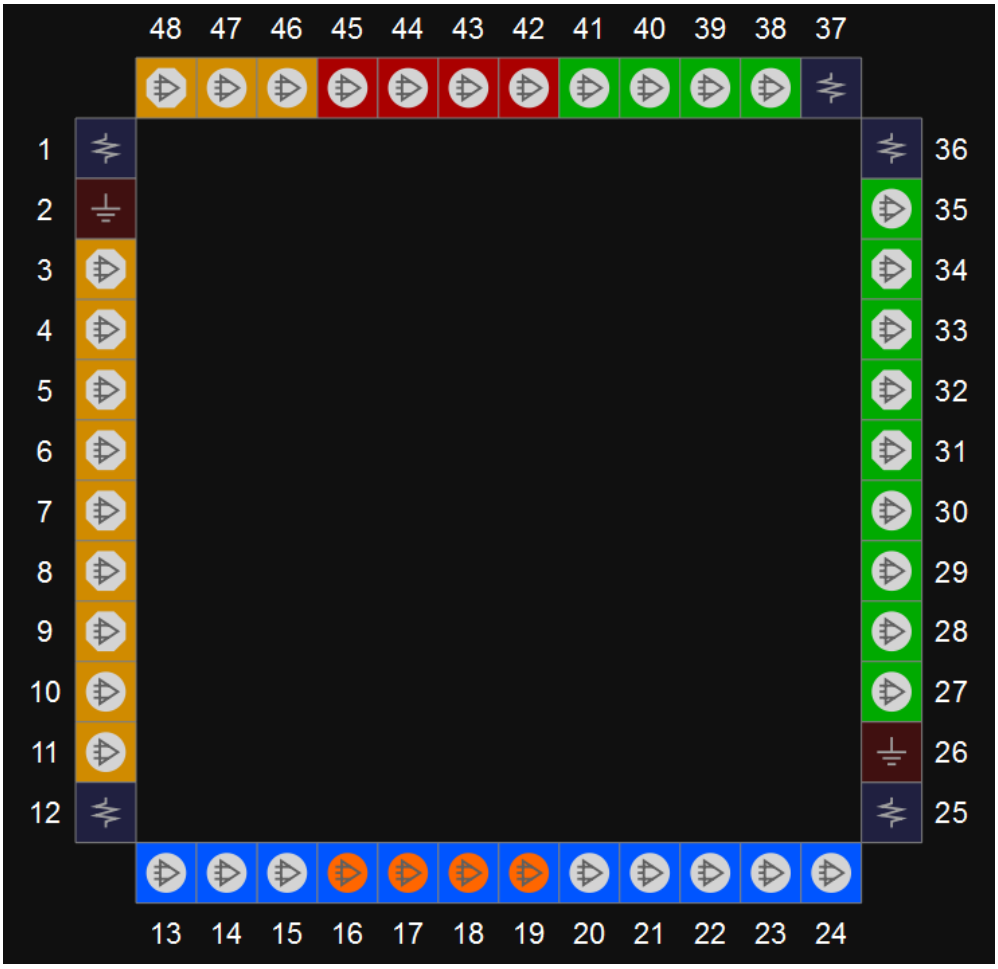


Table 3-45 Other Pins in GW1N-9 QN48

VCC	12, 37
VCCO0/VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2, 26

3.6.2 View of CM64 Pins Distribution

Figure 3-46 View of GW1N-9 CM64 Pins Distribution (Top View)

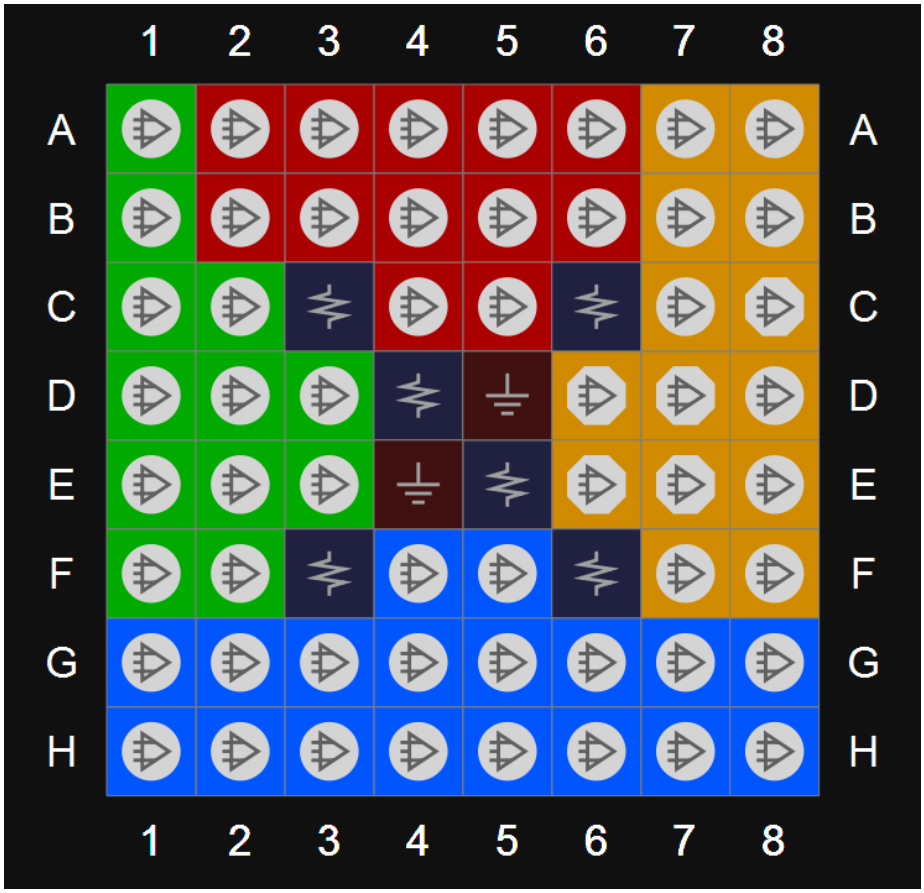


Table 3-46 Other Pins in GW1N-9 CM64

VCC	D4, E5
VCCO0/VCCO2	C6
VCCO1/VCCO3	F3
VCCX	C3, F6
VSS	D5, E4

3.6.3 View of CS81M Pins Distribution

Figure 3-47 View of GW1N-9 CS81M Pins Distribution (Top View)

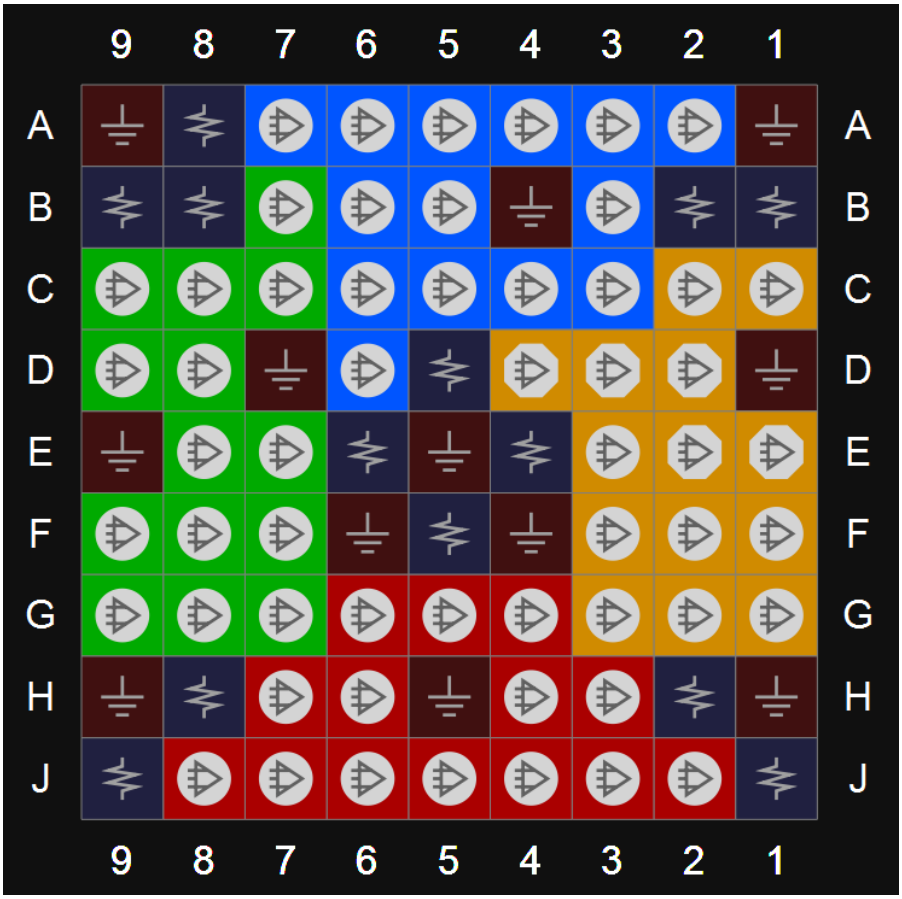


Table 3-47 Other Pins in GW1N-9 CS81M

VCC	A8、B2、B9、H2、H8
VCCO0	F5
VCCO1	E6
VCCO2	D5
VCCO3	E4
VCCX	B1、B8、J1、J9
VSS	A1、A9、B4、D1、D7、E5、E9、F4、F6、H1、H5、H9

3.6.4 View of QN88 Pins Distribution

Figure 3-48 View of GW1N-9 QN88 Pins Distribution (Top View)

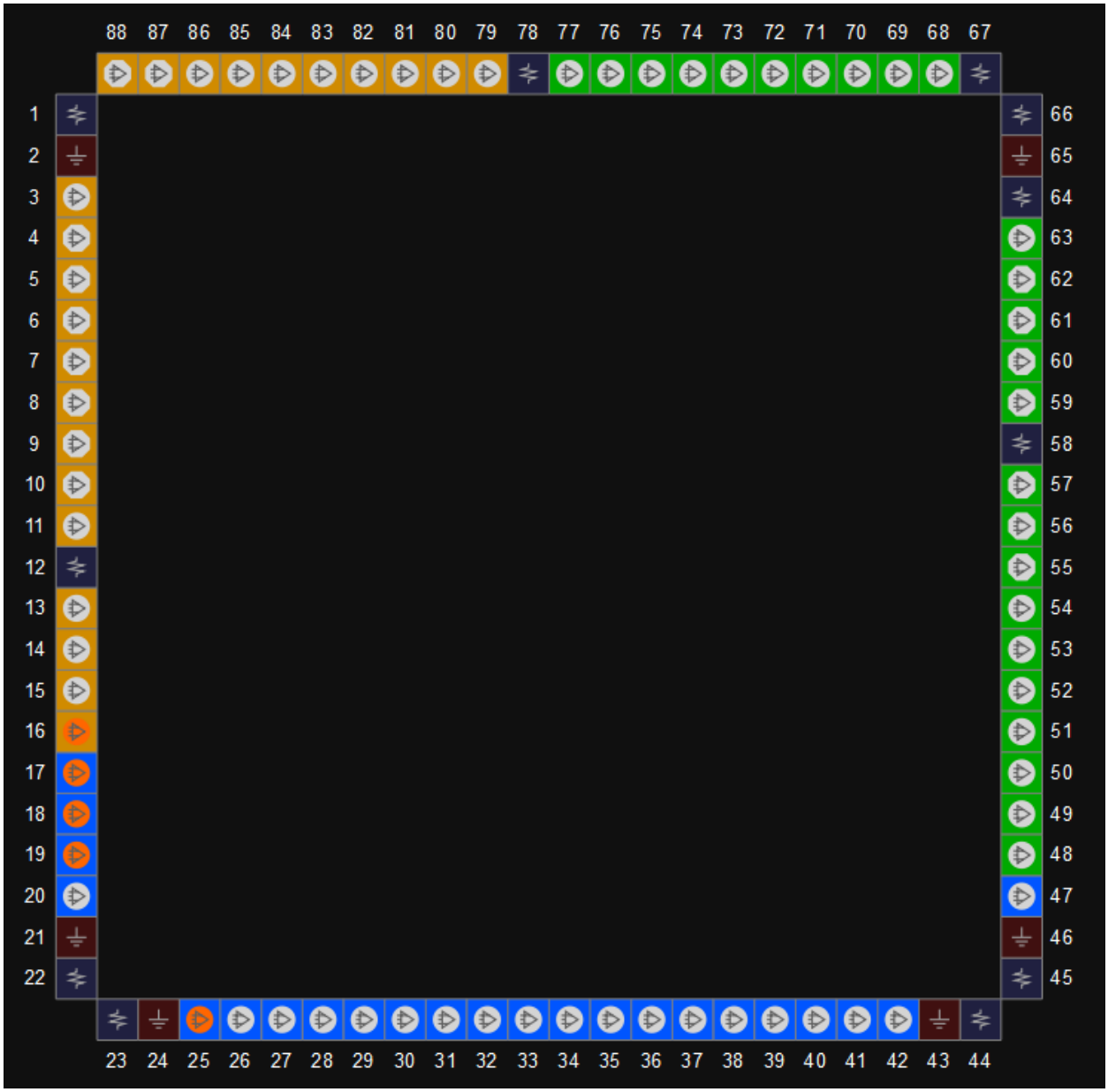


Table 3-48 Other Pins in GW1N-9 QN88

VCC	1, 22, 45, 66
VCCO0	67
VCCO1	58
VCCO2	23, 44
VCCO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

3.6.5 View of LQ100 Pins Distribution

Figure 3-49 GW1N-9 LQ100 Pins Distribution View (Top View)

Table 3-49 Other Pins in GW1N-9 LQ100

VCC	1, 25, 51, 75
VCCO0	76, 88
VCCO1	63, 71
VCCO2	26, 38
VCCO3	4, 13
VCCX	21, 54
VSS	2, 24, 52, 74, 87, 37

3.6.6 View of MG100 Pins Distribution

Figure 3-50 View of GW1N-9 MG100 Pins Distribution (Top View)

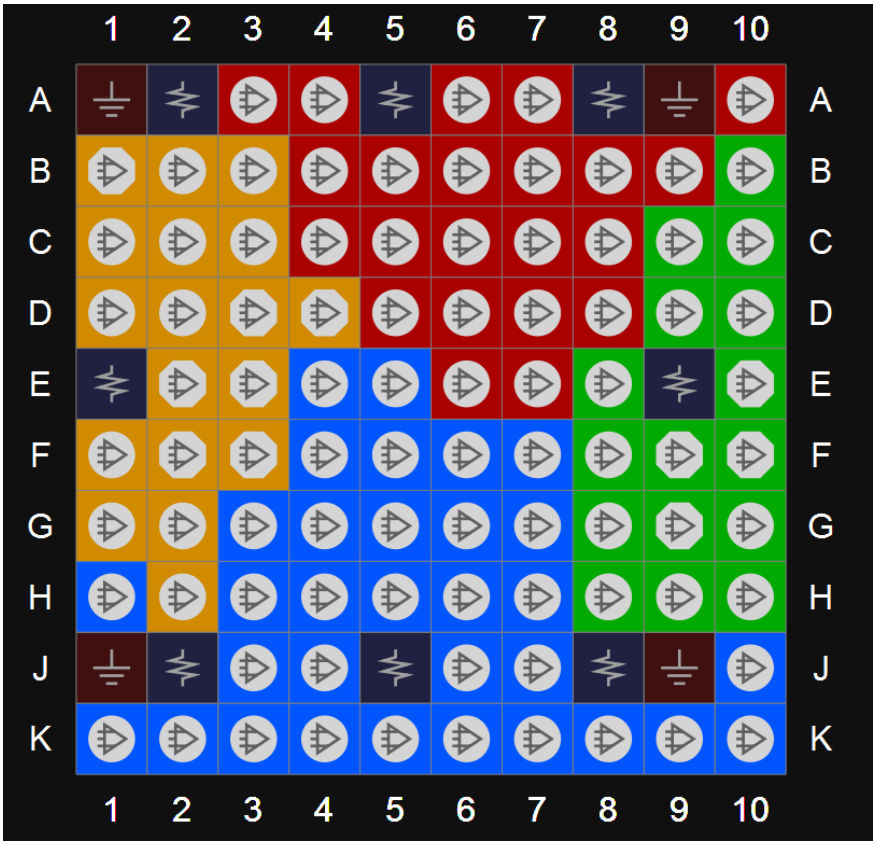


Table 3-50 Other Pins in GW1N-9 MG100

VCC	A2,A8,J2
VCCO0	A5
VCCO1	E9
VCCO2	J5
VCCO3	E1
VCCX	J8
VSS	A1,A9,J1,J9

3.6.7 View of LQ144 Pins Distribution

Figure 3-51 View of GW1N-9 LQ144 Pins Distribution (Top View)

Table 3-51 Other Pins in GW1N-9 LQ144

VCC	1, 36, 73, 108
VCCO0	109, 127
VCCO1	103, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 77
VSS	2, 17, 33, 35, 53, 74, 89, 105,107, 107, 125

3.6.8 View of EQ144 Pins Distribution

Figure 3-52 View of GW1N-9 EQ144 Pins Distribution (Top View)

Table 3-52 Other Pins in GW1N-9 EQ144

VCC	1, 36, 73, 108
VCCO0	109, 127
VCCO1	103, 91
VCCO2	37, 55
VCCO3	5, 19
VCCX	31, 77
VSS	2, 17, 33, 35, 53, 74, 89, 105,107

3.6.9 View of MG160 Pins Distribution

Figure 3-53 GW1N-9 MG160 Pins Distribution View (Top View)

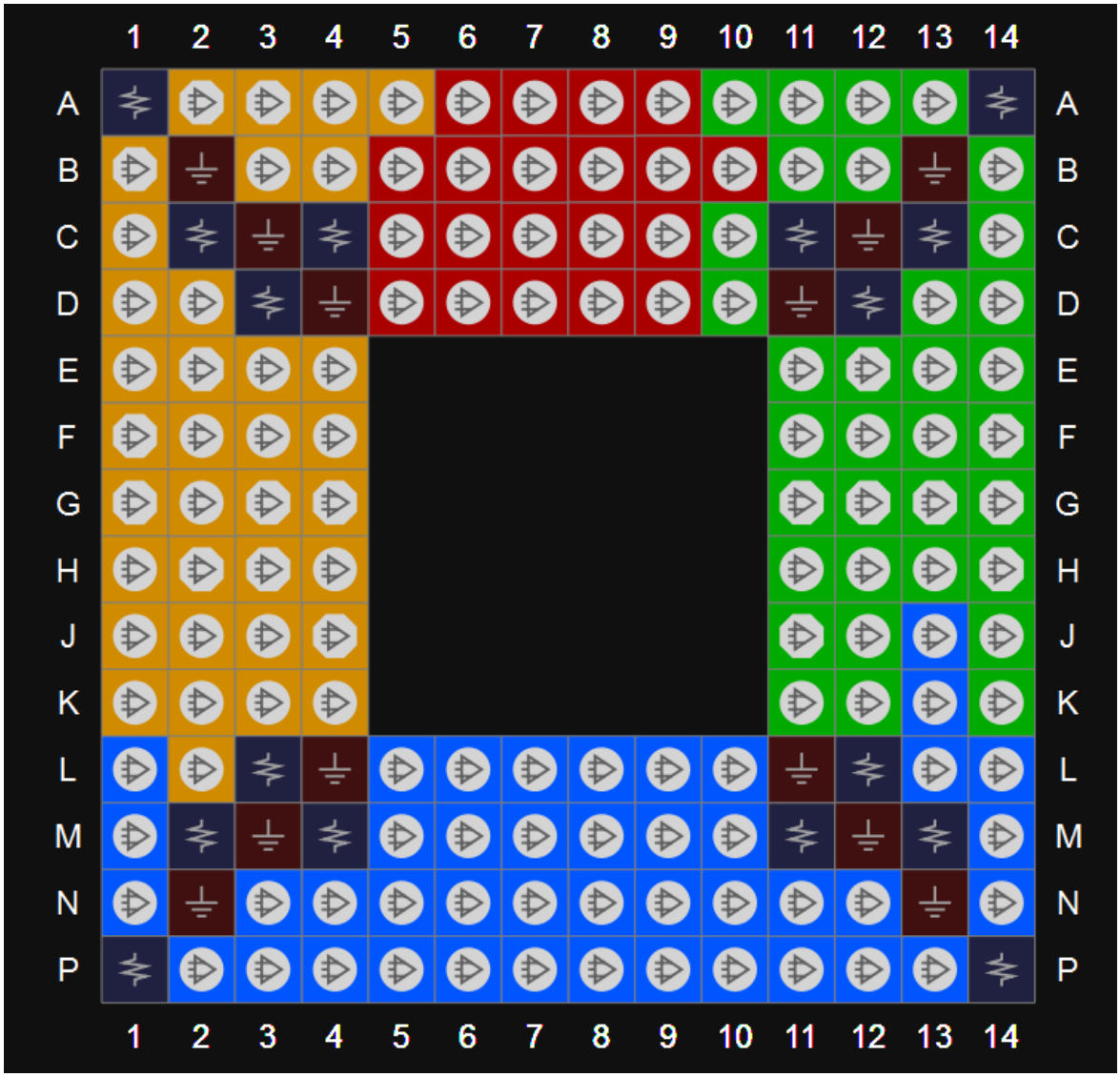


Table 3-53 Other Pins in GW1N-9 MG160

VCC	A1, A14, P1, P14
VCCO0	C4, C11
VCCO1	D12, L12
VCCO2	M11, M4
VCCO3	D3, L3
VCCX	C13, C2, M13, M2
VSS	B13, B2, C12, C3, D11, D4, L11, L4, M12, M3, N13, N2

3.6.10 View of UG169 Pins Distribution

Figure 3-54 View of GW1N-9 UG169 Pins Distribution (Top View)

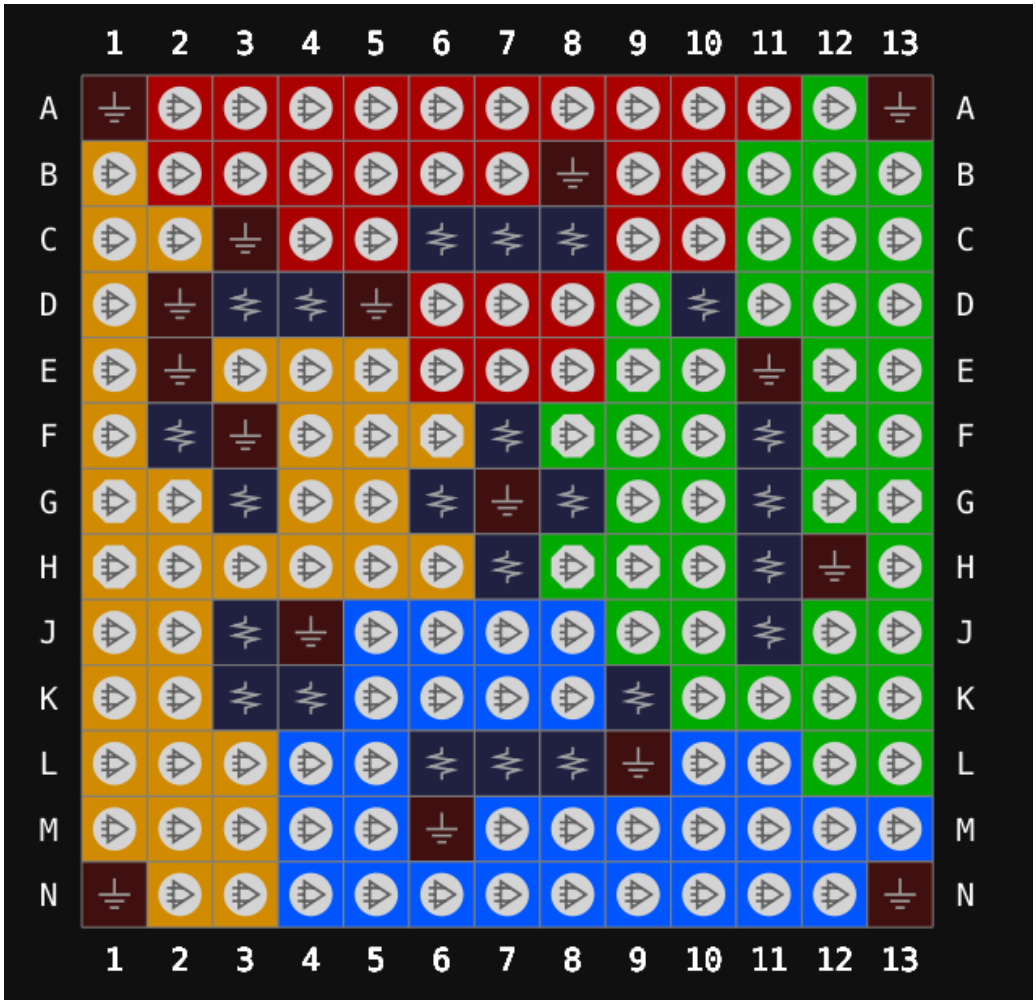


Table 3-54 Other Pins for GW1N-9 UG169

VCC	F7,G6,G8,H7
VCCO0	C6,C7,C8
VCCO1	F11,G11,H11,J11
VCCO2	L6,L7,L8
VCCO3	F2,G3,J3,K3
VCCX	D10,D3,D4,K4,K9
VSS	A1,A13,B8,C3,D2,D5,E11,E2,F3,G7,H12,J4,L9,M6,N1,N13

3.6.11 View of LQ176 Pins Distribution

Figure 3-55 View of GW1N-9 LQ176 Pins Distribution (Top View)

Table 3-55 Other Pins for GW1N-9 LQ176

VCC	1, 44, 89, 132
VCCO0	133, 155, 176
VCCO1	95, 110, 115
VCCO2	45, 65, 88
VCCO3	13, 22, 34
VCCX	40, 66, 130, 154
VSS	2, 43, 46, 87, 90, 131, 134, 175

3.6.12 View of EQ176 Pins Distribution

Figure 3-56 View of GW1N-9 EQ176 Pins Distribution (Top View)

Table 3-56 Other Pins in GW1N-9 EQ176

VCC	1, 44, 89, 132
VCCO0	133, 155, 176
VCCO1	95, 110, 115
VCCO2	45, 65, 88
VCCO3	13, 22, 34
VCCX	40, 66, 130, 154
VSS	2, 43, 46, 87, 90, 131, 134, 175

3.6.13 View of MG196 Pins Distribution

Figure 3-57 View of GW1N-9 MG196 Pins Distribution (Top View)

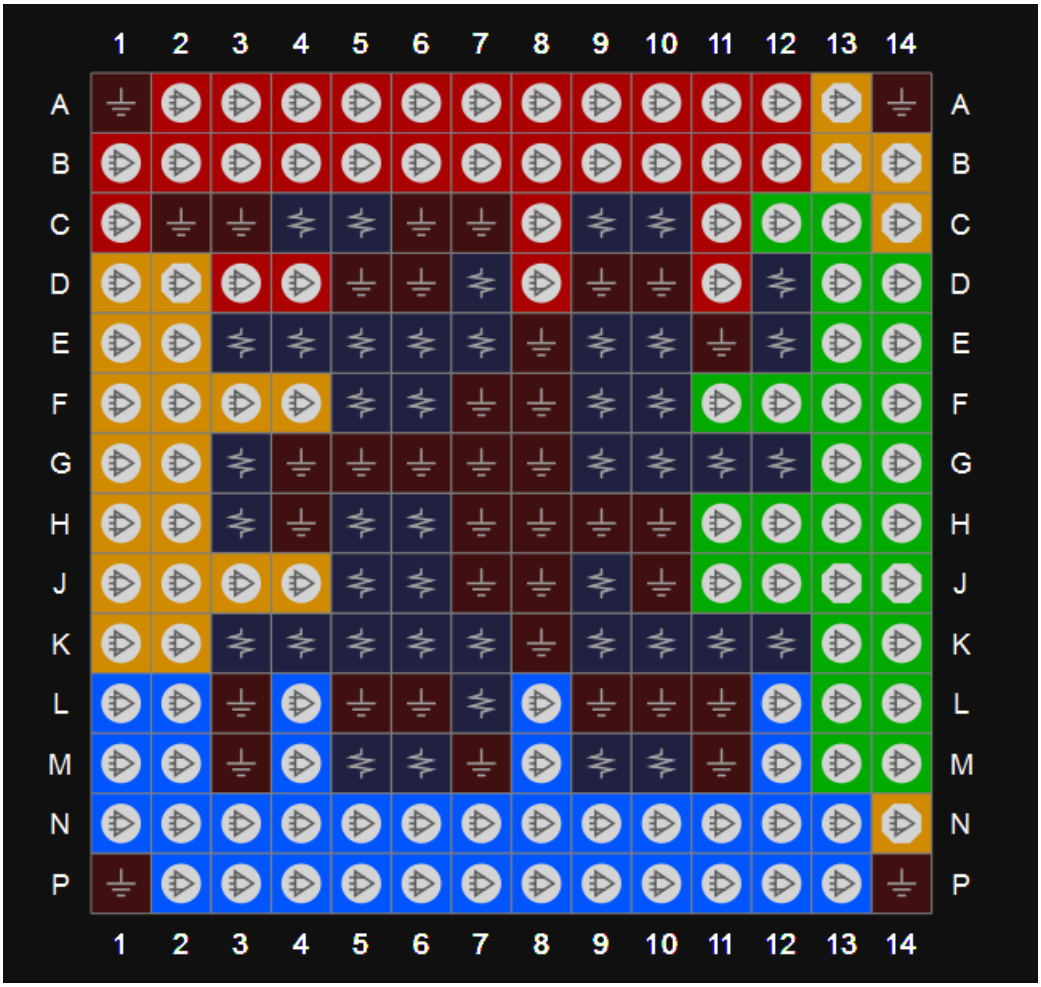


Table 3-57 Other Pins in GW1N-9 MG196

VCC	E10,E5,E6,E9,F10,F5,F6,F9,J5,J6,J9,K10,K5,K6,K9
VCCO0	C4,C10,C5,C9
VCCO1	D12,E12,G11,G12,K11,K12
VCCO2	M5,M10,M6,M9
VCCO3	E3,E4,G3,H3,K3,K4
VCCX	L7,K7,H6,H5,D7,E7,G10,G9
VSS	A14,A1,C3,C2,C7,C6,D5,D10,D9,D6,E8,E11,F7,F8,G4,G5,G6,G7,G8, H10,H4,H7,H8,H9,J10,J7,J8,K8,L10,L11,L3,L5,L6,L9,M11,M3,M7,P1, P14

3.6.14 View of PG256 Pins Distribution

Figure 3-58 View of GW1N-9 PG256 Pins Distribution (Top View)

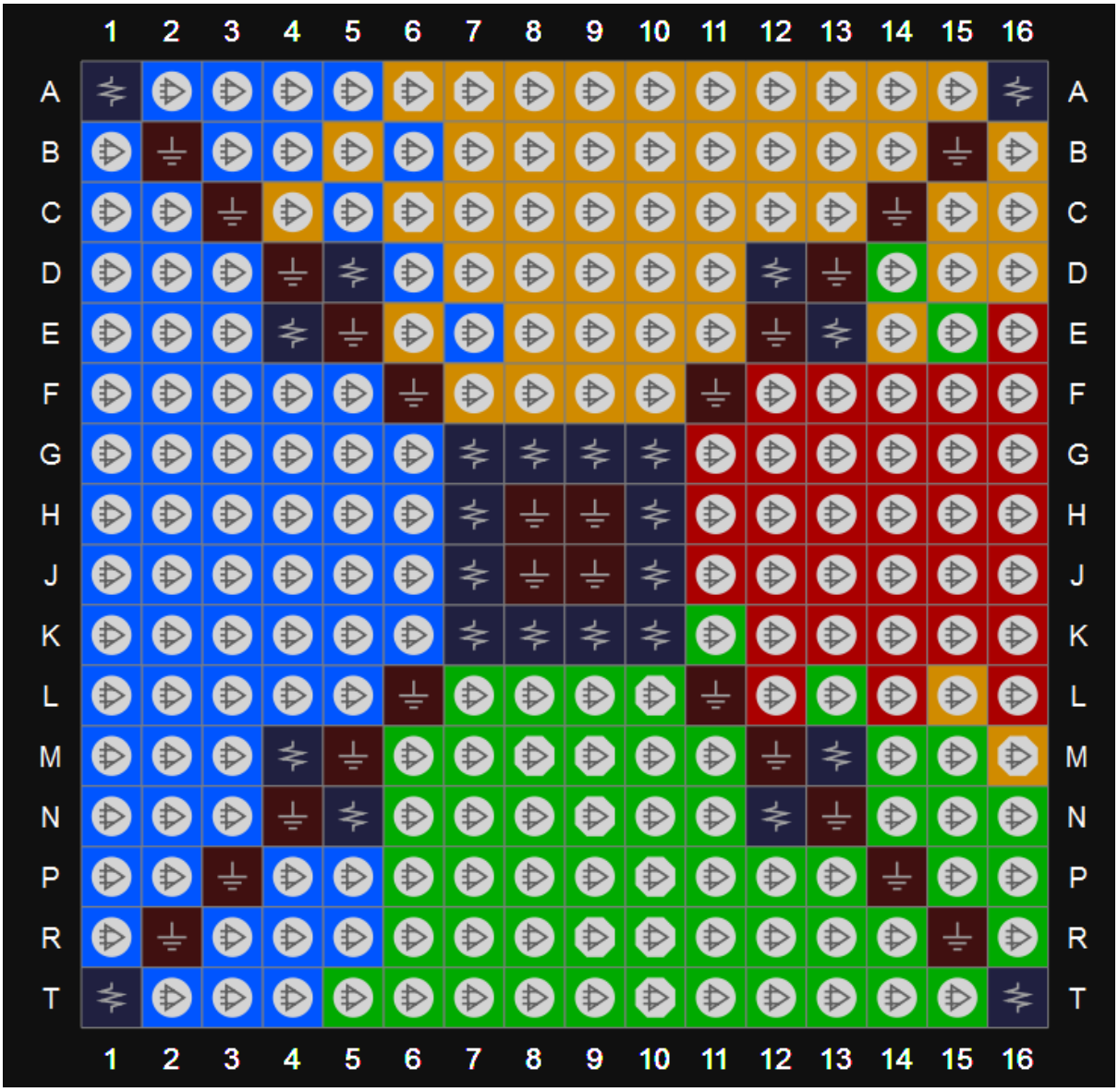


Table 3-58 Other Pins in GW1N-9 PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCCO0	E13, J10, M13, H10
VCCO1	K8, N5, N12
VCCO2	E4, H7, M4, J7
VCCO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9, J8, J9, L6, L11, M5, M12, N4, N13, P3, P14, R2, R15

3.6.15 View of UG256 Pins Distribution

Figure 3-59 View of GW1N-9 UG256 Pins Distribution (Top View)

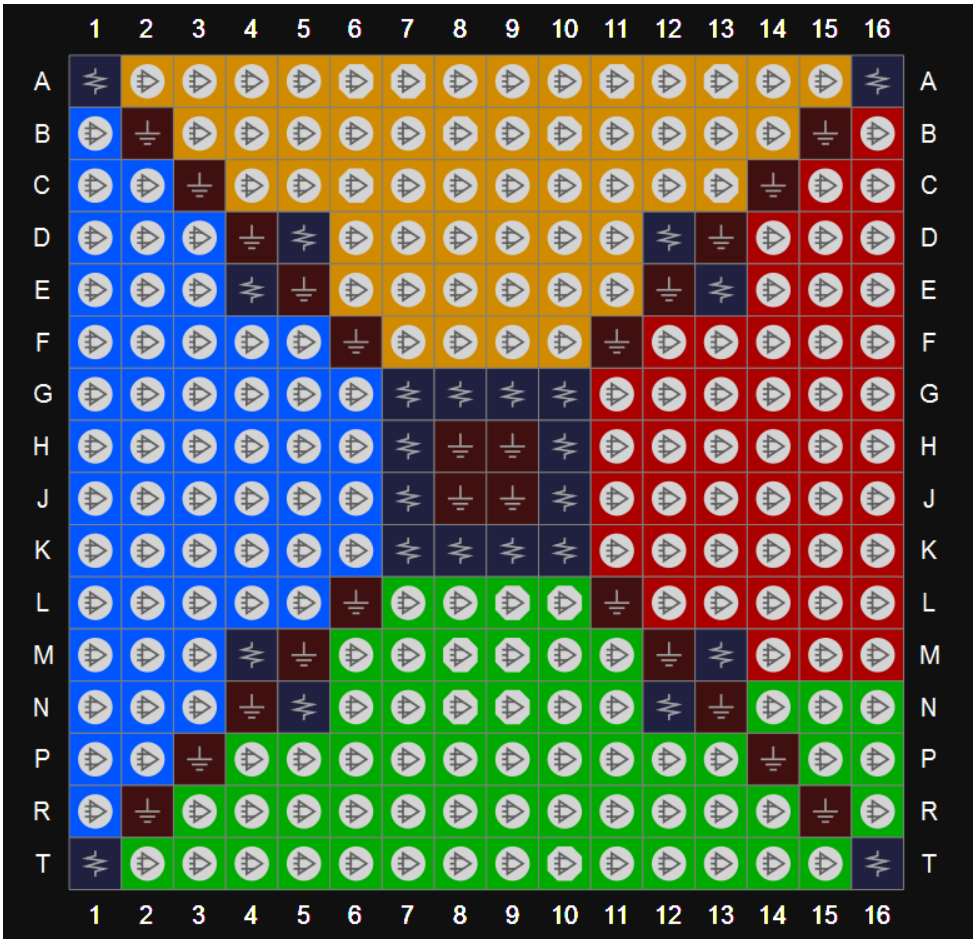


Table 3-59 Other Pins in GW1N-9 UG256

VCC	A1, A16, G10, G7, K10, K7, T1, T16
VCCO0	E13, H10, J10, M13
VCCO1	K8, K9, N12,N5
VCCO2	E4, H7, J7, M4
VCCO3	D12, D5, G9
VCCX	G8
VSS	B15, B2, C14, C3, D13, D4, E12, E5, F11, F6, H8, H9, J8, J9, L11, L6, M12, M5, N13, N4, P14, P3, R15, R2

3.6.16 View of UG332 Pins Distribution

Figure 3-60 View of GW1N-9 UG332 Pins Distribution (Top View)

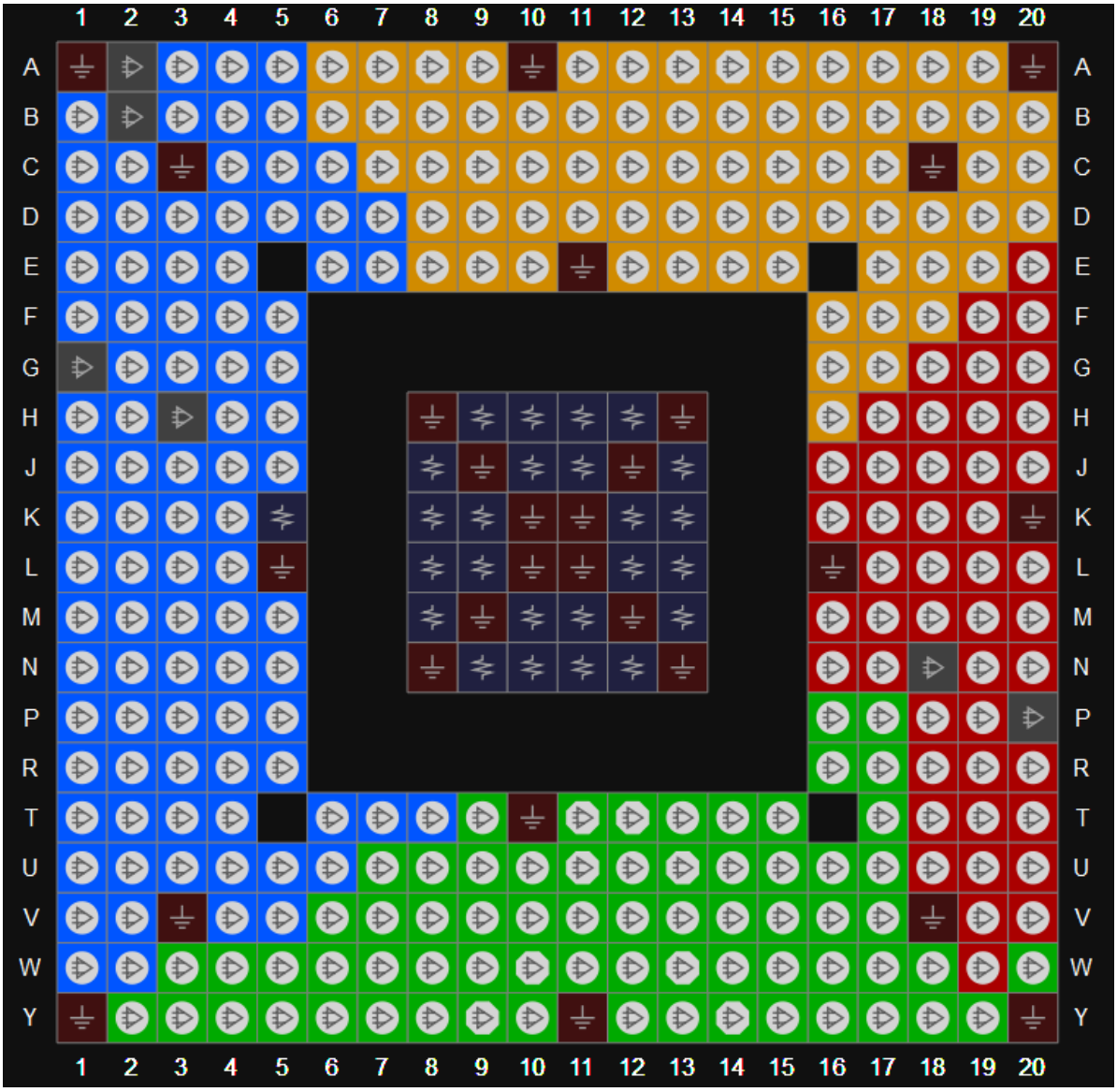


Table 3-60 Other Pins in GW1N-9 UG332

VCC	J10, J11, K9, K12, L9, L12, M10, M11
VCCO0	J13, K13, L13
VCCO1	N9, N10, N1, N12
VCCO2	J8, K5, K8, L8, M8
VCCO3	H11, H9, H12
VCCX	H10, M13
VSS	A1,A10, A20, C3, C18, E11, H8, H13, J9, J12, K10, K11, K20, L5, L10, L11, L16, M9, M12, N8, N13, T10, V3, V18, Y1, Y11, Y20
NC	N18, P20, G1, H3, A2, B2

3.6.17 View of QN48F Pins Distribution

Figure 3-61 View of GW1N-9 QN48F Pins Distribution (Top View)

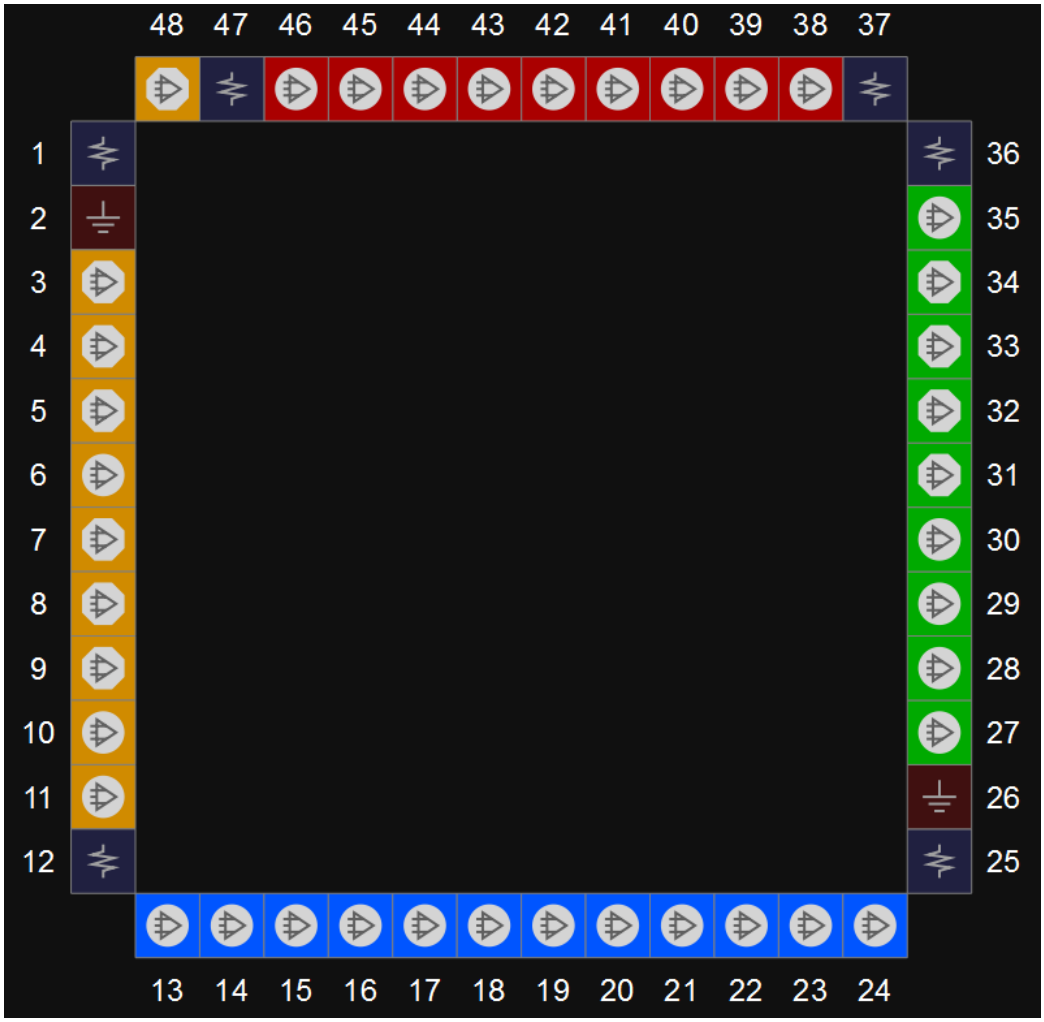


Table 3-61 Other Pins in GW1N-9 QN48F

VCC	12,37
VCCO0	47
VCCO3	1
VCCO1/VCCO2	25
VCCX	36
VSS	2,26

3.6.18 View of MG100T Pins Distribution

Figure 3-62 View of GW1N-9 MG100T Pins Distribution (Top View)

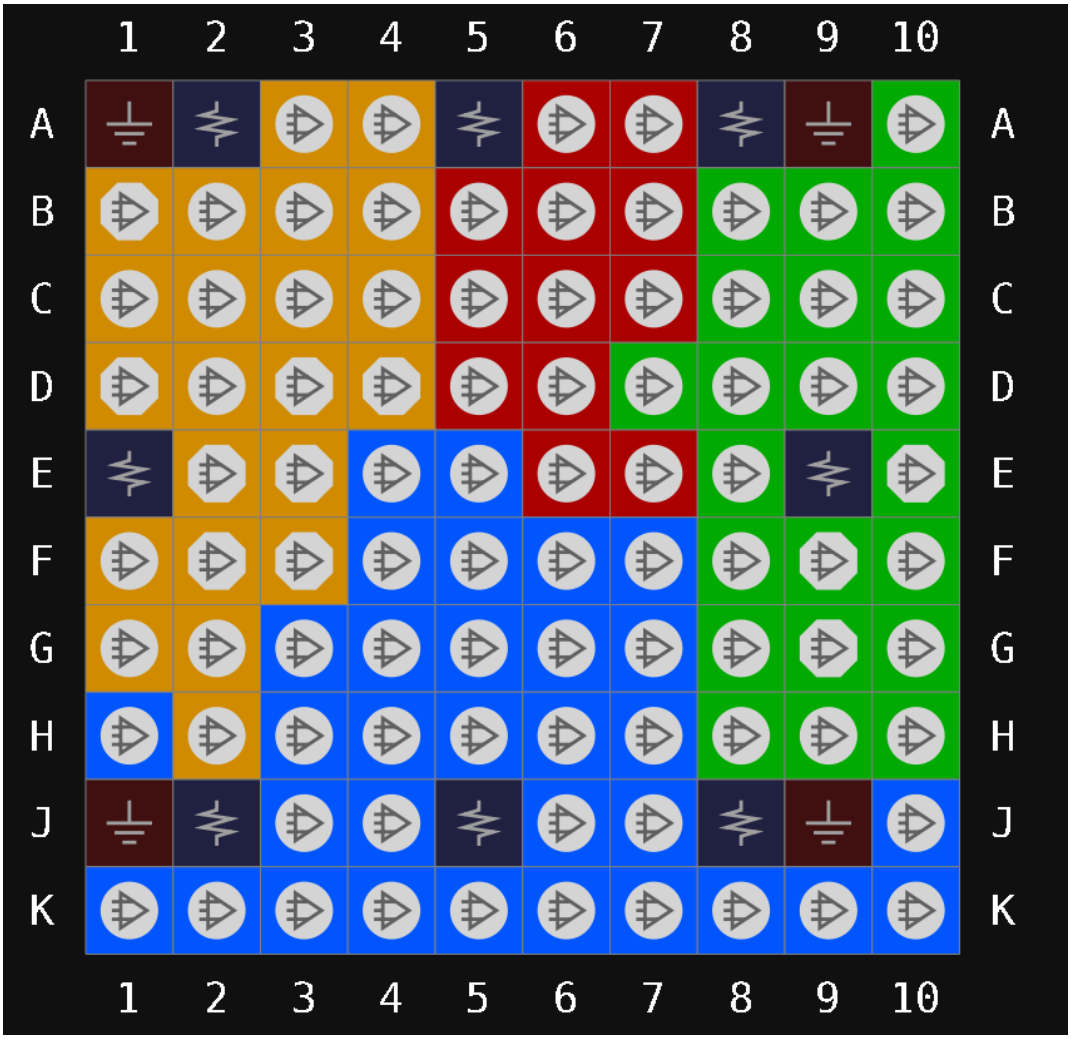


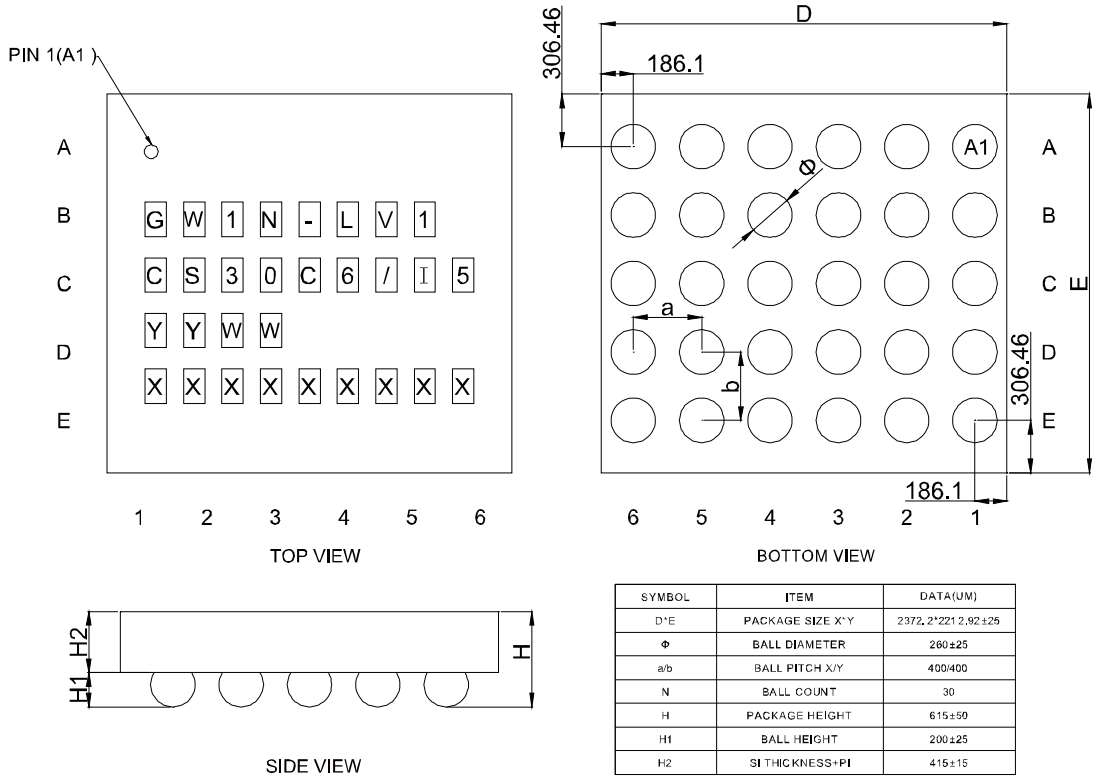
Table 3-62 Other Pins in GW1N-9 MG100T

VCC	J2,A8,A2
VCCO0	A5
VCCO1	E9
VCCO2	J5
VCCO3	E1
VCCX	J8
VSS	A1,A9,J1,J9

4 Package Diagrams

4.1 CS30 Package Outline (2.3mm x 2.4mm, GW1N-1)

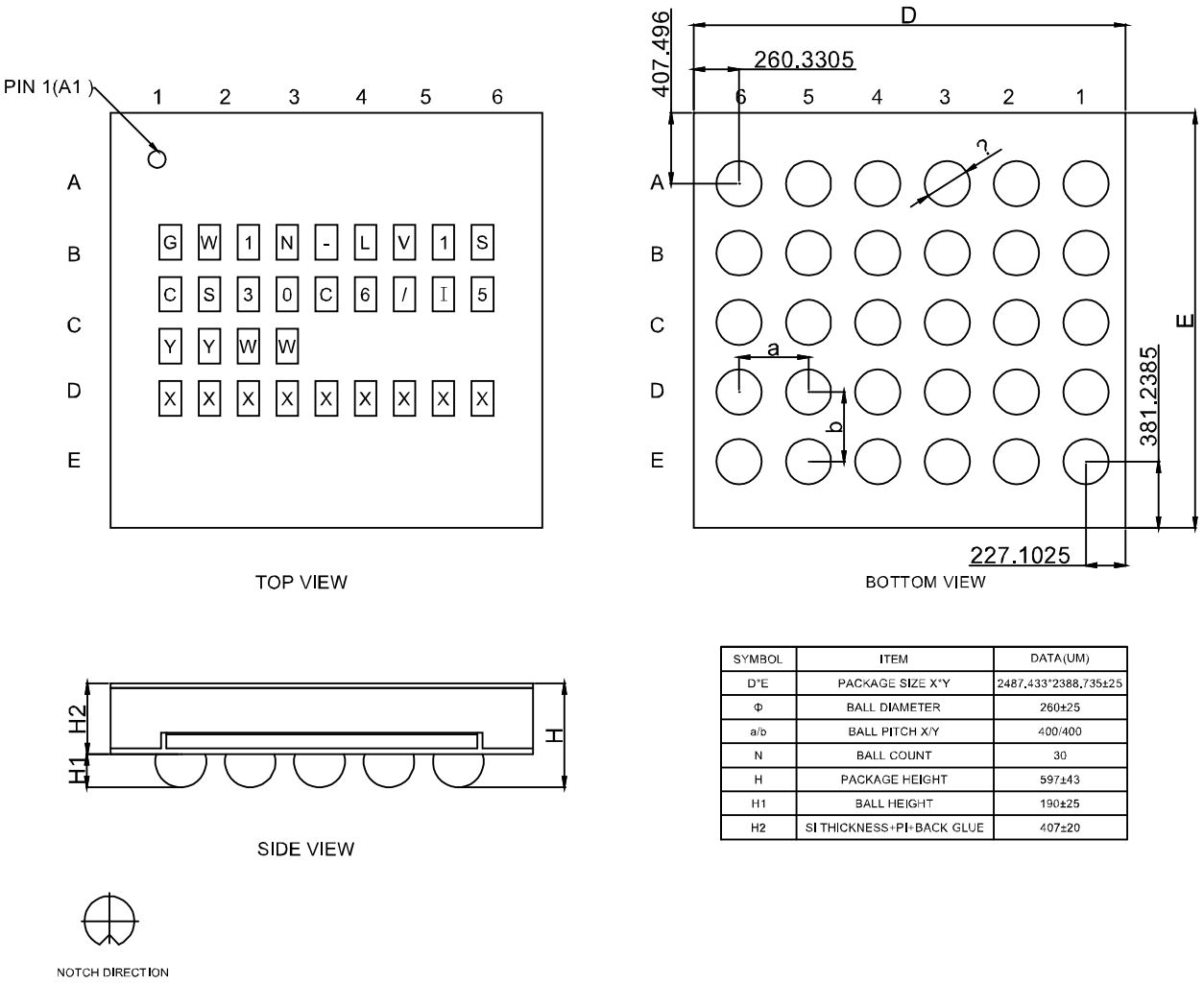
Figure 4-1 Package Outline CS30 (GW1N -1)



SYMBOL	ITEM	DATA(UM)
D*E	PACKAGE SIZE X*Y	2372.2*2212.92±25
Φ	BALL DIAMETER	260±25
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	30
H	PACKAGE HEIGHT	615±50
H1	BALL HEIGHT	200±25
H2	SI THICKNESS+PI	415±15

4.2 CS30 Package Outline (2.3mm x 2.4mm, GW1N-1S)

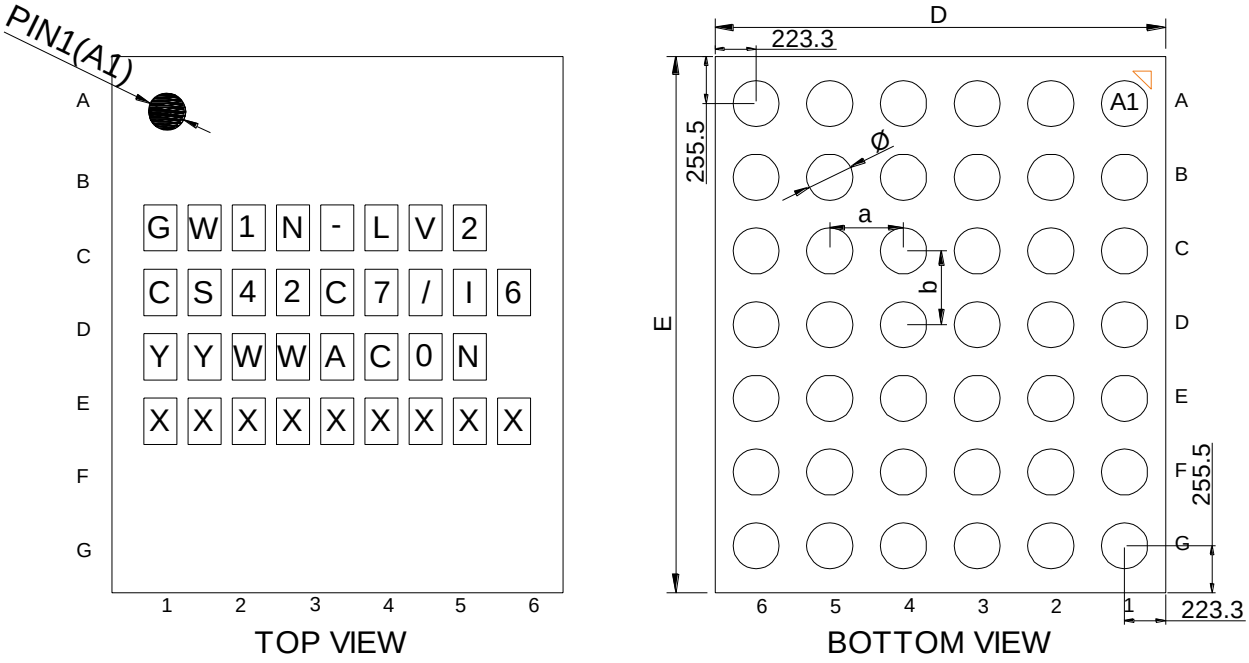
Figure 4-2 Package Outline CS30 (GW1N-1S)



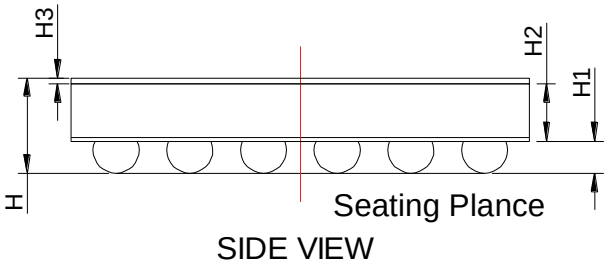
SYMBOL	ITEM	DATA(UM)
D*E	PACKAGE SIZE X*Y	2487.433*2388.735±25
Φ	BALL DIAMETER	260±25
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	30
H	PACKAGE HEIGHT	597±43
H1	BALL HEIGHT	190±25
H2	SI THICKNESS+PI+BACK GLUE	407±20

4.3 CS42 Package Outline (2.4mm x 2.9mm)

Figure 4-3 Package Outline CS42

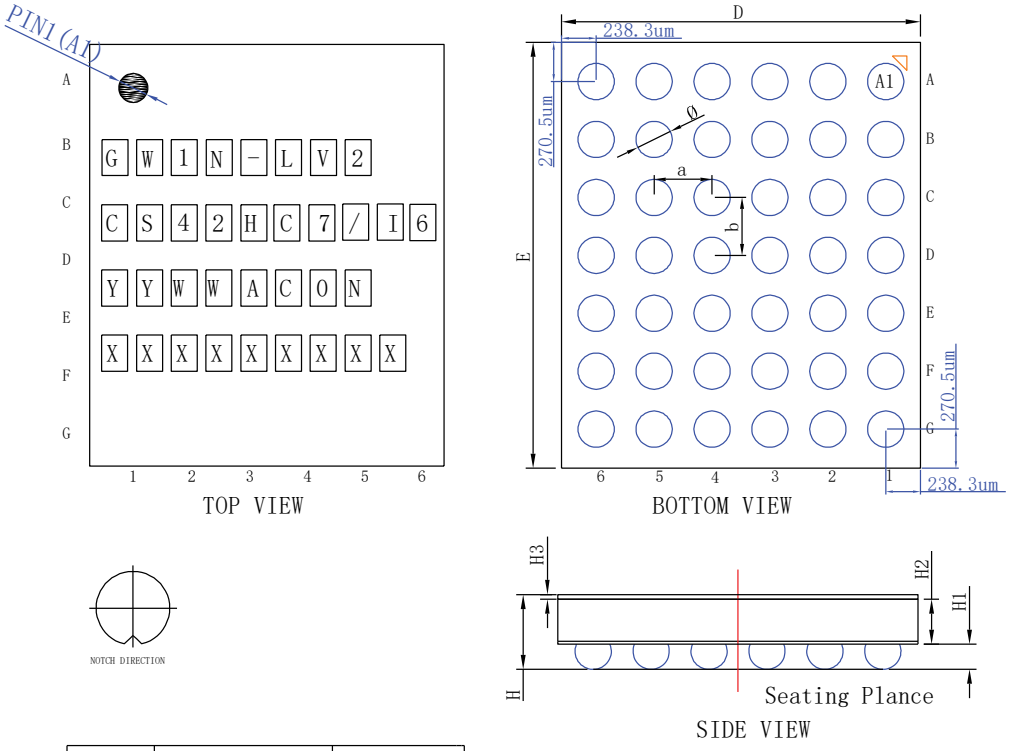


SYMBOL	ITEM	DATA(um)
D*E	PACKAGE SIZE	2446.6*2911.0 ±25
Ø	BALL DIAMETER	268 ±20
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	42
H	PACKAGE HEIGHT	542 ±41
H1	BALL HEIGHT	194 ±20
H2	SI THICKNESS+PI+UBM	323 ±16
H3	BACK COATING	25 ±5



4.4 CS42H Package Outline (2.4mm x 2.9mm)

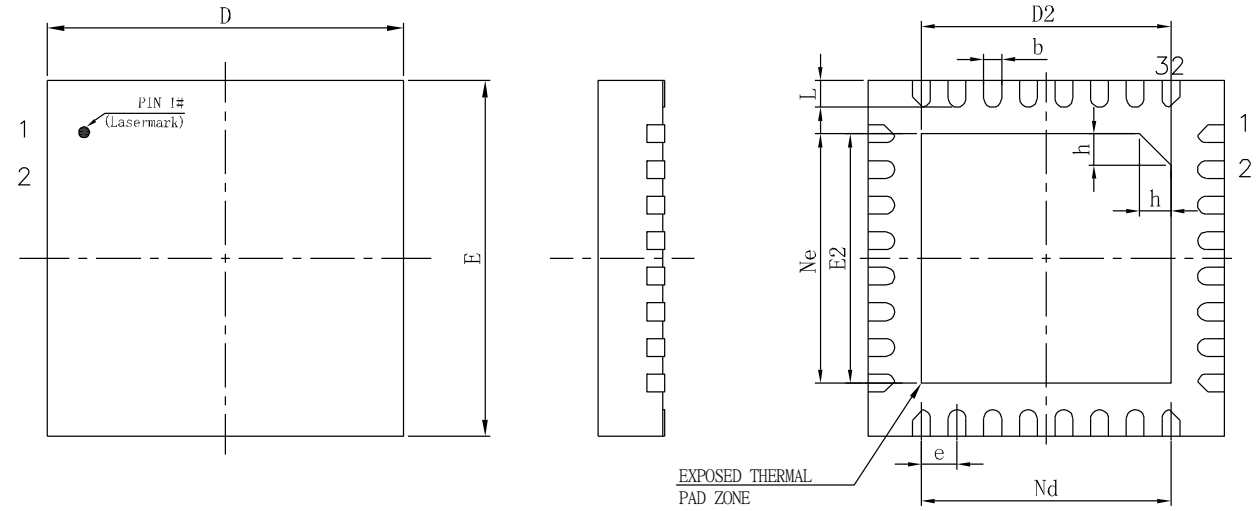
Figure 4-4 Package Outline CS42H

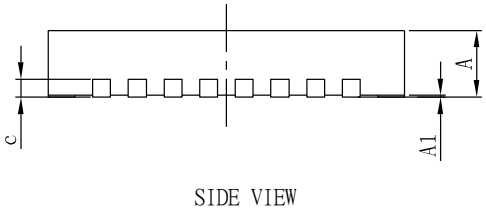


SYMBOL	ITEM	DATA(um)
D*E	PACKAGE SIZE	2476.6*2941.0±20
Ø	BALL DIAMETER	268 ±20
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	42
H	PACKAGE HEIGHT	542 ±41
H1	BALL HEIGHT	194 ±20
H2	SI THICKNESS+PI+UBM	323 ±16
H3	BACK COATING	25 ±5

4.5 FN32 Package Outline (4mm x 4mm)

Figure 4-5 Package Outline FN32 (GW1N-1S)

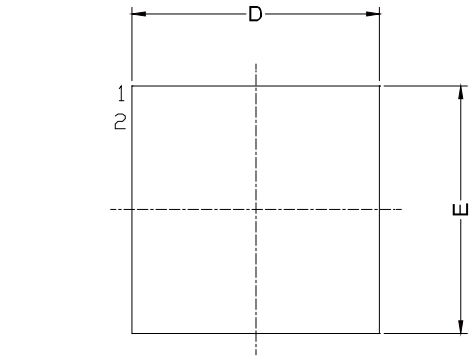




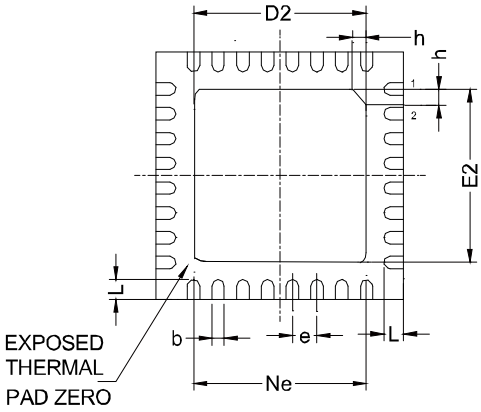
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122X122		

4.6 QN32 Package Outline (5mm x 5mm)

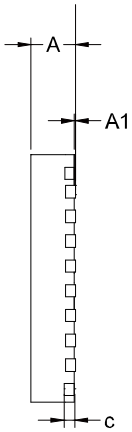
Figure 4-6 Package Outline QN32



TOP VIEW



BOTTOM VIEW



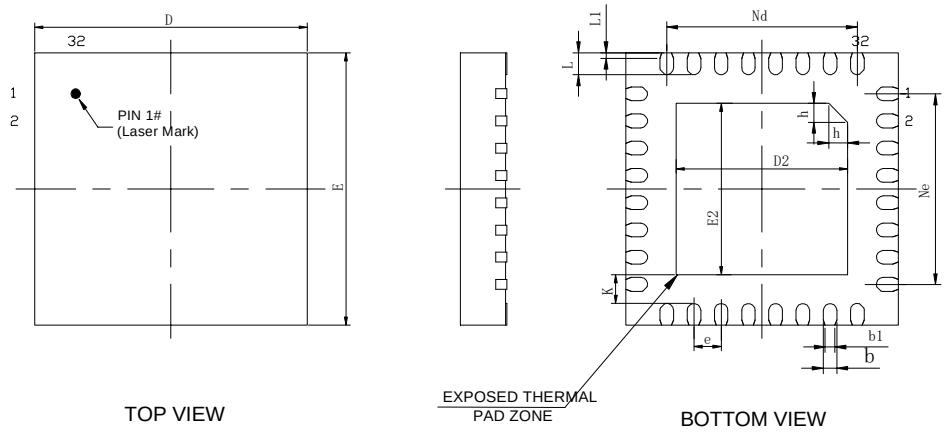
SIDE VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50 bsc		
Ne	3.50 bsc		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F 载体尺寸		150x150	130x130

4.7 QN32X Package Outline (5mm x 5mm)

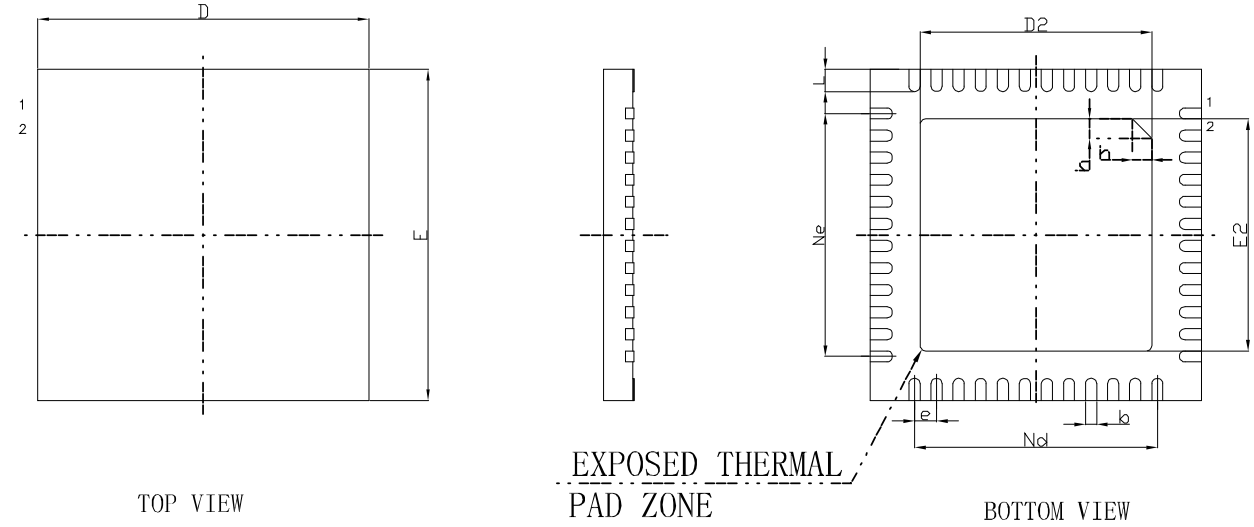
Figure 4-7 Package Outline QN32X

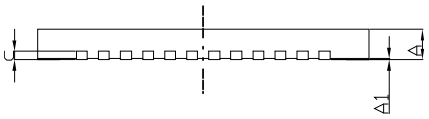


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
e	0.50BSC		
Nd	3.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.05	3.15	3.25
L	0.35	0.40	0.45
L1	0.10REF		
h	0.30	0.35	0.40
K	0.525REF		

4.8 QN48/QN48F/QN48H Package Outline (6mm x 6mm)

Figure 4-8 Package Outline QN48/QN48F/QN48H

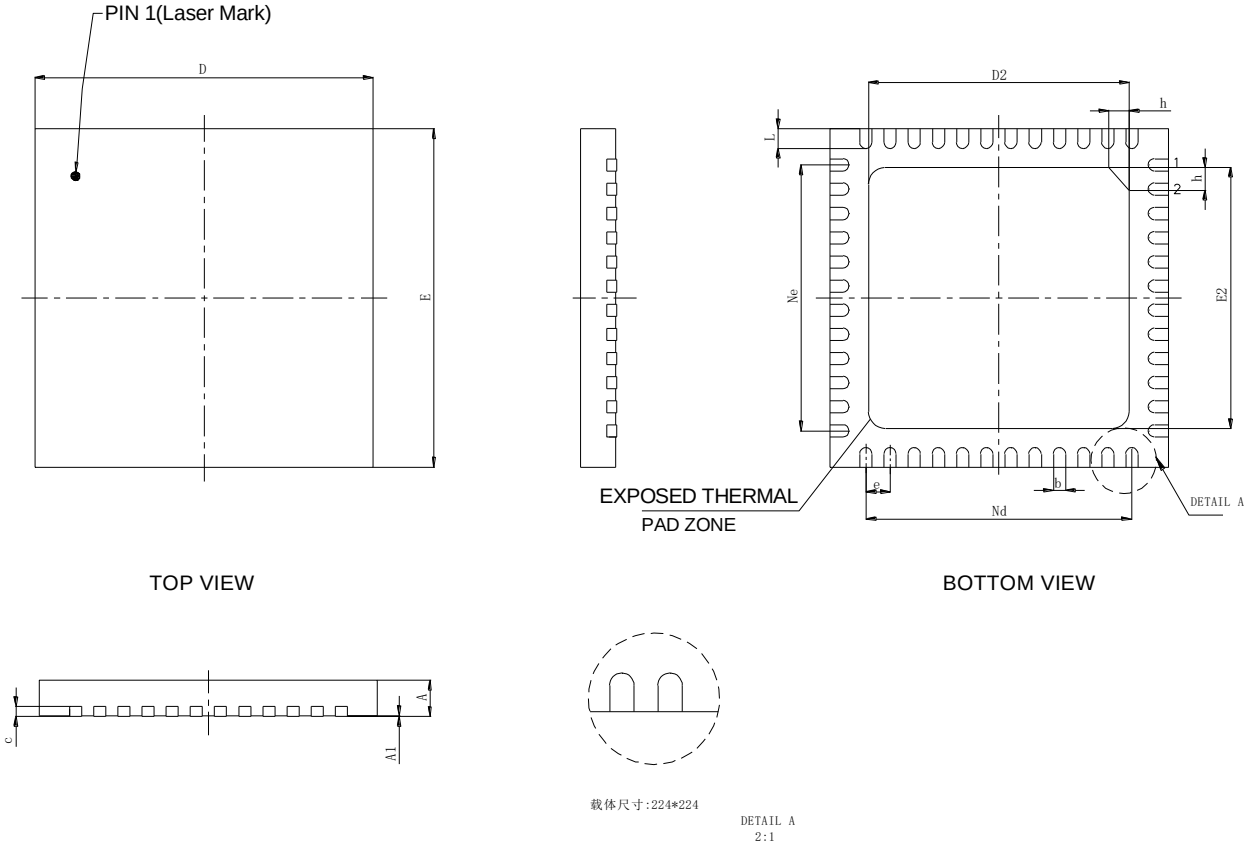




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		

4.9 FN48X Package Outline (7mm x 7mm)

Figure 4-9 Package Outline FN48X

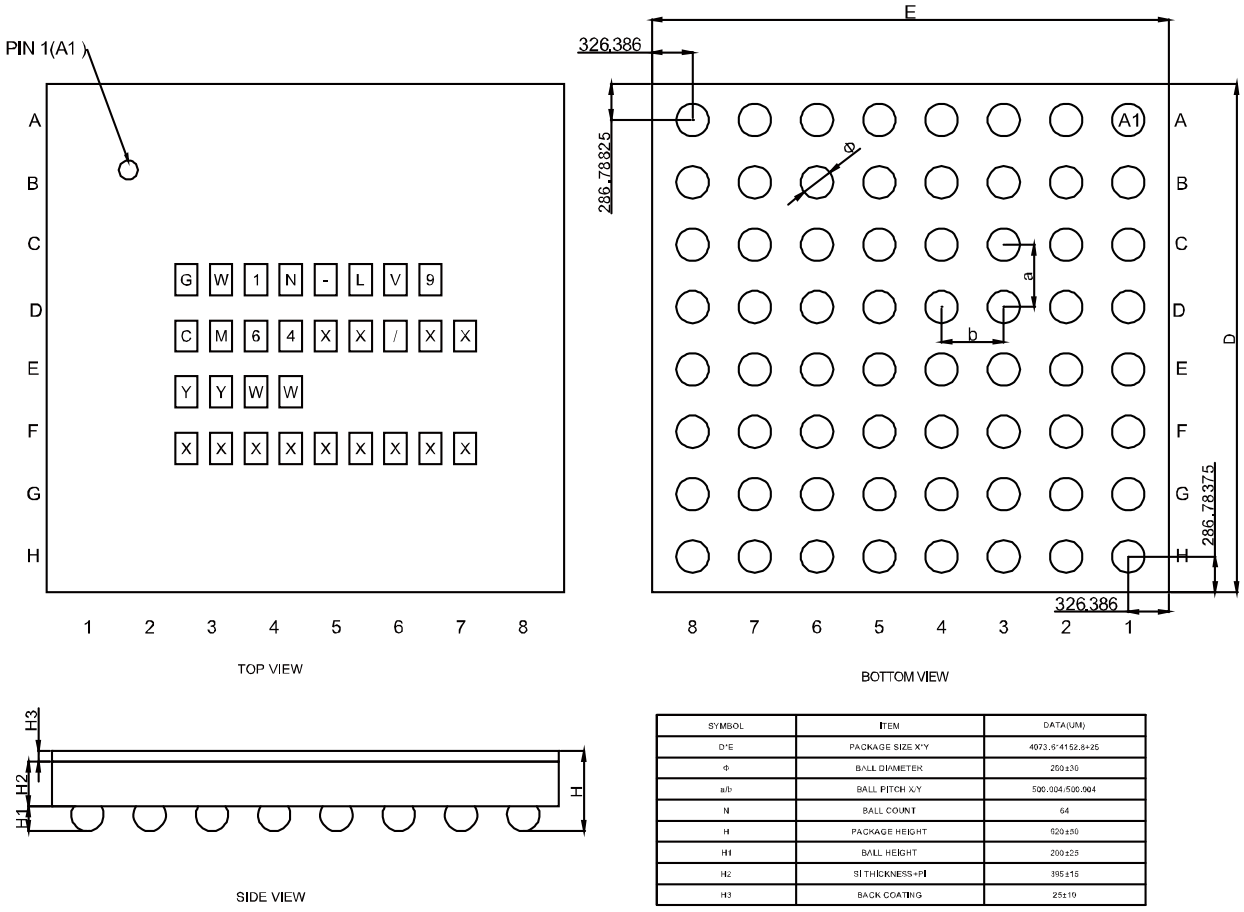


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.23
D	6.90	7.00	7.10
D2	5.30	5.40	5.50
e	0.50BSC		
Ne	5.50BSC		
Nd	5.50BSC		
E	6.90	7.00	7.10
E2	5.30	5.40	5.50
L	0.35	0.40	0.45
h	0.30	0.35	0.40

L/F载体尺寸	SYMBOL	MILLIMETER
224*224	D2	5.40±0.10
	E2	5.40±0.10

4.10 QN48/QN48F/QN48H CM64 Package Outline (4.1mm x 4.1mm)

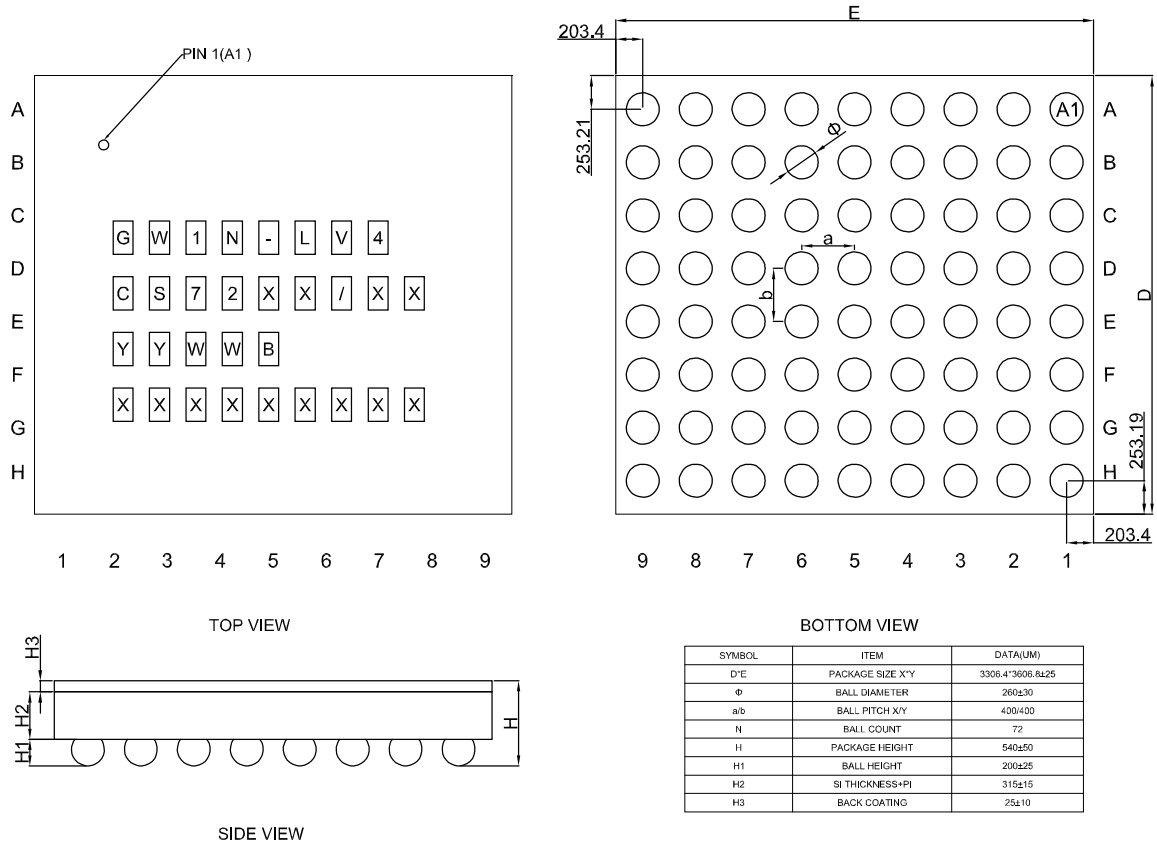
Figure 4-10 Package Outline CM64



SYMBOL	ITEM	DATA(UM)
D*E	PACKAGE SIZE X*Y	4073.6*4152.8±25
Φ	BALL DIAMETER	260±30
a/b	BALL PITCH X/Y	500.004/500.004
N	BALL COUNT	64
H	PACKAGE HEIGHT	620±30
H1	BALL HEIGHT	200±25
H2	SI THICKNESS+PI	395±15
H3	BACK COATING	25±10

4.11 CS72 Package Outline (3.6mm x 3.3mm)

Figure 4-11 Package Outline CS72



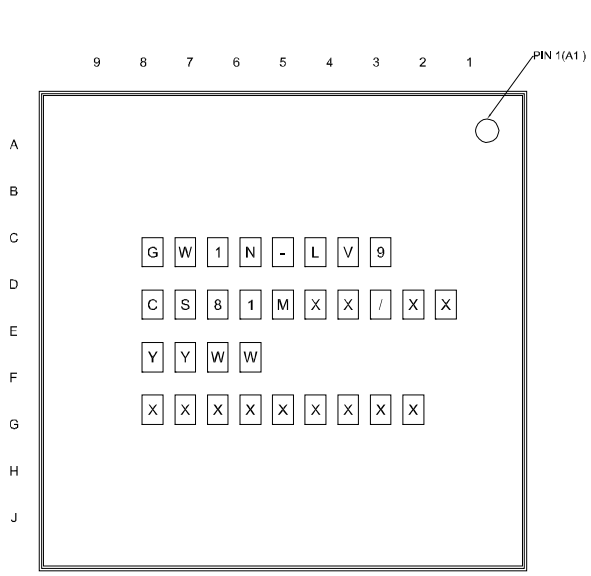
SYMBOL	ITEM	DATA(UM)
D*E	PACKAGE SIZE X*Y	3306.4*3606.8±25
Φ	BALL DIAMETER	260±30
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	72
H	PACKAGE HEIGHT	540±50
H1	BALL HEIGHT	200±25
H2	SI THICKNESS+PI	315±15
H3	BACK COATING	25±10

4.12 CS81M Package Outline (4.1mm x 4.1mm)

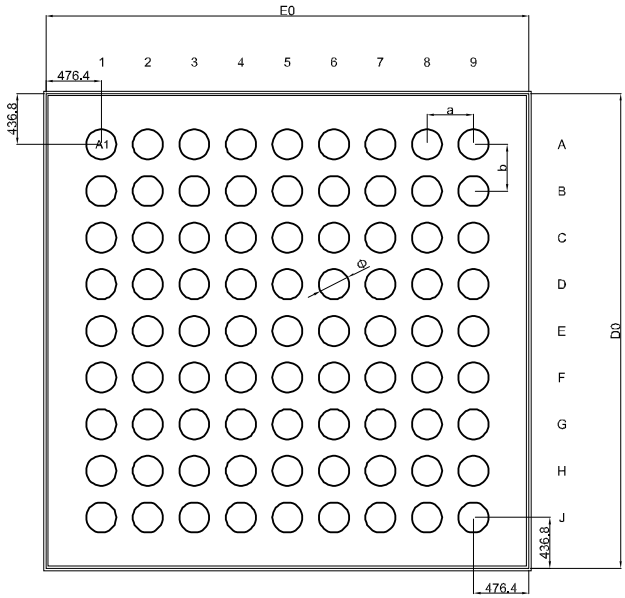
Note!

The sequence of pins 1-9 in the CS81M package outline is opposite to other WLCSP packages.

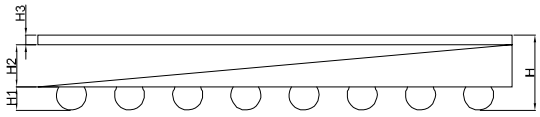
Figure 4-12 Package Outline CS81M



TOP VIEW



BOTTOM VIEW

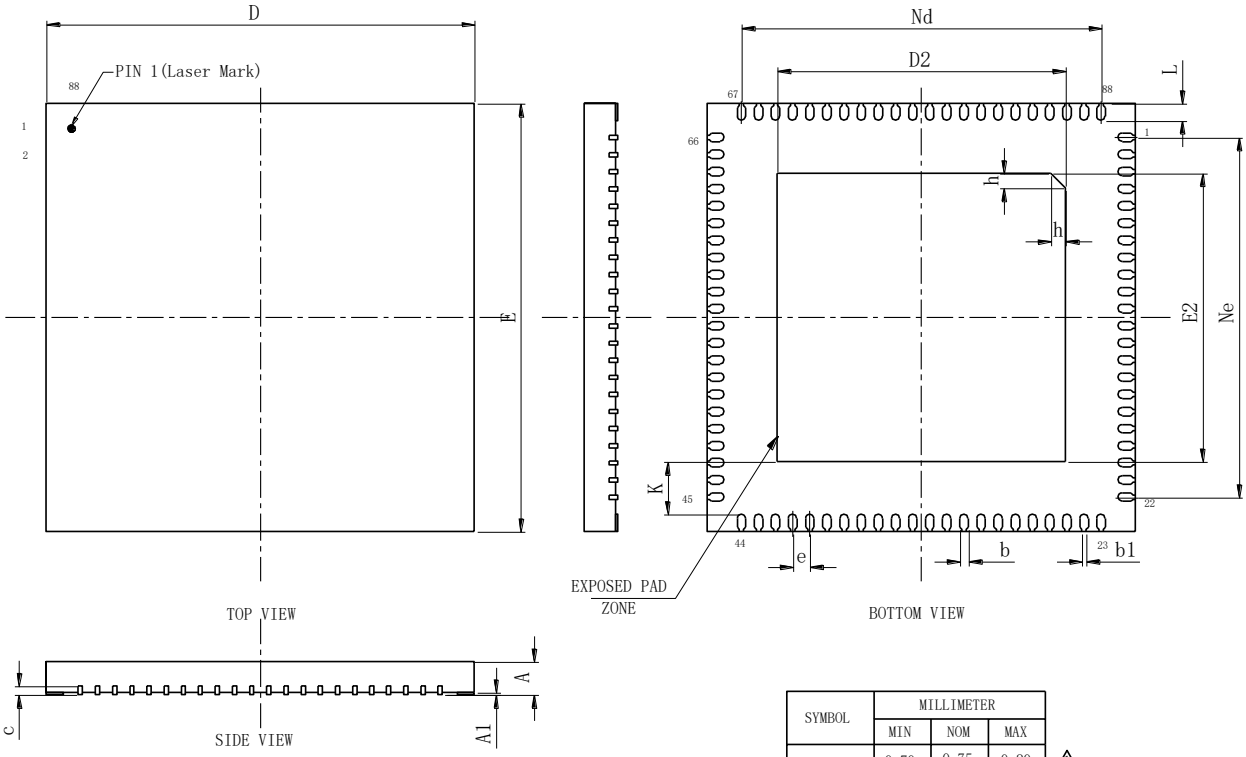


SIDE VIEW

SYMBOL	ITEM	DATA(UM)
D0*E0	PACKAGE SIZE X*Y	4073.6*4152.8±25
Φ	BALL DIAMETER	260±30
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	81
H	PACKAGE HEIGHT	540±50
H1	BALL HEIGHT	200±25
H2	SI THICKNESS+PI	315±15
H3	BACK COATING	25±10

4.13 QN88 Package Outline (10mm x 10mm)

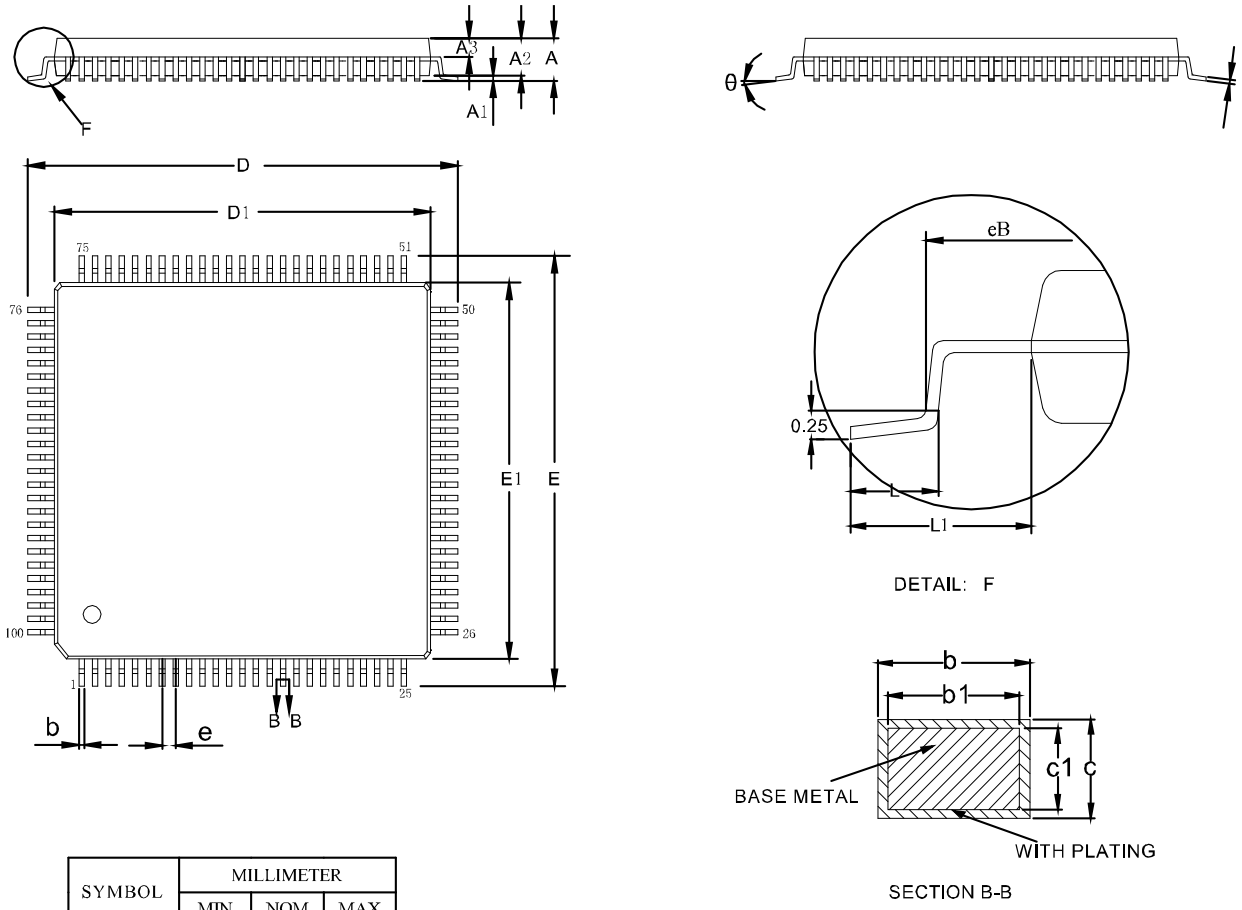
Figure 4-13 Package Outline QN88



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	⚠1
	0.80	0.85	0.90	
	0.85	0.90	0.95	⚠2
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.10REF			⚠2
c	0.18	0.20	0.25	
D	9.90	10.00	10.10	
D2	6.64	6.74	6.84	
e	0.40BSC			
Nd	8.40REF			
E	9.90	10.00	10.10	
E2	6.64	6.74	6.84	
Ne	8.40REF			
L	0.30	0.40	0.50	
K	0.20	-	-	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	300x300			

4.14 LQ100/LQ100X Package Outline (14mm x 14mm)

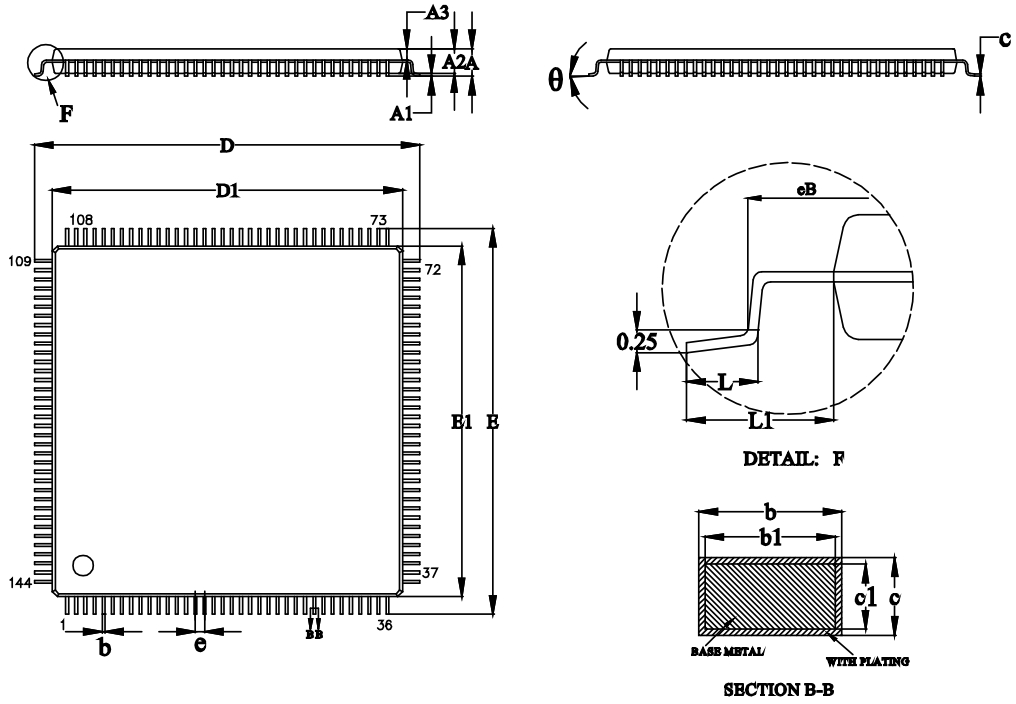
Figure 4-14 Package Outline LQ100/LQ100X



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
0	0	—	7°

4.15 LQ144/LQ144X Package Outline (20mm x 20mm)

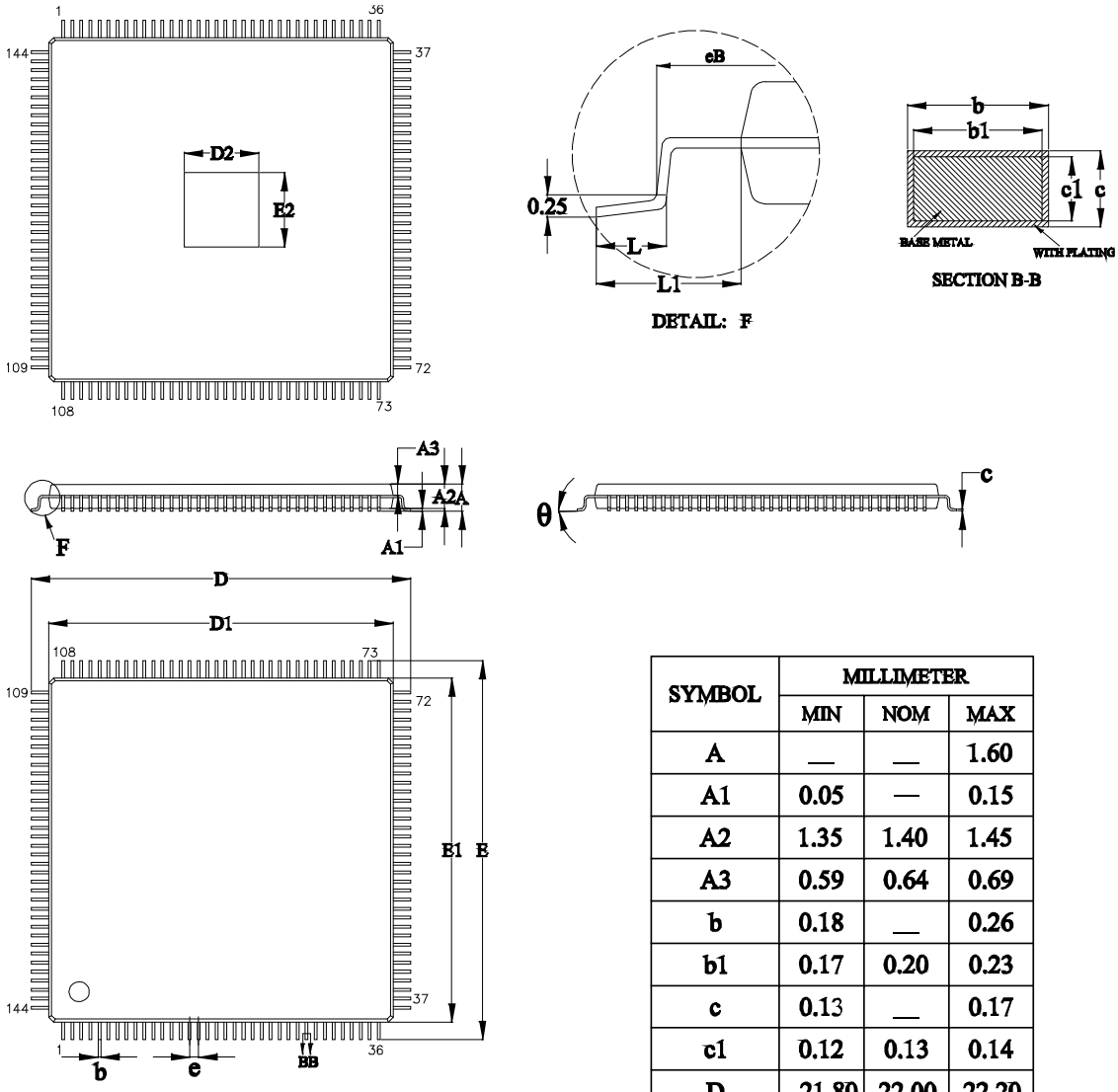
Figure 4-15 Package Outline LQ144 / LQ144X



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

4.16 EQ144 Package Outline (20mm x 20mm)

Figure 4-16 Package Outline EQ144

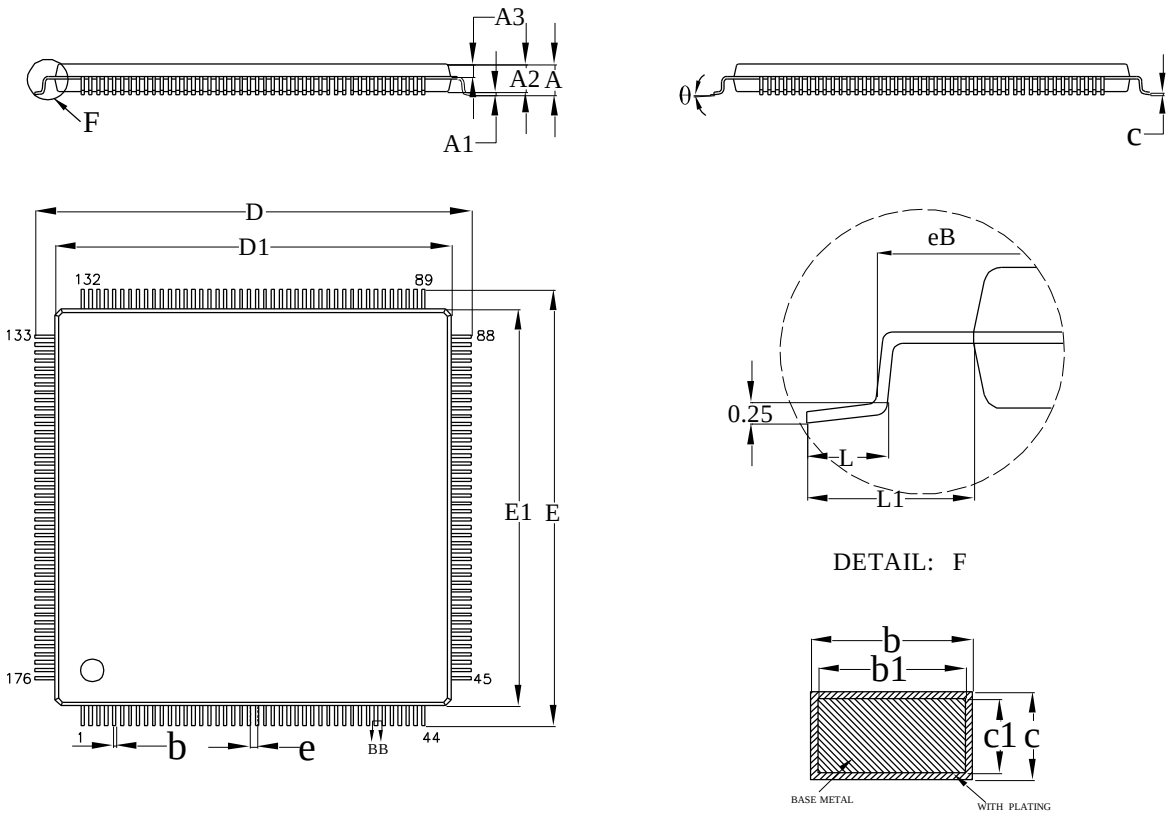


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
eB	21.15		21.40
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

L/F Size (mil) \ Size (mm)	D2	E2
218*218	5.00REF	5.00REF

4.17 LQ176 Package Outline (20mm x 20mm)

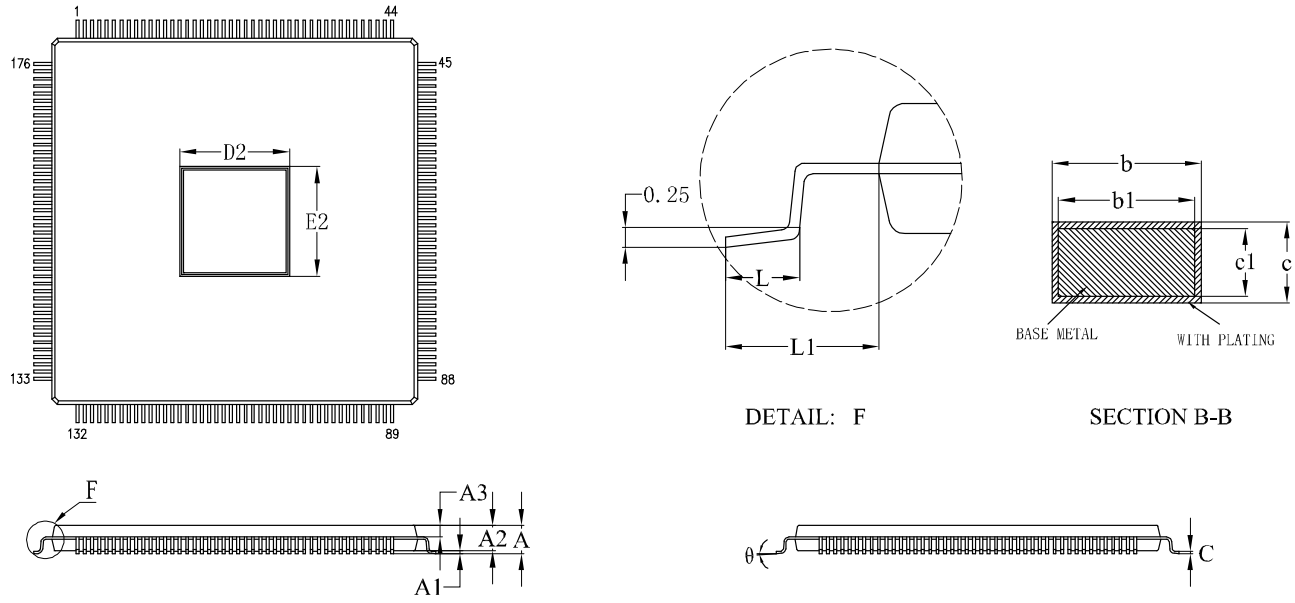
Figure 4-17 Package Outline LQ176

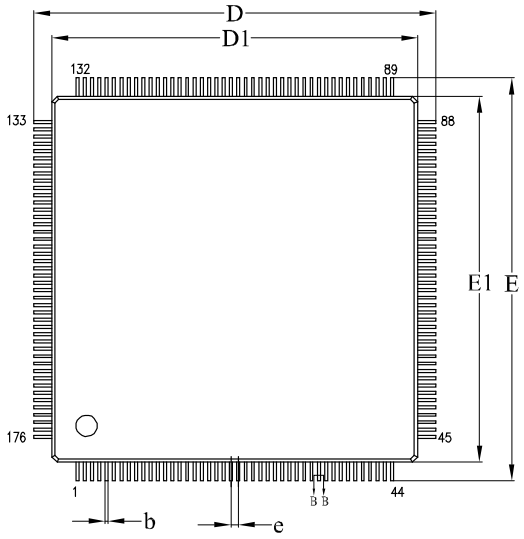


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	__	__	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	__	0.22
b1	0.13	0.16	0.19
c	0.13	__	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
eB	21.15	__	21.40
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	__	7°

4.18 EQ176 Package Outline (20mm x 20mm)

Figure 4-18 Package Outline EQ176



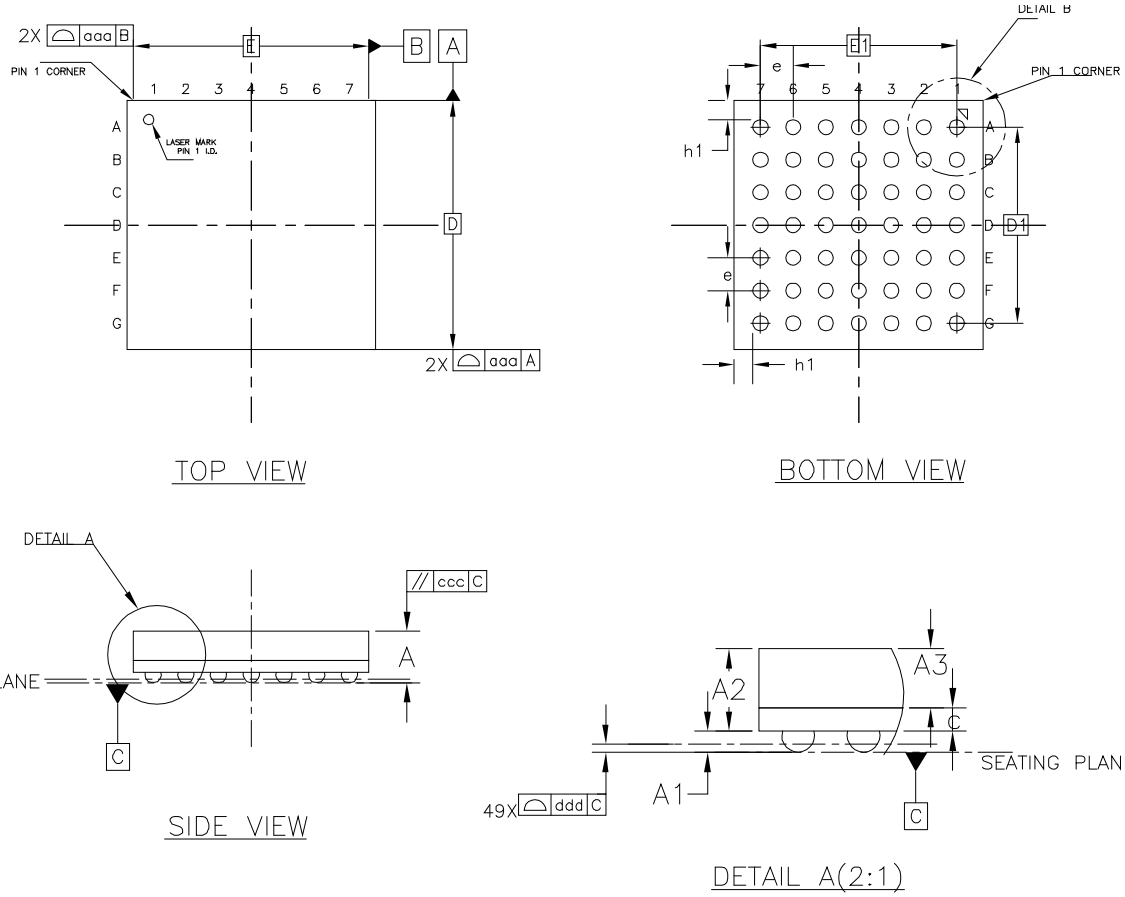


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

Size / PF Size (mil)	D2	E2
236*236	6.00REF	6.00REF

4.19 MG49 Package Outline (3.8mm x 3.8mm)

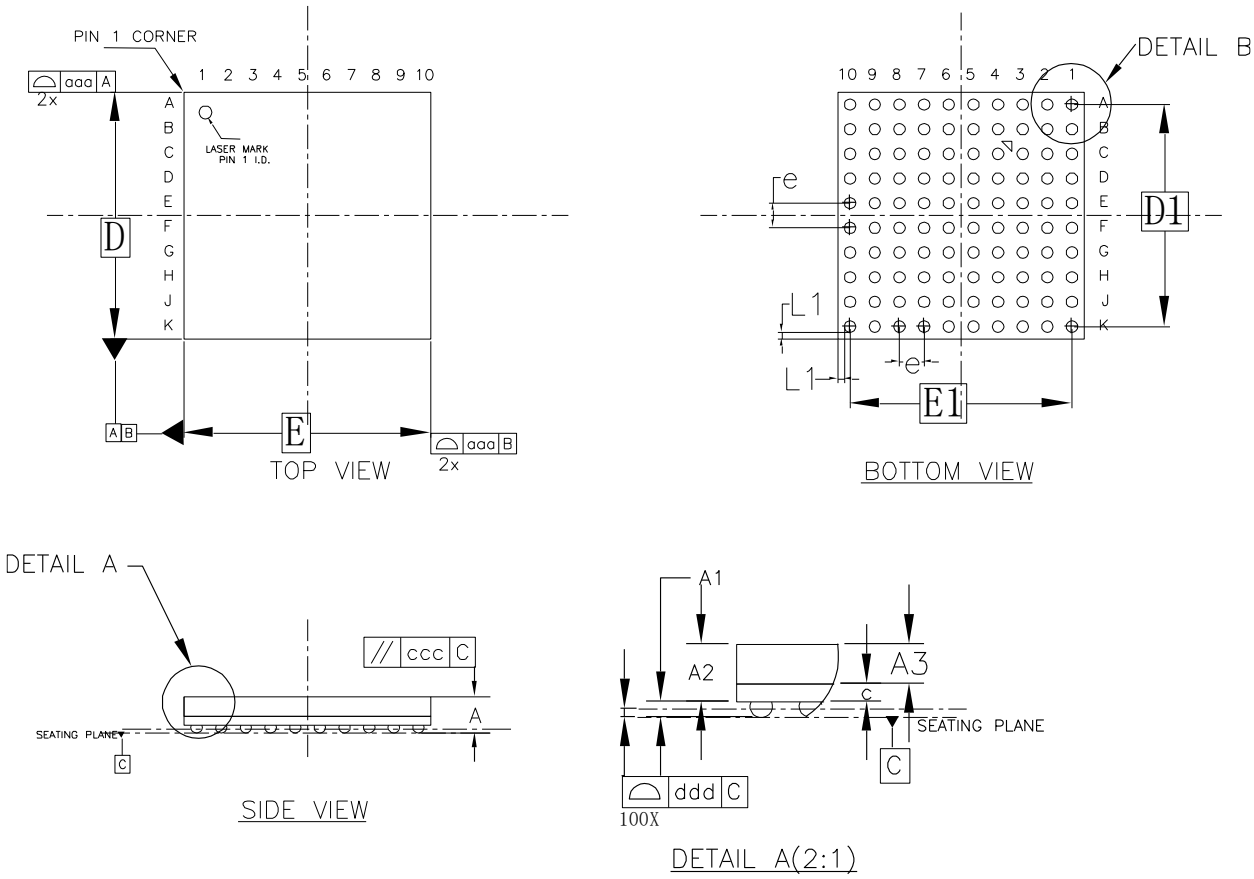
Figure 4-19 Package Outline MG49



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.71	0.79	0.87
A1	0.11	0.16	0.21
A2	0.58	0.63	0.68
A3	0.45 BASIC		
c	0.15	0.18	0.21
D	3.70	3.80	3.90
D1	3.00 BASIC		
E	3.70	3.80	3.90
E1	3.00 BASIC		
e	0.50 BASIC		
b	0.18	0.23	0.28
h1	0.285 REF		
aaa	0.10		
ccc	0.08		
ddd	0.08		
eee	0.15		
fff	0.05		

4.20 MG100/MG100T Package Outline (5mm x 5mm)

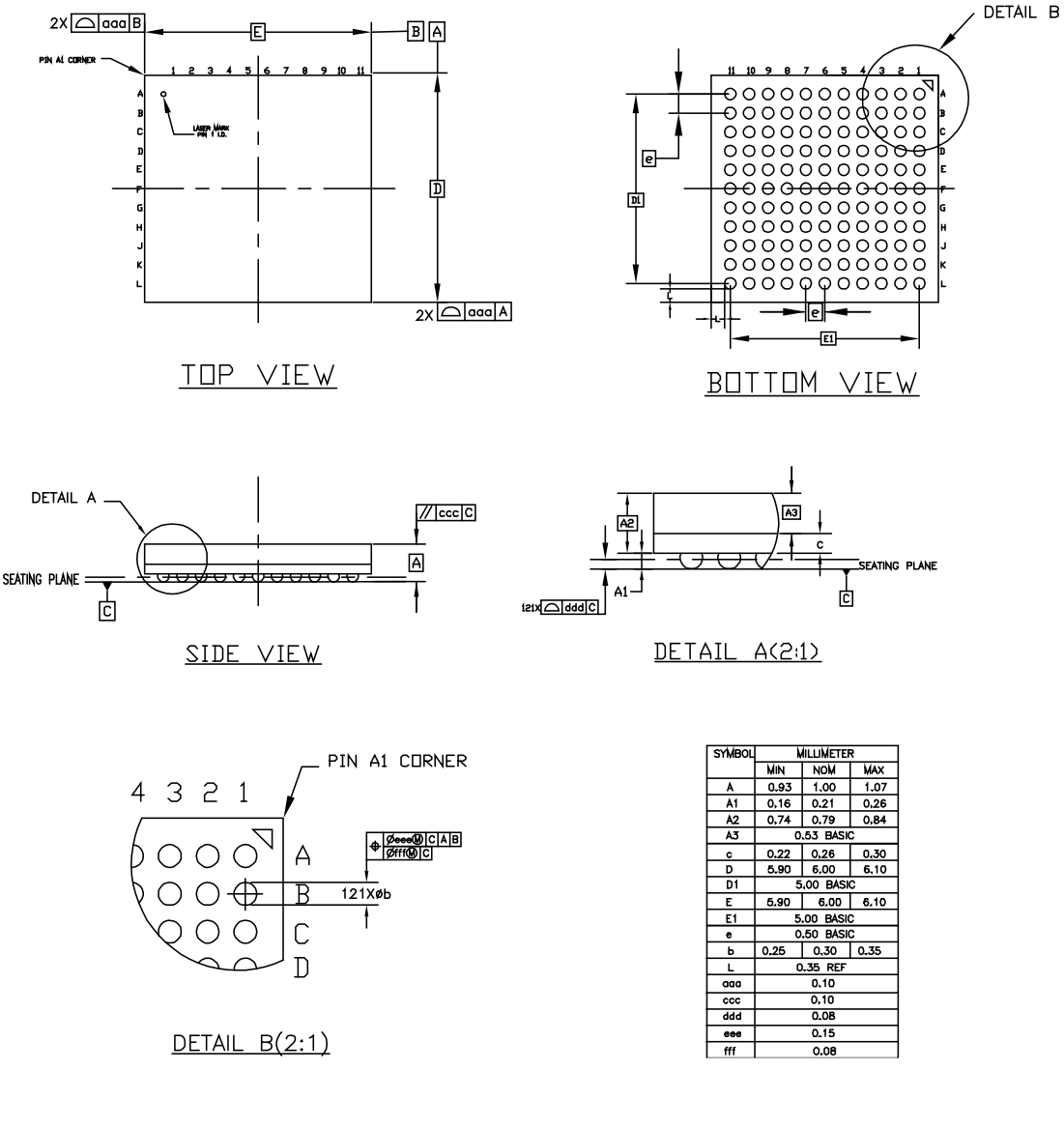
Figure 4-20 Package Outline MG100/MG100T



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.68	0.74	0.80
A1	0.11	0.16	0.21
A2	0.53	0.58	0.63
A3	0.40 BASIC		
c	0.15	0.18	0.21
D	4.90	5.00	5.10
D1	4.50 BASIC		
E	4.90	5.00	5.10
E1	4.50 BASIC		
e	0.50 BASIC		
b	0.18	0.23	0.28
L1	0.135 REF		
aaa	0.15		
ccc	0.08		
ddd	0.10		
eee	0.15		
fff	0.05		

4.21 MG121/MG121X Package Outline (6mm x 6mm)

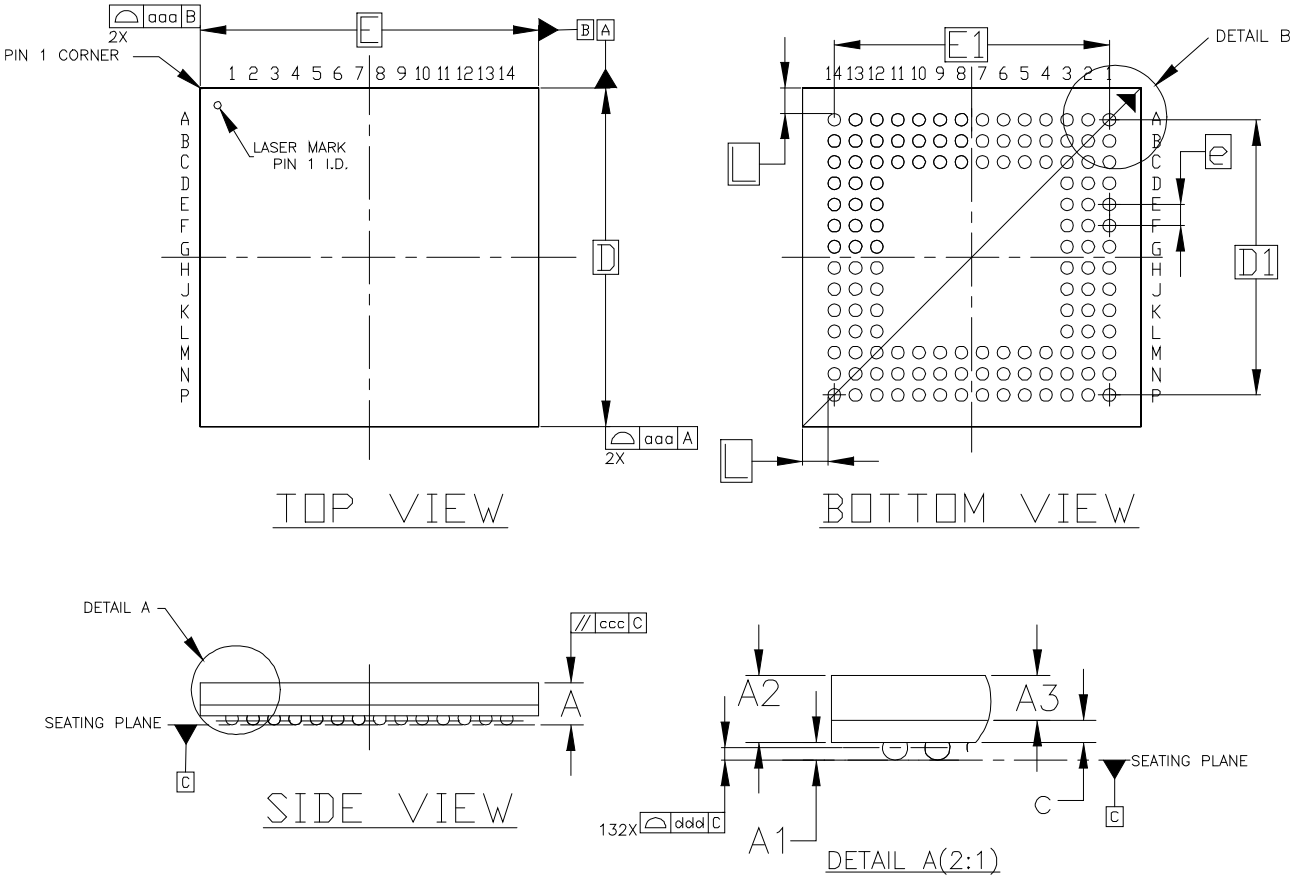
Figure 4-21 Package Outline MG121/MG121X



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.93	1.00	1.07
A1	0.16	0.21	0.26
A2	0.74	0.79	0.84
A3	0.53 BASIC		
c	0.22	0.26	0.30
D	5.90	6.00	6.10
D1	5.00 BASIC		
E	5.90	6.00	6.10
E1	5.00 BASIC		
e	0.50 BASIC		
b	0.25	0.30	0.35
L	0.35 REF		
aaa	0.10		
ccc	0.10		
ddd	0.08		
eee	0.15		
fff	0.08		

4.22 MG132/MG132X/MG132H Package Outline (8mm x 8mm)

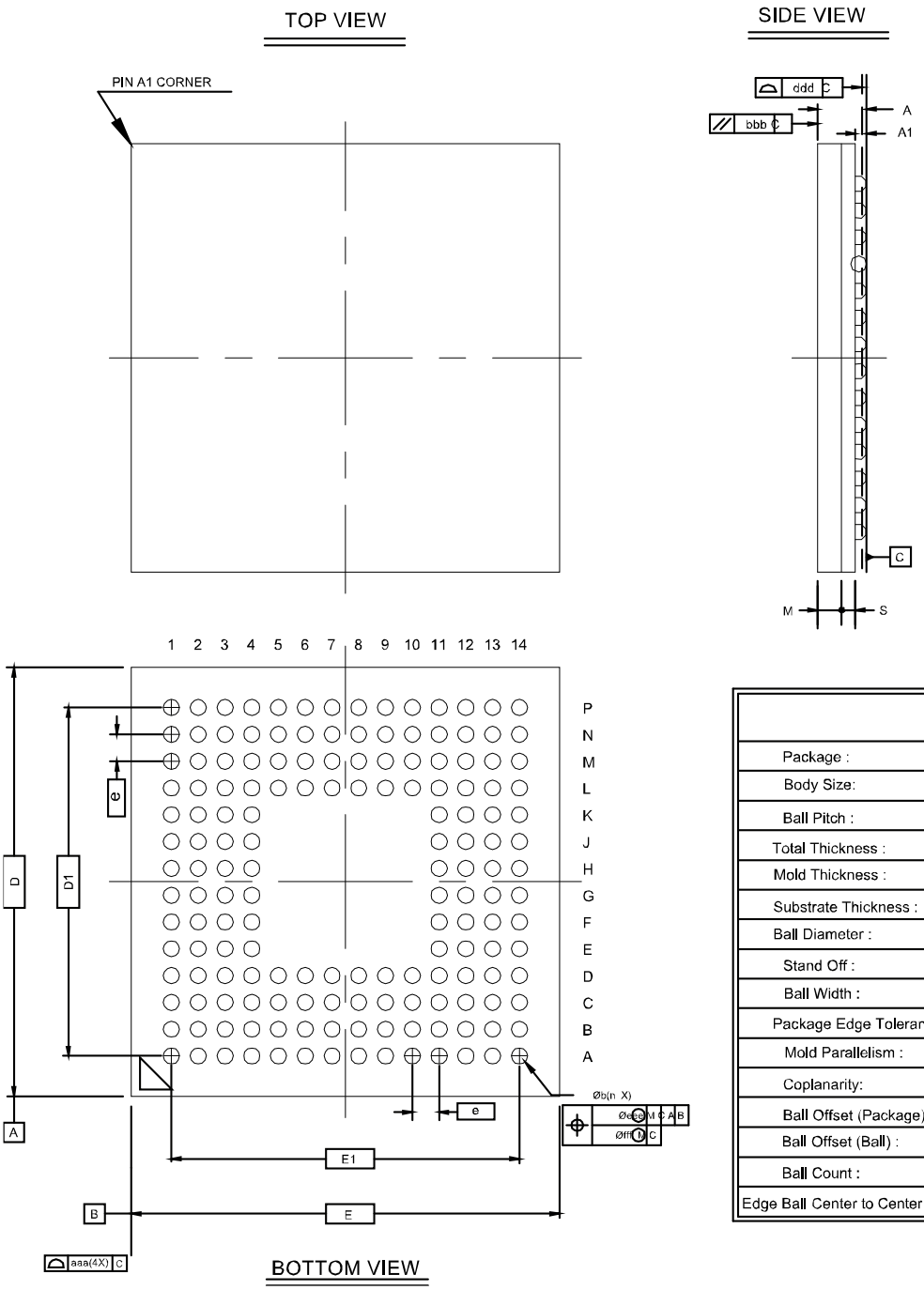
Figure 4-22 Package Outline MG132/MG132X/MG132H



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.92	1.00	1.08
A1	0.16	0.21	0.26
A2	0.74	0.79	0.84
A3		0.53 BASIC	
c	0.22	0.26	0.30
D	7.90	8.00	8.10
D1		6.50 BASIC	
E	7.90	8.00	8.10
E1		6.50 BASIC	
e		0.50 BASIC	
b	0.25	0.30	0.35
L		0.60 REF	
aaa		0.15	
ccc		0.08	
ddd		0.08	
eee		0.15	
fff		0.05	

4.23 MG160 Package Outline (8mm x 8mm)

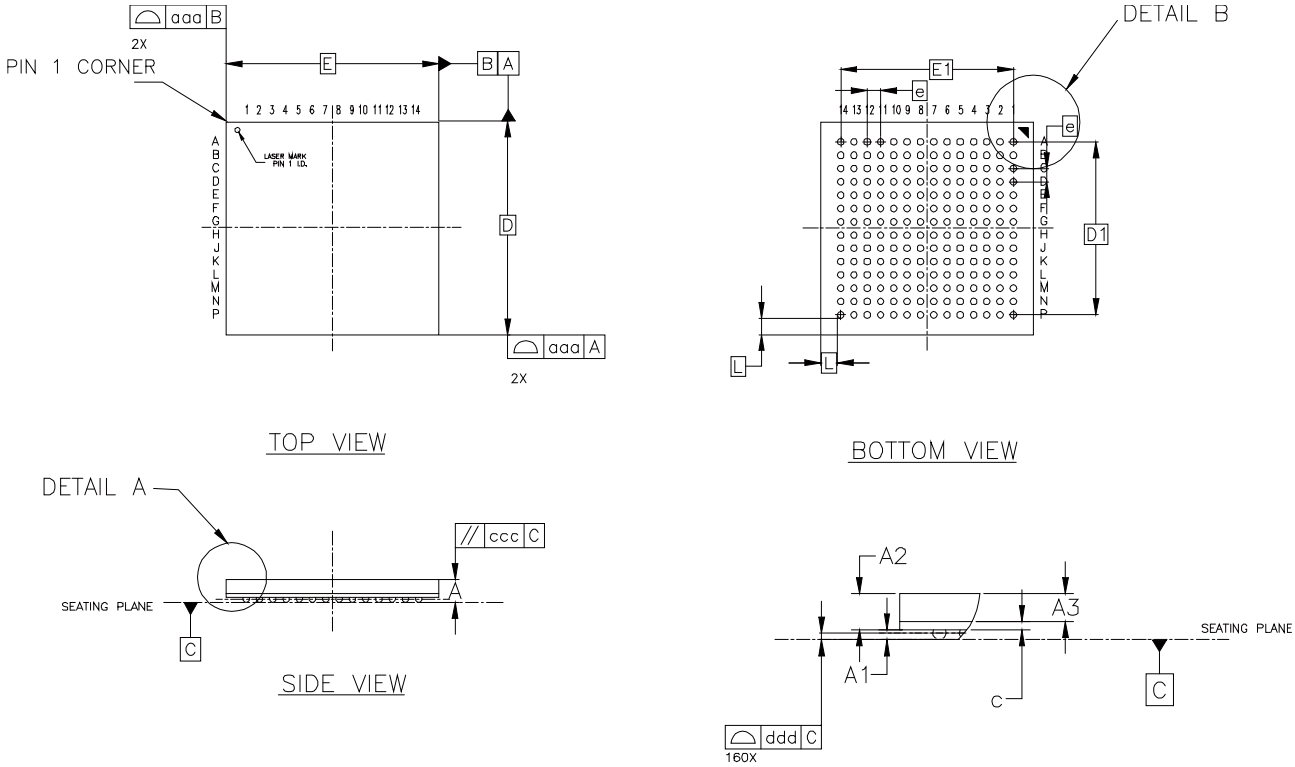
Figure 4-23 Package Outline MG160



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			MBGA		
Body Size:	X	E	8.000		
	Y	D	8.000		
Ball Pitch :		e	0.500		
Total Thickness :		A	-	-	1.000
Mold Thickness :		M	0.450 Ref.		
Substrate Thickness :		S	0.260 Ref.		
Ball Diameter :			0.300		
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	-	0.370
Package Edge Tolerance :		aaa	0.100		
Mold Parallelism :		ccc	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	160		
Edge Ball Center to Center :	X	E1	-		
	Y	D1	-		

4.24 MG196 Package Outline (8mm x 8mm)

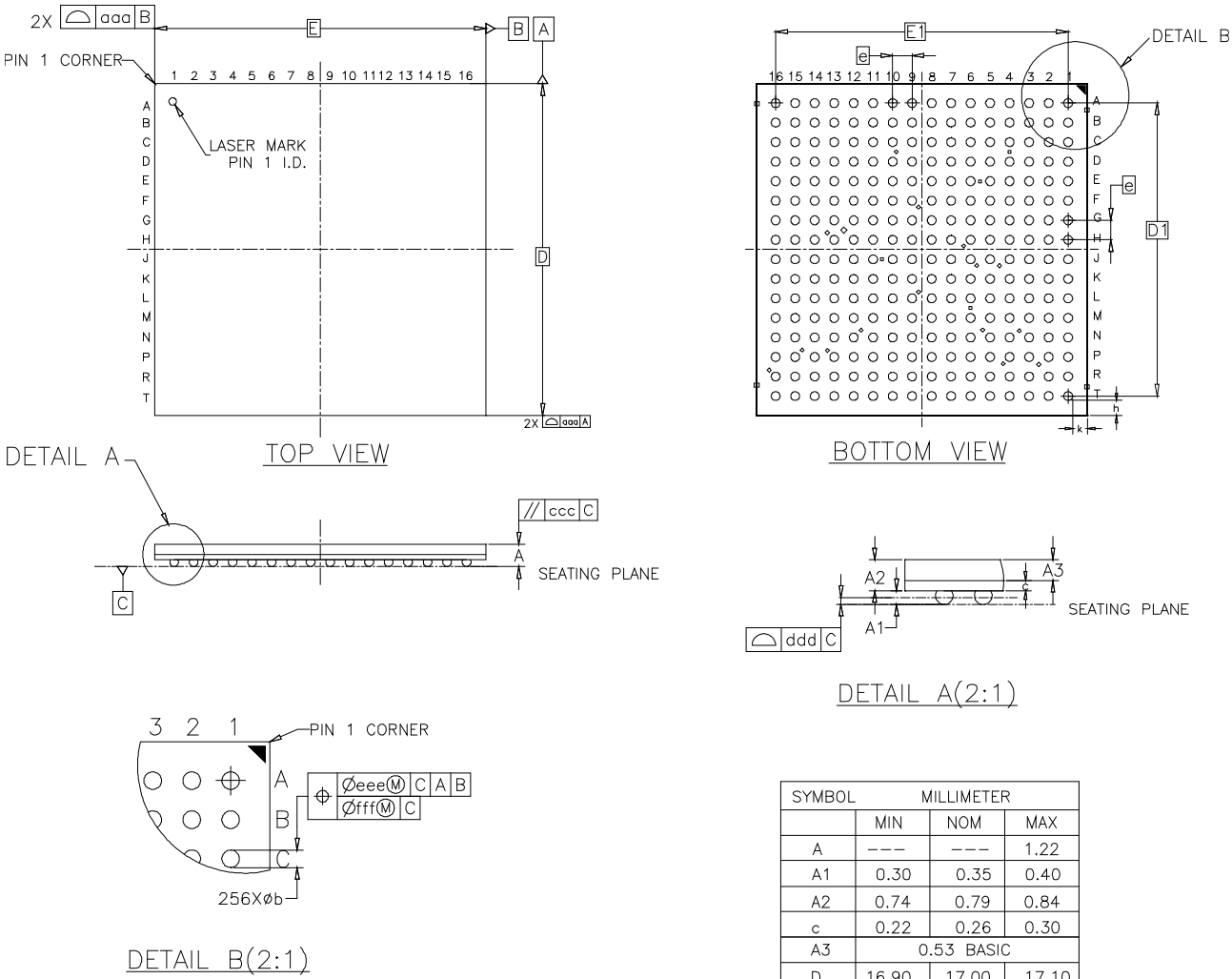
Figure 4-24 Package Outline MG196



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	0.97
A1	0.13	0.18	0.23
A2	0.64	0.69	0.74
A3	0.53 BASIC		
c	0.13	0.16	0.19
D	7.90	8.00	8.10
D1	6.50 BASIC		
E	7.90	8.00	8.10
E1	6.50 BASIC		
L	0.625 BASIC		
e	0.50 BASIC		
b	0.20	0.25	0.30
aaa	0.15		
ccc	0.15		
ddd	0.08		
eee	0.15		
fff	0.05		

4.25 PG256M Package Outline (17mm x 17mm)

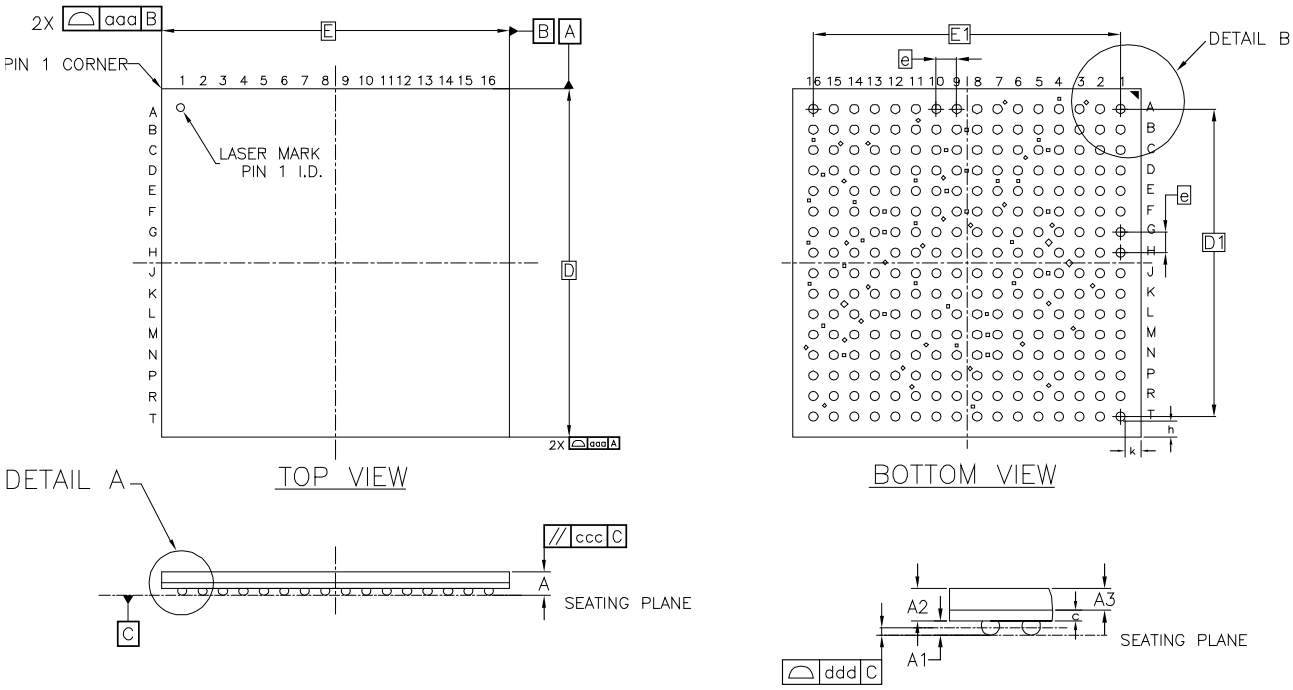
Figure 4-25 Package Outline PG256M



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3	0.53 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.40	0.45	0.50
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		
h	0.775 REF		
k	0.775 REF		

4.26 PG256 Package Outline (17mm x 17mm)

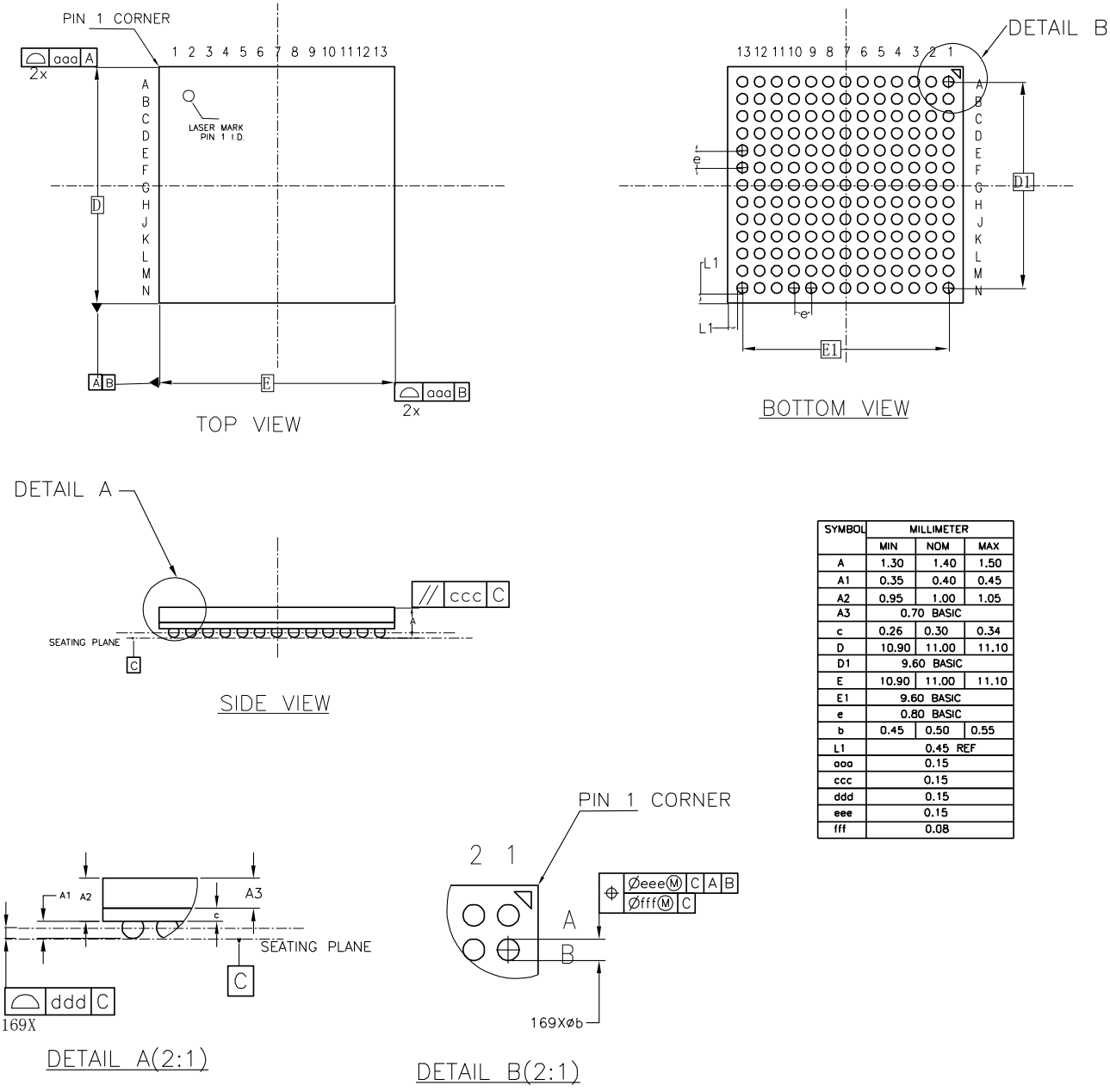
Figure 4-26 Package Outline PG256



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3	0.53 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.40	0.45	0.50
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		
h	0.775 REF		
k	0.775 REF		

4.27 UG169 Package Outline (11mm x 11mm)

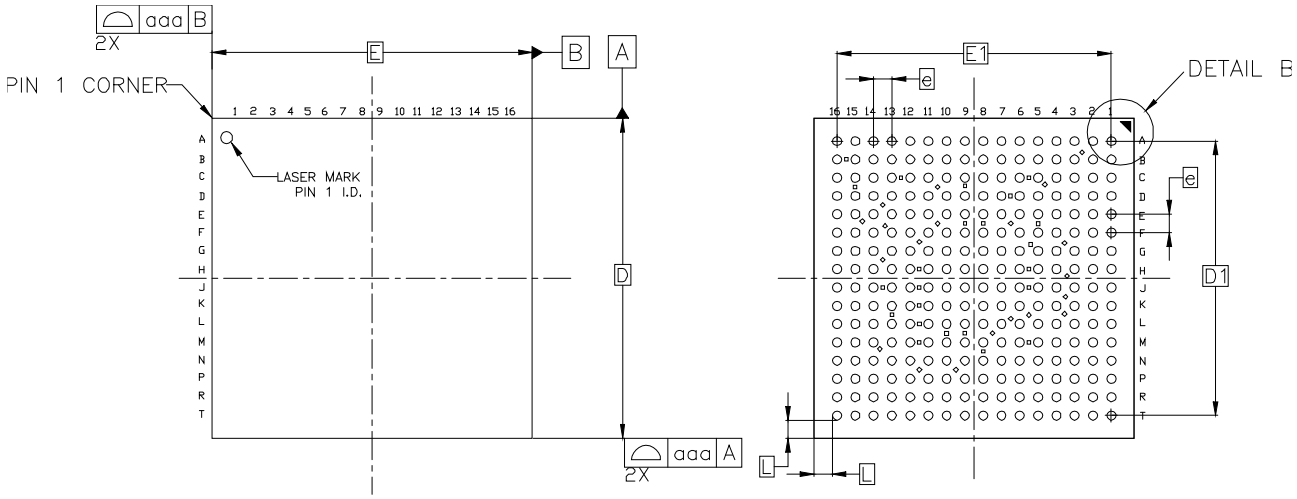
Figure 4-27 Package Outline UG169



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.30	1.40	1.50
A1	0.35	0.40	0.45
A2	0.95	1.00	1.05
A3		0.70 BASIC	
c	0.26	0.30	0.34
D	10.90	11.00	11.10
D1		9.60 BASIC	
E	10.90	11.00	11.10
E1		9.60 BASIC	
e		0.80 BASIC	
b	0.45	0.50	0.55
L1		0.45 REF	
aaa		0.15	
ccc		0.15	
ddd		0.15	
eee		0.15	
fff		0.08	

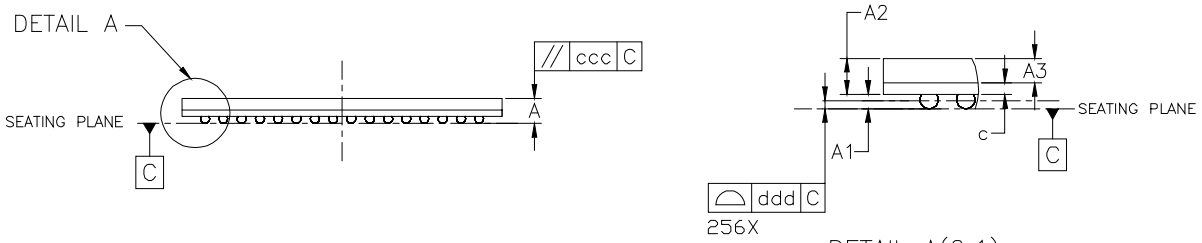
4.28 UG256 Package Outline (14mm x 14mm)

Figure 4-28 Package Outline UG256



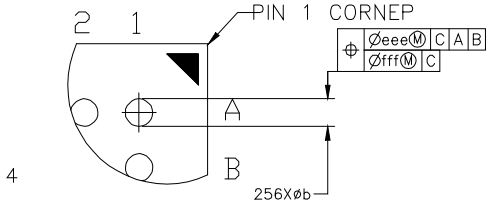
TOP VIEW

BOTTOM VIEW



SIDE VIEW

DETAIL A(2:1)

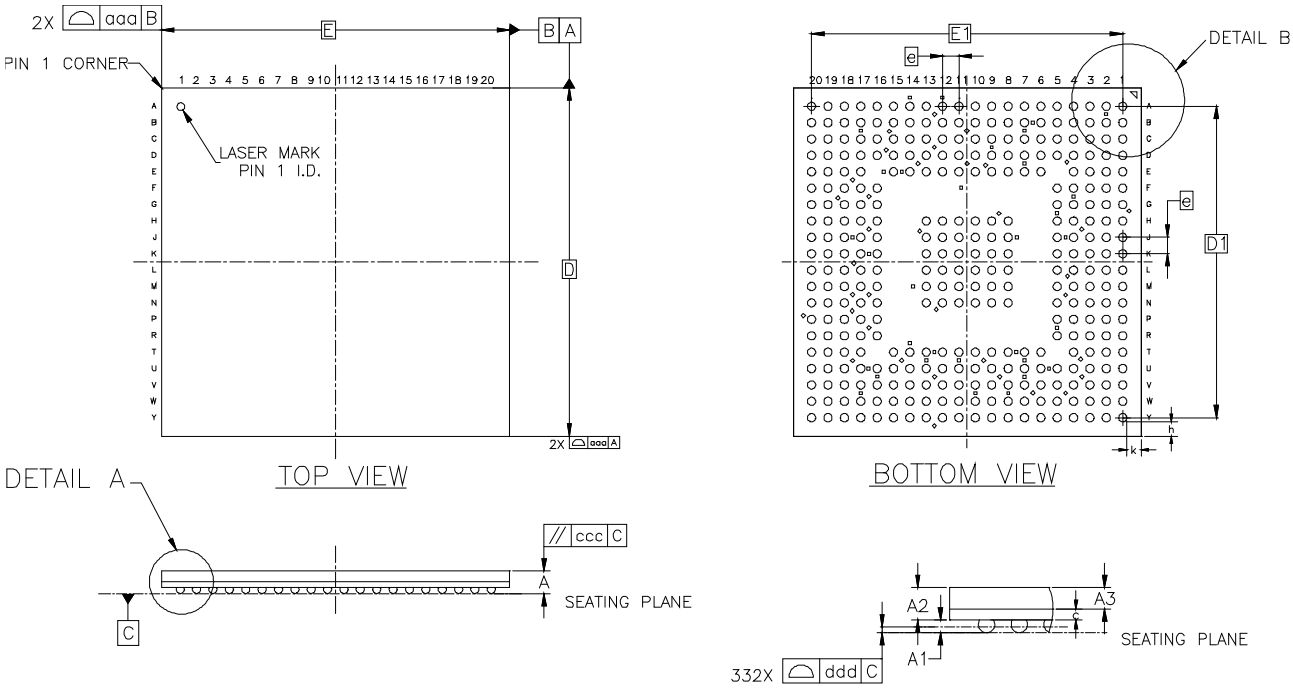


DETAIL B(3:1)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.18
A1	0.26	0.31	0.36
A2	0.74	0.79	0.84
A3	0.53 BASIC		
c	0.22	0.26	0.30
D	13.90	14.00	14.10
D1	12.00 BASIC		
E	13.90	14.00	14.10
E1	12.00 BASIC		
e	0.8 BASIC		
b	0.35	0.40	0.45
L	0.8 REF		
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		

4.29 UG332 Package Outline (17mm x 17mm)

Figure 4-29 Package Outline UG332



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.18
A1	0.26	0.31	0.36
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3	0.53 BASIC		
D	16.90	17.00	17.10
D1	15.20 BASIC		
E	16.90	17.00	17.10
E1	15.20 BASIC		
e	0.800 BASIC		
b	0.35	0.40	0.45
aaa	0.15		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.08		
h	0.700 REF		
k	0.700 REF		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