GOWIN
PROGRAMMING FOR FUTURE

GW1NSR series of FPGA Products

Datasheet

DS861-1.1E, 1/3/2019

Disclaimer

Revision History

Date	Version	Description
11/15/2018	1.0E	Initial version published.
1/3/2019	1.1 E	● The recommended working voltage list updated; ● The description about PSRAM reference manual updated.

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1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NSR series of FPGA product. It is designed to help you understand the GW1NSRseries of FPGA products quickly and select and use devices appropriately.

1.2 Supported Products

The information presented in this guide applies to the following products:

GW1NSR series of FPGA products: GW1NSR-2, GW1NSR-2C;

1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1NSR series of FPGA Products Data Sheet
2. GW1NSR series of FPGA Products Programming and Configuration User Guide
3. GW1NSR series of FPGA Products Package and Pinout
4. GW1NSR-2&2C Pinout

1.4 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
SoC	System On Chip
ARM	Advanced RISC Machines
AHB	Advanced High performance Bus
APB	Advanced Peripheral Bus
Timer	Timer
UART	Universal Asynchronous Receiver/Transmitter
NVIC	Nested Vector Interrupt Controller
DAP	Debug Access Port
Watchdog	Watchdog
TimeStamp	TimeStamp
DWT	Data Watchpoint Trace
ITM	Instrumentation Trace Module
TUIP	Trace Port Interface Unit
USB	Universal Serial Bus
PHY	Physical Layer
ADC	Analog to Digital Converter
SAR	Successive Approximation Register
SFDR	Spurious-free Dynamic Range
SINAD	Signal to Noise And Distortion
LSB	Least Significant Bit
INL	Integral Nonlinearity
DNL	Differential Nonlinearity
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block

Abbreviations and Terminology	Full Name
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
QN48	QFN48
TDM	Time Division Multiplexing

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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2General Description

The GW1NSR series of FPGA products are the first generation products in the LittleBee® family and represent one form of SIP chip.The main difference between the GW1NS series and the GW1NSR series is that the GW1NSR series integrates abundant PSRAM. The GW1NSR series includes GW1NSR-2C and GW1NSR-2. ARM Cortex-M3 hard-core processor is embedded in the GW1NSR-2C device. In addition, the GW1NSR series of FPGA products are also embedded with USB2.0 PHY, user flash, and ADC. When the ARM Cortex-M3 hard-core processor is employed as the core of GW1NSR-2C, the needs of the Min. memory can be met. FPGA logic resources and other embedded resources can flexibly facilitate the peripheral control functions, which provide excellent calculation functions and exceptional system response interrupts. They also offer high performance, low power consumption, flexible usage, instant start-up, affordability, nonvolatile, high security, and abundant package types, among other benefits. GW1NSR-2C achieves seamless connection between programmable logic devices and embedded processors. They are compatible with multiple peripheral device standards and can, therefore, reduce costs of operation and be widely deployed in industrial control, communication, Internet of Things, servo drive, consumption fields, etc.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NSR series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- Lower power consumption
  - 55nm embedded flash technology
  - Core voltage: 1.2V
  - Support LX and UX
  - Clock dynamically turns on and off
- Integrate PSRAM system in package chip
- Hard core processor
  - Cortex-M3 32-bit RISC
  - ARM3v7M architecture optimized for small-footprint embedded

applications
  - System timer (SysTick), providing a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism
  - Thumb compatible Thumb-2-only instruction set processor core for high code density
  - Up to 60 MHz operation
  - Hardware-division and single-cycle-multiplication
  - Integrated nested vectored interrupt controller (NVIC) providing deterministic interrupt handling
  - 26 interrupts with eight priority levels
  - Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
  - Unaligned data access, enabling data to be efficiently packed into memory
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Timer0 and Timer1
  - UART0 and UART1
  - Watchdog
  - Debug port: JTAG and TPIU
- USB2.0 PHY
  - 480Mbps data speed, compatible with USB1.1 1.5/12Mbps data speed
  - Plug and play
  - Hot socket
- ADC
  - Eight channels
  - 12-bit SAR AD conversion
  - Slew Rate: 1MHz
  - Dynamic range: >81 dB SFDR，>62 db SINAD
  - Linear performance: INL<1 LSB, DNL<0.5 LSB, no missing codes
- User Flash
  - 1Mb storage space
  - 32-bit data width
- Multiple I/O Standards
  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE
  - MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA,etc. drive options
  - Slew Rate option
  - Output drive strength option
  - Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
  - Hot Socket
  - BANK0 supports MIPI input
  - BANK2 supports MIPI output
  - BANK0 and BANK2 support I3C

- Abundant Slices
  - Four input LUT (LUT4)
  - Double-edge flip-flops
  - Supports shifter register
- Block SRAM with multiple modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
- Flexible PLLs+DLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Supports on-chip DUAL BOOT configuration mode
  - Multiple GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1NSR-2	GW1NSR-2C
LUT4	1,728	1,728
Flip-Flop (FF)	1,296	1,296
Block SRAM B-SRAM (bits)	72K	72K
B-SRAM quantity B-SRAM	4	4
User Flash (bits)	1M	1M
PSRAM(bits)	32M	32M
PLLs+DLLs	1+2	1+2
OSC	1, ±5% accuracy	1, ±5% accuracy
Hard core processor	-	Cortex-M3
USB PHY	USB 2.0 PHY	USB 2.0 PHY
ADC[1]	1	1
Total number of I/O banks	4	4
Max. user I/O[1]	38	38
Core voltage	1.2V	1.2V

Note!

- [1]Supports up to 8-channel ADC. For the details, please refer to Table 2-2 Package Information.
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The amount of Max. I/O in this table refers to when the loaded four pins of JTAG (TCK, TDI, TDO, and TMS) are used as I/O.

2.3 Package Information

Table 2-3 GW1NSR-2 Package Information

Internal Resources	QN48
LUT4	✓
FF	✓
B-SRAM	✓
User Flash	✓
PSRAM	✓
PLL/DLL	✓
OSC	✓
USB2.0 PHY	-
ADC[1]	8

Note!

[1] This Number refers to the number of channels supported by this package.

Table 2-4 GW1NSR-2C Package Information

Internal Resources	QN48
LUT4	✓
FF	✓
B-SRAM	✓
User Flash	✓
PSRAM	✓
Coretx-M3	✓
PLL/DLL	✓
OSC	✓
USB2.0 PHY	-
ADC[1]	8

Table 2-3 Package Information and Max. I/O

Package	Pitch(mm)	Size(mm)	GW1NSR-2	GW1NSR-2C
QN48	0.4	6 x 6	38(7)	38(7)

Note!

- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O; See *GW1NSR series of FPGA Products Package and Pinout User Guide* for more details.
- The package types in this data sheet are written with abbreviations. See 5.1Part Name.
- Please refer to GW1NSR-2&2C Pinout.

3 Architecture

3.1 Architecture Overview

Figure 3-1 GW1NSR-2 Architecture Overview

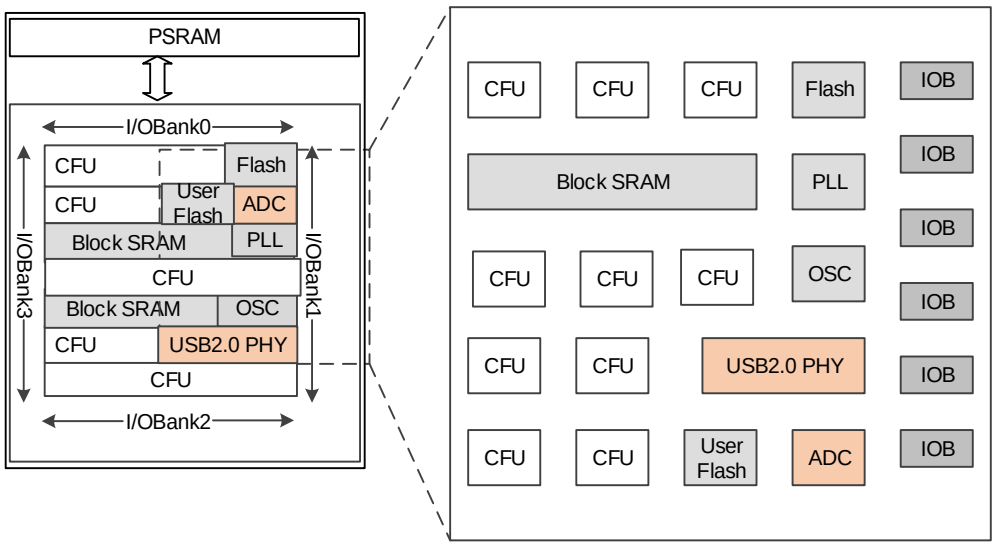
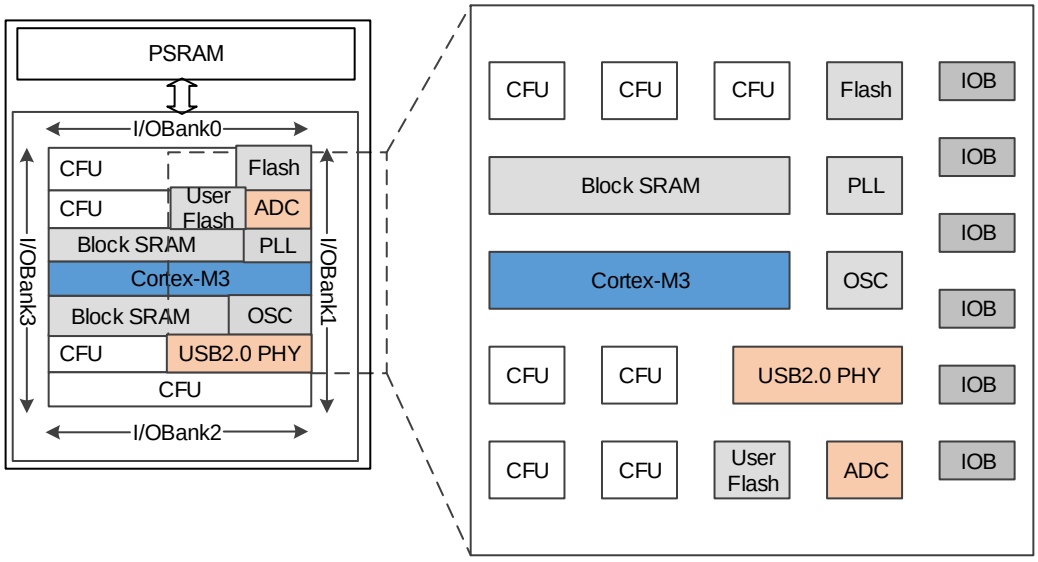


Figure 3-2 GW1NSR-2C Architecture Overview



GW1NSR is one form of SIP chip, integrated with the GW1NS series of FPGA products and PSRAM chip. For PSRAM features and overview, see3.2PSRAM.

Except for the basic units of CFU, I/O, GW1NSR series of FPGA products include B-SRAM, PLL, DLL, User Flash, on-chip oscillator, downloaded flash resources, USB2.0 PHY, and ADC. GW1NSR-2C also includes Cortex-M3, See Table 2-1 and Table 2-1 for more detailed information.

Configurable Function Unit (CFU) is the base cell for the array of the GW1NSR series of FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode and ALU mode, and Memory mode. For more detailed information, see 3.3Configurable Function Unit.

The I/O resources in the GW1NSR series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0, Bank1, Bank2, and Bank3. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. For more detailed information, see 3.4IOB.

The B-SRAM is embedded as a row in the GW1NSR series of FPGA products. In the FPGA array, each B-SRAM occupies three columns of CFU. B-SRAM has two usages; however, these cannot be employed simultaneously. One is for the Cortex-M3 processor SRAM in GW1NSR-2C devices, which is used for memory data read/write. One B-SRAM capacity is 16 Kbits, and the total capacity is 64 Kbits. One is for user SRAM in GW1NSR-2C and GW1NSR-2 devices. One B-SRAM capacity is 18 Kbits, and the total capacity is 72 Kbits. It supports multiple configuration modes and operation modes. For further details, please refer to 3.5Block SRAM (B-SRAM).

The User Flash is embedded in the GW1NSR series of FPGA products, without loss of data even if power off. It has three usages; however, these cannot be used simultaneously. One is used to storage the ARM programs of Cortex-M3 processor. In this way, the User Flash can only be read and cannot be written. One is used as the non-volatile memory resource in GW1NSR-2C and GW1NSR-2 devices. One is used for the DUAL BOOT mode of FPGA in GW1NSR-2C and GW1NSR-2 devices. See 3.6User Flash for more detailed information.

GW1NSR series of FPGA products provide one PLL and two DLLs. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each of the GW1NSR series of the FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 120MHz, providing the clock resource for the MSPI mode. It also provides clock resource for user designs with the clock precision reaching ±5%. For more detailed information, see 3.10Clock.

The Flash resources embedded in the GW1NSR series of FPGA products are used for built-in Flash programming, support instant start and

security bit operation, and support AUTO BOOT and DUAL BOOT programming modes. For more detailed information, see 4.8Configuration Interface Timing Specification.

The Cortex-M3 hard-core processor is embedded in the GW1NSR-2C device. It supports 30 MHz program loading when the system starts up and supports higher speed data/instructions transmission. The AHB expansion bus facilitates communication with external storage devices. The APB bus also facilitates communication with external devices, such as UART. GPIO interfaces are convenient for communicating with the external interfaces. FPGA can be programmed to realize controller functions across different interfaces / standards, such as SPI, I^2C, I^3C, etc. For more detailed information, see 3.7Cortex-M3.

USB2.0 PHY is embedded in the GW1NSR series of FPGA products. FPGA logics can be programmed to realize USB controllers with specific functions. For more detailed information, see 3.8USB2.0 PHY.

An ADC is embedded in the GW1NSR series of FPGA products. It is a successive-approximation ADC with eight-channel data conversion, high dynamic performance, high precision, low power consumption, and low cost. For more detailed information, see 3.9ADC.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NSR series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see 3.10Clock、3.11Long Wire (LW) and 3.12Global Set/Reset (GSR).

3.2 PSRAM

Features

- Clock frequency: 166MHz, the maximum frequency can be DDR332.
- Double Data Rate (DDR)
- Data Width: 8bits
- Read Write Data Strobe (RWDS)
- Temperature Compensated Refresh
- Partial Array Self Refresh (PASR)
- Hybrid Sleep Mode
- Deep power-down (DPD)
- Drive Strength: 35 ohms, 50 ohms, 100 ohms and 200 ohms
- Legacy wrap burst access
- 16/32/64/128 bytes burst access
- Status/Control Registers
- 1.8V power supply[1]

Note!

For the more detailed information about power supply, please refer to Table 4-2 Recommended Operating Conditions.

The supply voltage for the PSRAM interface is 1.8V; the BANK voltage that connects to the PSRAM needs to be 1.8V. For more details, please

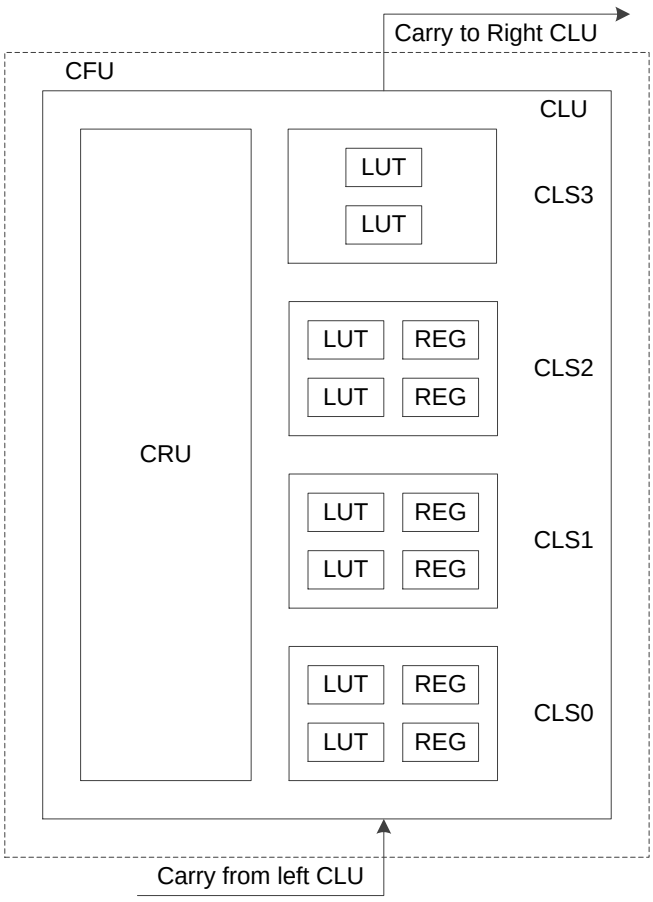
refer toTable 4-2 Recommended Operating Conditions.

The IP Core Generator in Gowin YunYuan software supports both the embedded and external PSRAM controller IP. This controller IP can be used for the PSRAM power-up, initialization, read calibration, etc., by following the controller read/write timing. For the further detailed information, please refer to *Gowin PSRAM Memory Interface IP User Guide*.

3.3 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array of the GW1NSR series of FPGA products. Each CFU consists of a configurable logic unit (CLU) and its routing resource configurable routing unit (CRU). In each CLU, there are four configurable logic slices (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-3 below.

Figure 3-3 CFU Structure



3.3.1 CLU

The CLU supports three operation modes: basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

  Each LUT can be configured as one four input LUT. A higher input

number of LUT can be formed by combining LUT4 together.

- Each CLS can form one five input LUT5.
- Two CLSs can form one six input LUT6.
- Four CLSs can form one seven input LUT7.
- Eight CLSs (two CLUs) can form one eight input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

- Adder and subtractor
- Up/down counter
- Comparator,including greater-than, less-than, and not-equal-to
- MULT

Register

Each configurable logic slice (CLS0~CLS2) has two registers (REG), as shown in Figure3-4 below.

Figure3-4 Register in CLS

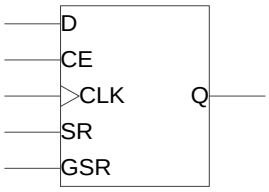


Table 3-1 Register Description in CFU

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSE[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW1NSR series of FPGA products,GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

3.3.2 CRU

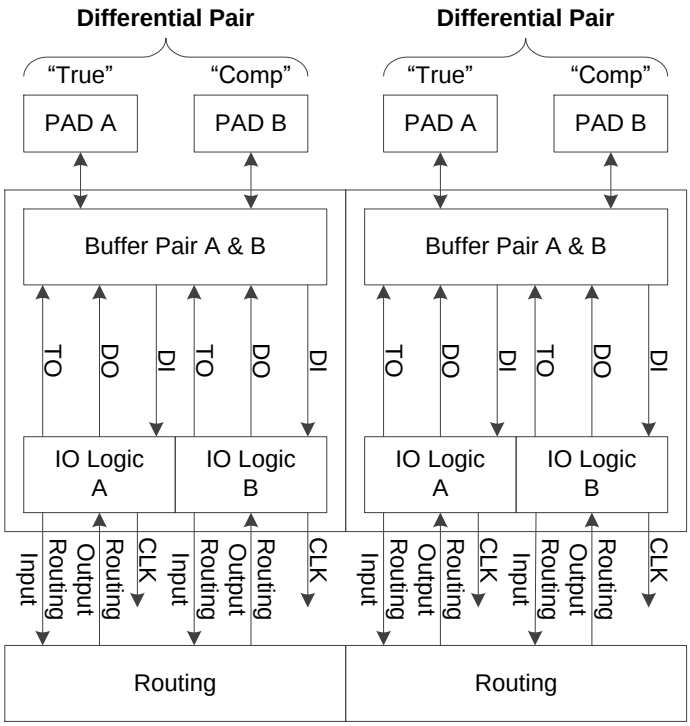
The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3.4 IOB

The IOB in the GW1NSR series of FPGA products includes IO buffer, IO logic, and its routing unit. As shown in Figure 3-5, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-end input/output.

Figure 3-5 IOB Structure View



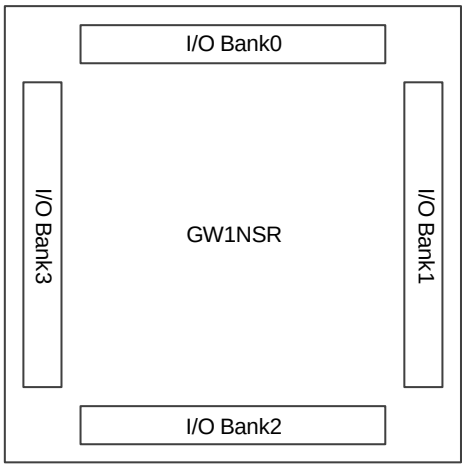
IOB Features:

- V_{CCO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode
- BANK0 supports MIPI input
- BANK2 supports MIPI output
- BANK0 and BANK2 support I3C

3.4.1 I/O Buffer

There are four IO Banks in the GW1NSR series of FPGA products, as shown in Figure 3-6. To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as referenced voltage. The user can choose from the internal reference voltage of the bank (0.5 x V_{CCO}) or the external reference voltage using any IO from the bank.

Figure 3-6 GW1NSR I/O Bank Distribution



The GW1NSR series of FPGA products support LX and UX.

The core voltage of the GW1NSR series of FPGA products is 1.2V;

LX has no linear voltage regulator, and V_{CCX} needs to be set to 1.8V. The I/O Bank voltage V_{CCO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V according to requirements.

UX has linear voltage regulator, and V_{CCX} needs to be set to 2.5 V. The I/O Bank voltage V_{CCO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V according to requirements.

Note!

- V_{CCO2} needs to be set as 1.2V for all LX and UX devices when BANK2 MIPI output is used. LX version can only reach 60% of the MIPI output speed.
- By default, the systemIO is weak pull-up for blank chips.

For the V_{CCO} requirements of different I/O standards, see Table 3-2.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVTTL33	Single end	3.3	4,8,12,16,24
LVCMOS33	Single end	3.3	4,8,12,16,24
LVCMOS25	Single end	2.5	4,8,12,16
LVCMOS18	Single end	1.8	4,8,12
LVCMOS15	Single end	1.5	4,8
LVCMOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	N/A
LVPECL33E	Differential	3.3	16
MVLDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
LVDS25	Differential	2.5/3.3	3.5/2.5/2/1.25
RSDS	Differential	2.5/3.3	2
MINILVDS	Differential	2.5/3.3	2
PPLVDS	Differential	2.5/3.3	3.5
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8

Table 3-3 Input I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single end	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No

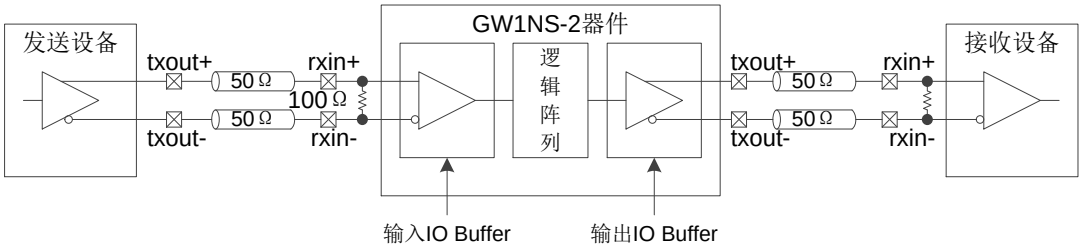
3.4.2 True LVDS Design

BANK1/2/3 in the GW1NSR devices support true LVDS output, but BANK1/2/3 do not support internal 100Ω input differential matched resistance. Bank0 supports internal 100Ω input differential matched resistance, but does not support true LVDS output. BANK0/1/2/3 support LVDS25E, MLVDS25E, BLVDS25E, etc. For more detailed information about different levels, please refer to *Gowin systemIO User Guide*.

For more detailed information about true LVDS, please refer to *GW1NSR-2&2C Pinout*.

True LVDS input I/O needs external 100Ω terminal resistance for matching. SeeFigure 3-7for the true LVDS design.

Figure 3-7 True LVDS Design



For more detailed information about LVDS25E, MLVDS25E, and BLVDS25E on IO terminal matched resistance, please refer to *Gowin SystemIO User Guide*.

3.4.3 I/O Logic

Figure 3-8 shows the I/O logic output of the GW1NSR series of FPGA products.

Figure 3-8 I/O Logic Input

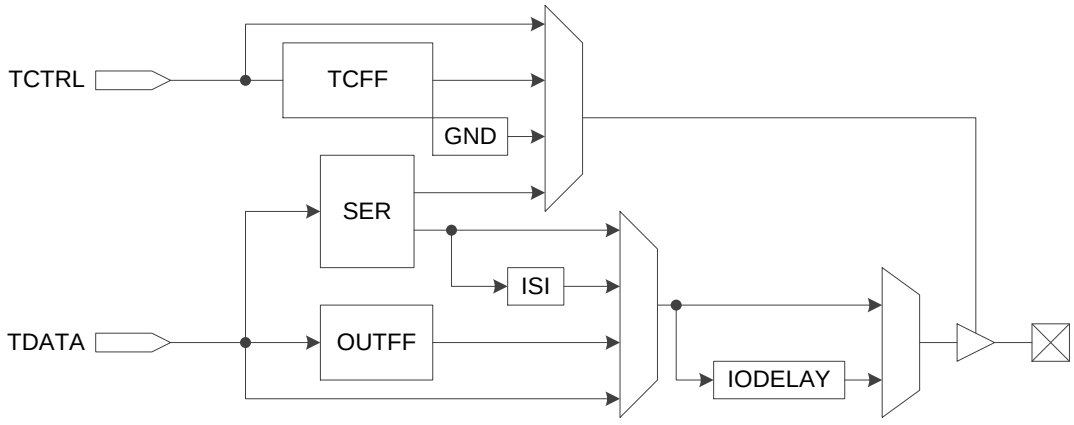
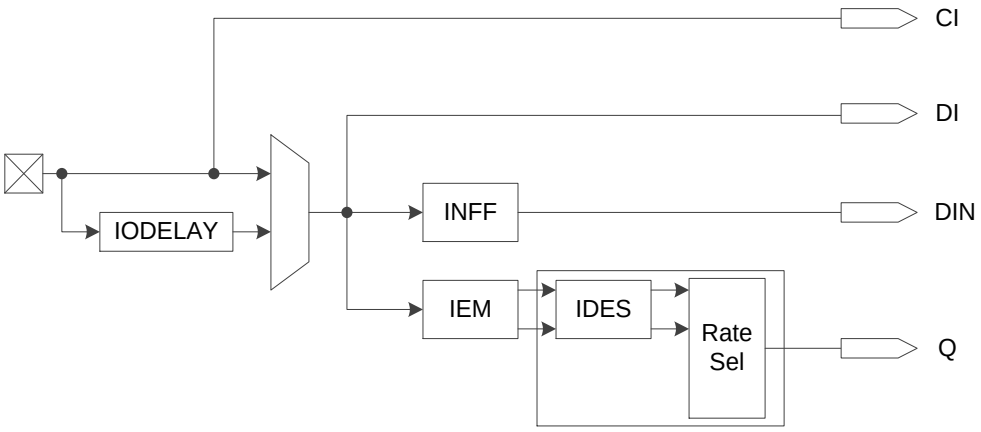


Figure 3-9 shows the I/O logic input of the GW1NSR series of FPGA products.

Figure 3-9 I/O Logic Input

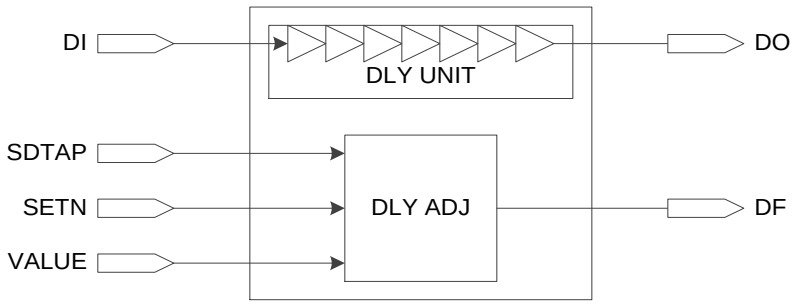


A description of the I/O logic modules of the GW1NSR series of FPGA products is presented below:

IODELAY

See Figure 3-10 for an overview of the IODELAY. Each I/O of the GW1NSR series of FPGA products has an IODELAY cell. The longest delay it can provide is about 128 steps x 25ps = 3200ps.

Figure 3-10 IODELAY



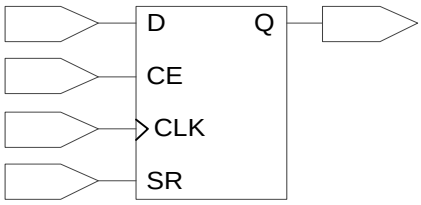
There are two ways to control the delay cell:

- Static control:
- Dynamic control: usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

See Figure Figure 3-11 for the I/O register in the GW1NSR series of FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

Figure 3-11 Register Structure in I/O Logic



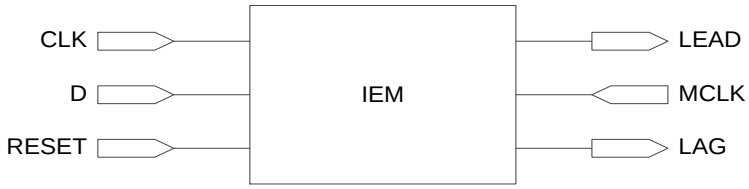
Note!

- CE can be either active ow (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-12 for the IEM structure.

Figure 3-12 IEM Structure



De-serializer DES

The GW1NSR series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

Serializer SER

The GW1NSR series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

3.4.4 I/O Logic Modes

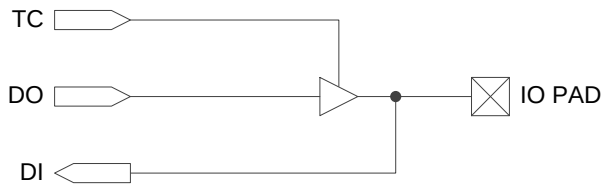
The I/O Logic in the GW1NSR series of FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

Not all the device pins support I/O logic. The IOL6 (A, B, C…. J) of GW1NSR-2 pins do not support IO logic.

Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-13, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

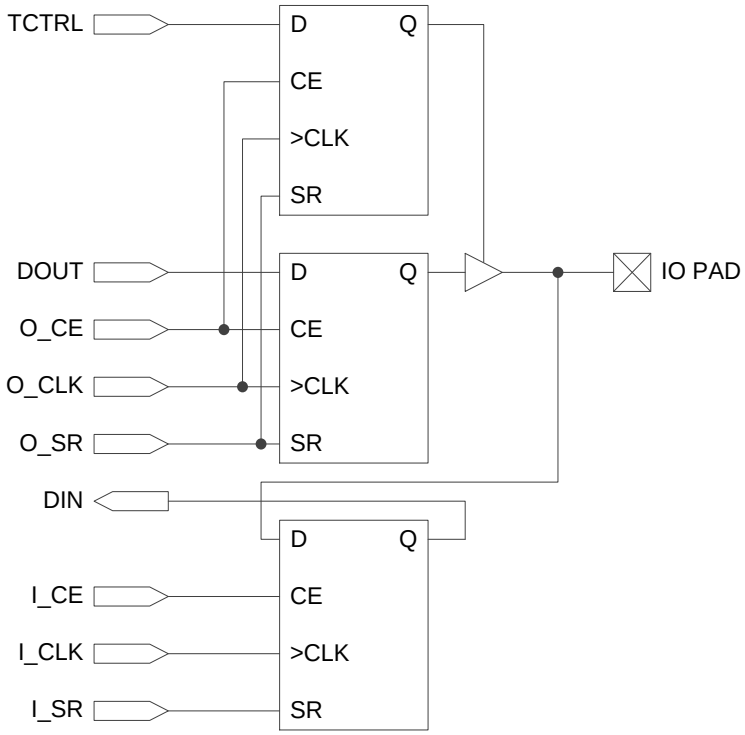
Figure 3-13 I/O Logic in Basic Mode



SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-14. This can effectively improve IO timing.

Figure 3-14 I/O Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either Synchronized reset,Synchronized set, Asynchronous reset, Asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

Higher speed I/O protocols can be supported in generic DDR mode.

Figure 3-15 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

Figure 3-15 I/O Logic in DDR Input Mode

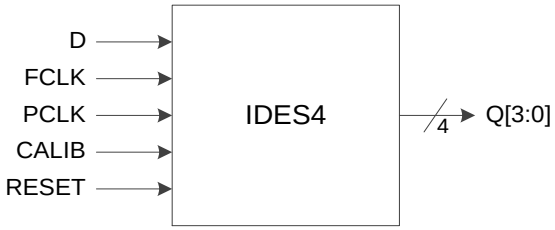
Figure 3-16 shows generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

Figure 3-16 I/O Logic in DDR Output Mode

IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

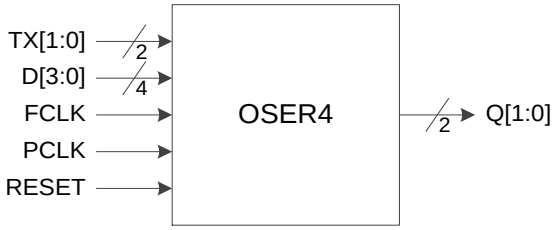
Figure 3-17 I/O Logic in IDES4 Mode



OSER4 Mode

In OSER4 mode, the speed ratio of the PAD to FPGA internal logic is 4:1.

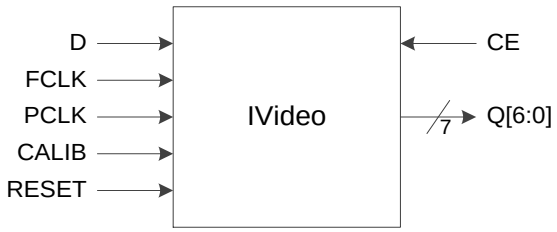
Figure 3-18 I/O Logic in OSER4 Mode



IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

Figure 3-19 I/O Logic in IVideo Mode



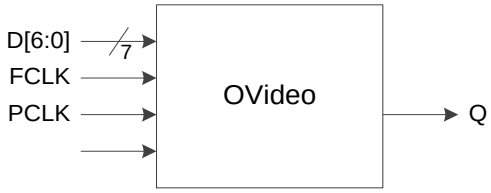
Note!

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is 7:1.

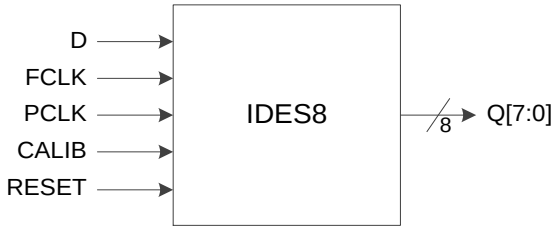
Figure 3-20 I/O Logic in OVideo Mode



IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

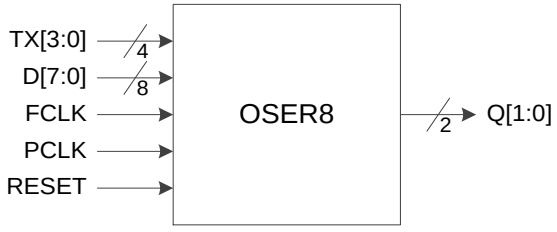
Figure 3-21 I/O Logic in IDES8 Mode



OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

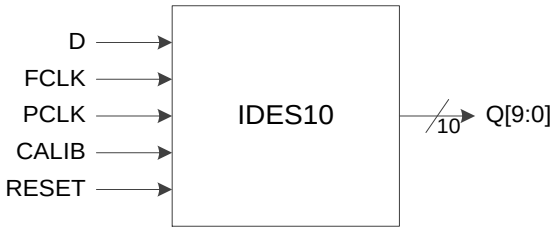
Figure 3-22 I/O Logic in OSER8 Mode



IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

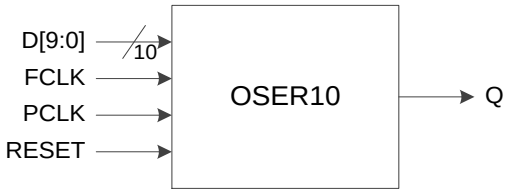
Figure 3-23 I/O Logic in IDES10 Mode



OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

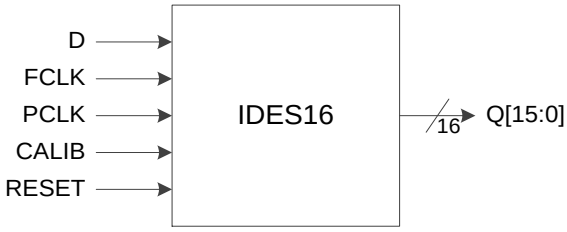
Figure 3-24 I/O Logic in OSER10 Mode



IDES16 Mode

In IDES16 mode, the speed ratio of the PAD to FPGA internal logic is 1:16.

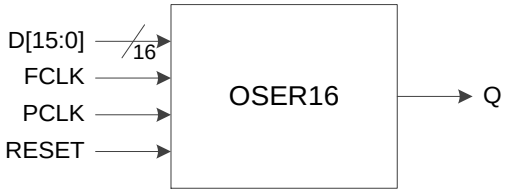
Figure 3-25 I/O Logic in IDES16 Mode



OSER16 Mode

In OSER16 mode, the speed ratio of the PAD to FPGA internal logic is 16:1.

Figure 3-26 I/O Logic in OSER16 Mode



3.5 Block SRAM (B-SRAM)

3.5.1 Introduction

GW1NSR series of FPGA products provide abundant SRAM. The Block SRAM (B-SRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each B-SRAM occupies three columns of CFU in the FPGA array.

B-SRAM supports two usages:

1. Used for Cortex-M3 SRAM, providing high-speed read/write functions for Cortex-M3 to ensure system operation. Cortex-M3 reads/writes the data using AHB bus. The data bit width is 32bits. Each B-SRAM provides 8 bits data. The address depth is 2048, and the total capacity is 64Kbits. In this way, this B-SRAM cannot be used as FPGA data storage.
2. Used for FPGA data storage of GW1NSR-2C and GW1NS-2 devices. Each B-SRAM can be configured up to 18,432 bits (18Kbits). In this way, this B-SRAM cannot be used as Cortex-M3 SRAM. There are 5 operation modes: Single Port, Dual Port, Semi Dual Port, ROM, and FIFO. The signals and functional descriptions of B-SRAM are listed in Table 3-4.

An abundance of B-SRAM resources provide a guarantee for the user's high-performance design. B-SRAM features:

- Max.18,432 bits per B-SRAM
- B-SRAM itself can run at 190MHz at max
- Single Port
- Dual Port
- Semi Dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Asynchronous reset, Synchronous reset
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

Table 3-4 B-SRAM Signals

Port Name	I/O	Description
DIA	I	Port A data input
DIB	I	Port B data input
ADA	I	Port A address
ADB	I	Port B address
CEA	I	Clock enable, Port A
CEB	I	Clock enable, Port B
RESETA	I	Register reset, Port A
RESETB	I	Register reset, Port B
WREA	I	Read/write enable, Port A
WREB	I	Read/write enable, Port B
BLKSEL	I	Block select
CLKA	I	Read/write cycle clock for Port A input registers
CLKB	I	Read/write cycle clock for Port B input registers
OCEA	I	Clock enable for Port A output registers
OCEB	I	Clock enable for Port B output registers
DOA	O	Port A data output
DOB	O	Port B data output

3.5.2 Configuration Mode

The B-SRAM mode in the GW1NSR series of FPGA products supports different data bus widths. See Table 3-5.

Table 3-5 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

3.5.3 Mixed Data Bus Width Configuration

B-SRAM in the GW1NSR series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-6 and Table 3-7 below.

Table 3-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*"denotes the modes supported.

Table 3-7 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*"denotes the modes supported.

3.5.4 Byte-enable

The B-SRAM in the GW1NSR series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the B-SRAM write operation.

3.5.5 Parity Bit

There are parity bits in B-SRAM. The 9th bit in each byte can be used as a parity bit or for data storage. However, the parity operation is not yet supported.

3.5.6 Synchronous Operation

- All the input registers of B-SRAM support synchronous write;
- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

3.5.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power-up process, B-SRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

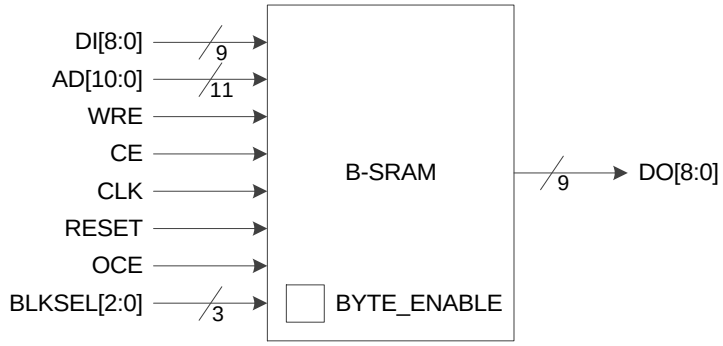
3.5.8 Operation Modes

The input registers of B-SRAM can be used for synchronous write. The output registers can be used as pipeline register to improve design performance. In the dual port mode, the two ports of B-SRAM can be operated totally independently. Port A and Port B have their own clock and are write-enabled; as such, both ports can be written to and read independently from each other.

Single Port Mode

In the single port mode, as shown below, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of B-SRAM. Normal write mode (Normal-write Mode) and write-through mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge. For the single port 2K x 9bits block memory, see Figure 3-27 below.

Figure 3-27 Single Port Block Memory



The table below shows all the configuration options that are available in the single port mode:

Table 3-8 Single Port Block Memory Configuration

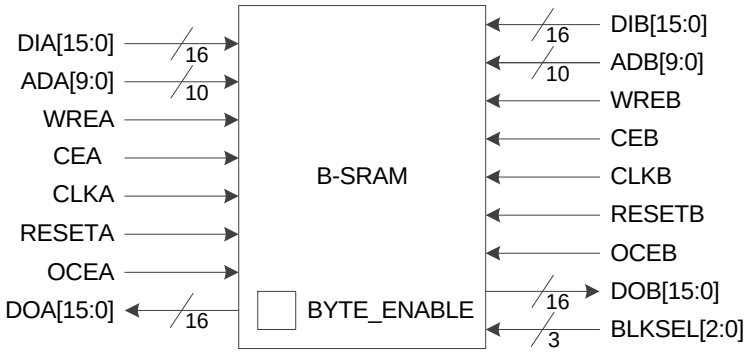
Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Read Data Width
SP	B-SRAM_16K_S1	16K	16K x 1	16,384	1
	B-SRAM_8K_S2	16K	8K x 2	8,192	2
	B-SRAM_4K_S4	16K	4K x 4	4,096	4
	B-SRAM_2K_S8	16K	2K x 8	2,048	8
	B-SRAM_1K_S16	16K	1K x 16	1,024	16
	B-SRAM_512_S32	16K	512 x 32	512	32
SPX9	B-SRAM_2K_S9	18K	2K x 9	2,048	9
	B-SRAM_1K_S18	18K	1K x 18	1,024	18
	B-SRAM_512_S36	18K	512 x 36	512	36

Dual Port Mode

B-SRAM support Dual Port mode, as shown in Figure 3-28. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

Figure 3-28 Semi-Dual Port Block Memory



All the configuration options for the dual port mode are as shown in Table 3-9 .

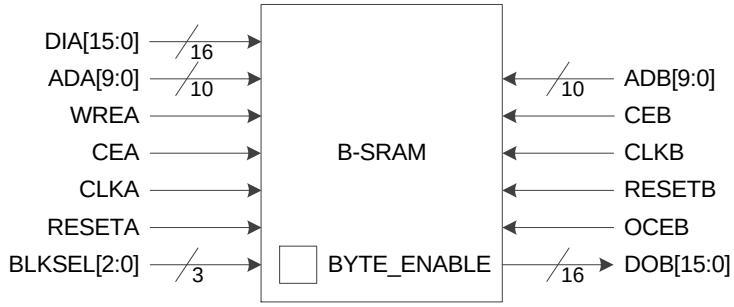
Table 3-9 Dual Port Memory Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Read Data Width
DP	B-SRAM_16K_D1	16K	16K x 1	16384	1
	B-SRAM_8K_D2	16K	8K x 2	8192	2
	B-SRAM_4K_D4	16K	4K x 4	4096	4
	B-SRAM_2K_D8	16K	2K x 8	2048	8
	B-SRAM_1K_D16	16K	1K x 16	1024	16
DPX9	B-SRAM_2K_D9	18K	2K x 9	2048	9
	B-SRAM_1K_D18	18K	1K x 18	1024	18

Semi-Dual Port Mode

The figure below shows the semi Dual Port 1 K x 16bits mode. It supports read and write at the same time on different ports. It is not possible to write and read to the same port at the same time. The system only supports write on port A , read on port B.

Figure 3-29 Semi Dual Port Block Memory 1



All the configuration options for the dual port mode are as shown in Table 3-10.

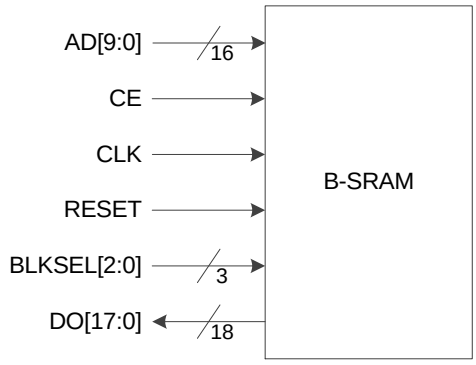
Table 3-10 Semi Dual Port Memory Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Read Data Width
SDP	B-SRAM_16K_SD1	16K	16K x 1	16,384	1
	B-SRAM_8K_SD2	16K	8K x 2	8,192	2
	B-SRAM_4K_SD4	16K	4K x 4	4,096	4
	B-SRAM_2K_SD8	16K	2K x 8	2,048	8
	B-SRAM_1K_SD16	16K	1K x 16	1,024	16
	B-SRAM_512_SD32	16K	512 x 32	512	32
SDPX9	B-SRAM_2K_SD9	18K	2K x 9	2,048	9
	B-SRAM_1K_SD18	18K	1K x 18	1,024	18
	B-SRAM_512_SD36	18K	512 x 36	512	36

Read Only

B-SRAM can be configured as ROM, as shown in Figure 3-30. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Figure 3-30 ROM Block Memory



Each B-SRAM can be configured as one 16 Kbits ROM. Table 3-11 lists all the configuration options for the ROM mode.

Table 3-11 Block ROM Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Read Data Width
ROM	B-SRAM_16K_O1	16K	16K x 1	16,384	1
	B-SRAM_8K_O2	16K	8K x 2	8,192	2
	B-SRAM_4K_O4	16K	4K x 4	4,096	4
	B-SRAM_2K_O8	16K	2K x 8	2,048	8
	B-SRAM_1K_O16	16K	1K x 16	1,024	16
	B-SRAM_512_O32	16K	512 x 32	512	32
ROMX9	B-SRAM_2K_O9	18K	2K x 9	2,048	9
	B-SRAM_1K_O18	18K	1K x 18	1,024	18
	B-SRAM_512_O36	18K	512 x 36	512	36

Note!

In the ROM mode, the RESET signal can only reset the input and output registers. It cannot clear the ROM content.

3.5.9 B-SRAM Operation Modes

B-SRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the B-SRAM via output registers or without using the registers.

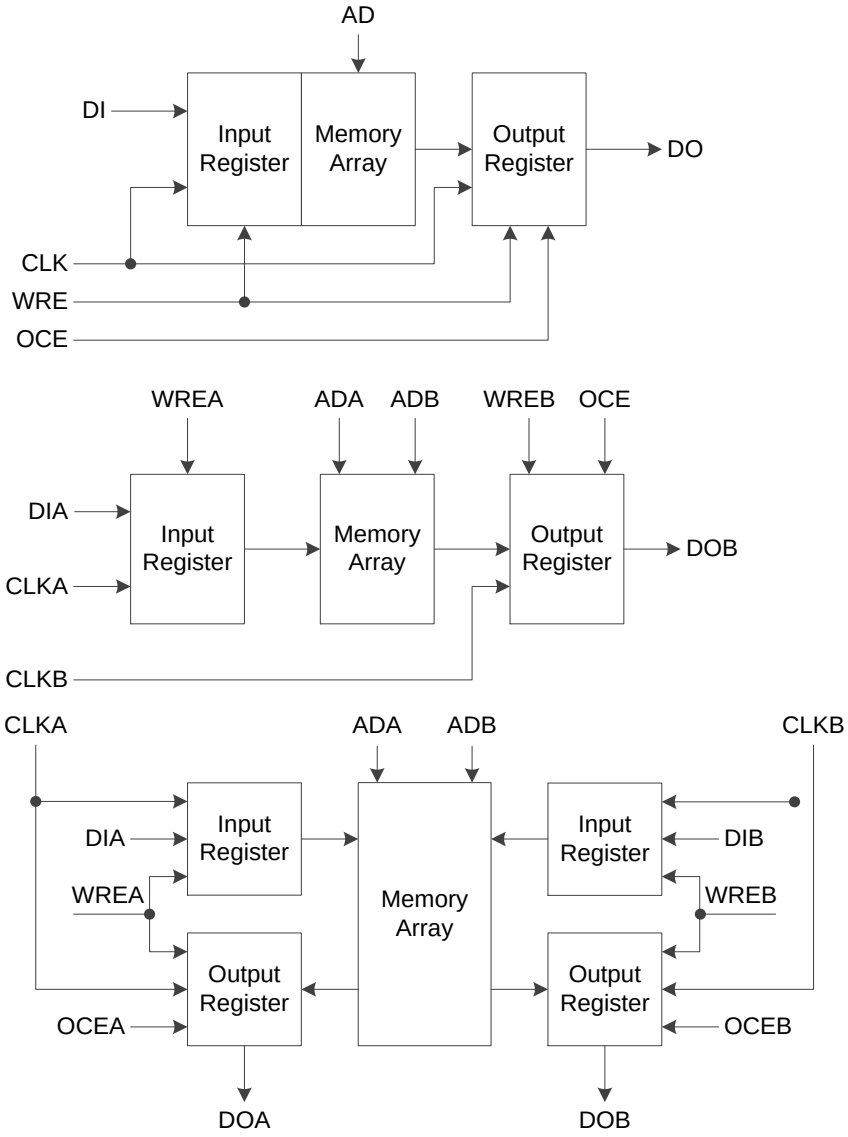
Pipeline Mode

While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of memory array.

Figure 3-31 Pipeline Mode in Single Port, Dual Port and Semi-Dual Port



Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.5.10 Clock Operations

Table 3-12 lists the clock operations in different B-SRAM modes:

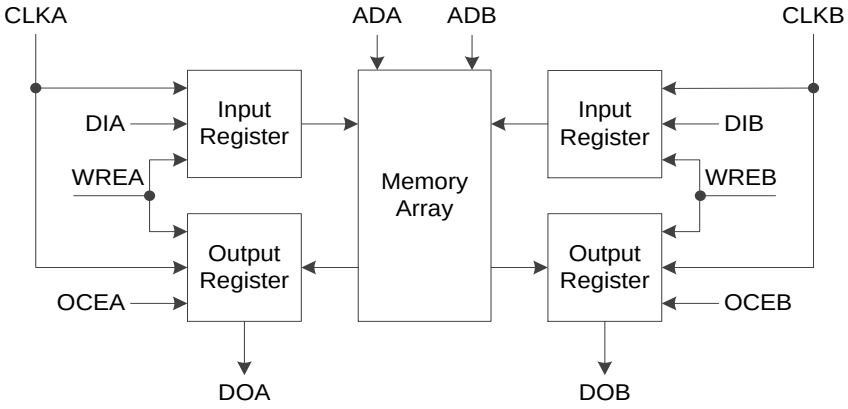
Table 3-12 Clock Operations in Different B-SRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-32 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

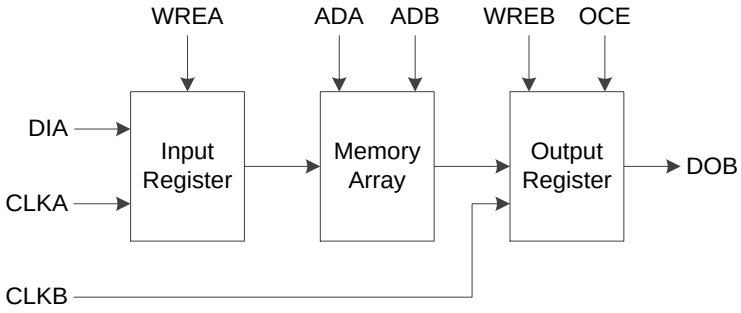
Figure 3-32 Independent Clock Mode



Read/Write Clock Operation

Figure 3-33 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

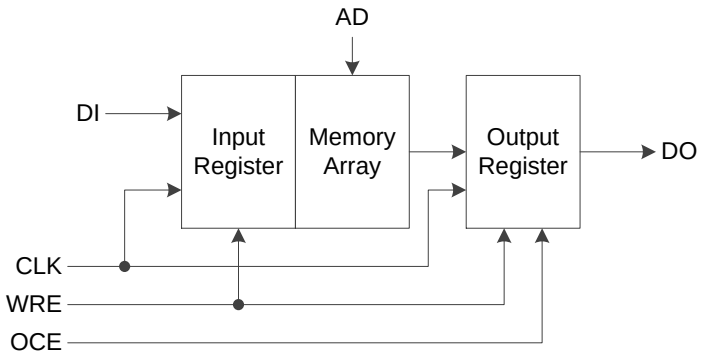
Figure 3-33 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-34shows the clock operation in single port mode.

Figure 3-34 Single Port Clock Mode



3.6 User Flash

3.6.1 Introduction

GW1NSR series of FPGA products offers 128 KB User Flash with the following functions:

1. Used for Cortex-M3 programming memory in GW1NSR-2C devices. User Flash can only be read and does not support the other two functions;
2. Offers non-volatile memory for users in GW1NSR-2C and GW1NSR-2 devices and does not support the other two functions;
3. In DUAL BOOT mode for GW1NSR-2C and GW1NSR-2 devices, on-chip downloaded flash is the primary memory for data bitstream; user flash is used as the secondary memory for data bitstream; The user flash used for this function does not support the other two functions.

Main features are as follows:

- 32 bits data input/output
- Page architecture
  - 128 x 32 bits page size
  - 256 pages in total
- Fast read, write, and erase
  - Read access time 30ns
  - Write time 30us
  - Page erasure time 2ms
  - Macro erasure time 10ms
- Lower power consumption
  - IDLE 100uA
  - Read operation current 60 uA/MHz
  - Write operation current 2.4mA
  - Erase operation current 2.4 mA
- 100,000 write/erase cycles
- Minimum10 years data retention

3.6.2 Port Signal

SeeFigure 3-35 for the User Flash signal diagram of GW1NSR series of FPGA products.

Figure 3-35 User Flash Ports

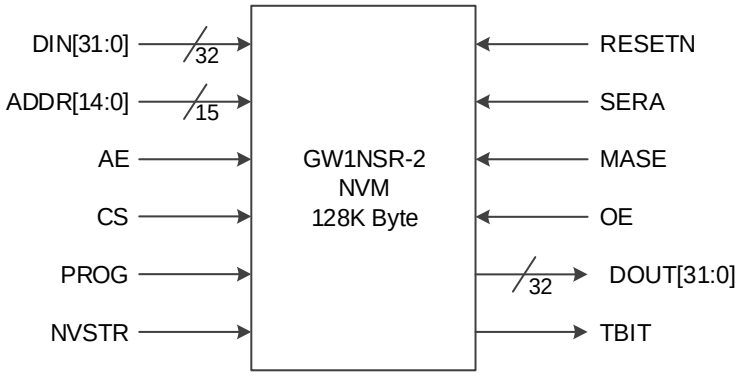


Table 3-13 Flash Module Signal Description

Pin name1	I/O	Description
RESETN	I	Reset signal, active - low
DIN[31:0]	I	Data input
ADDR[5:0]	I	Address input
AE	I	Address enable signals
CS	I	Chip select
PROG	I	Data enable signal
NVSTR	I	Write signal
SERA	I	Page erase signal
MASE	I	Macro erase signal
OE	I	Read enable
DOUT	O	Output data
TBIT	O	Indicator of write/erase done

Note!

[1] Port names of Control, address,and data signals.

3.6.3 Page Address Mapping

User flash capacity is 128KB. There are 256 pages in total, each of which has a page size of 512 bytes. Each page is divided into two lines, and each line includes 64 x 32 bits.

Table 3-14 User Data Flash Address Mapping

Page Selection Address								Line Selection	32bits Data Column Selection					
A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X8	X7	X6	X5	X4	X3	X2	X1	X0	Y5	Y4	Y3	Y2	Y1	Y0

Table 3-15 User Information Flash Address Mapping

Page Selection Address								Line Selection	32bits Data Column Selection					
A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	X1	X0	Y5	Y4	Y3	Y2	Y1	Y0

3.6.4 Operation Mode

User can set control signals to select different operation modes, as shown in Table 3-16.

Table 3-16Operation Modes

MODE	CS	AE	OE	PROG	SERA	MASE	DIN	DOUT	ADDR	NVSTR
IDLE	L	L	L	L	L	L	X	Z	X	X
Read	H	R	H	L	L	L	X	DOUT	ADDR	L
Write	H	R	L	H	L	L	DIN	Z	ADDR	H
Page Erasure Mode	H	R	L	L	H	L	X	Z	ADDR	H
Macro erase	H	R	L	L	L	H	X	Z	ADDR	H

3.6.5 Read Operation

The Flash read operation is similar to that of ROM. The following conditions need to be met to read data:

When the AE signal is pulled high and the address setup time is met (≥5ns), the address will be latched at the AE rising edge;

OE signal is pulled high, (≥1ns) data occurs at DOUT, and the data access time is 30ns.

3.6.6 Write Operation

Erase the memory you want to write before the write operation.

The Flash write operation (data 0) is similar to that of the SRAM write

operation. During the write operation, AE, PROG, and NVSTR must be high. Prepare the written data and address in advance. When the setup time is met (≥5ns), the data and address will be latched at the AE rising edge. When the AE is high and the NVSTR rising edge hold time is greater than 10 ns, NVSTR becomes high, and the data is written into the memory. The write access time is 30us.

3.6.7 Erase Operation

User Flash supports page erase and macro erase. The page erase size is 512 bytes. The macro erase size is the entire user data memory. When SERA is high, page erasure is valid; when MASE is high, Macro erasure is valid.

Page erase: AE, SERA, and NVSTR must be high for page erasure. Prepare the erasure address in advance. When the setup time is met (≥5ns), the address will be latched at the AE rising edge. When AE is high, and NVSTR rising edge hold time is greater than 10ns, NVSTR becomes high, and the address memory is erased, and the data becomes 1. Macro erasure time is 2 ms.

Macro erase: AE, MASE, and NVSTR must be high for macro erasure. Prepare the erasure address in advance. When the setup time is met (≥5ns), the address will be latched at the AE rising edge. When AE is high, and NVSTR rising edge hold time is greater than 10ns, NVSTR becomes high, and the address memory is erased, and the data becomes 1. Macro erasure time is 2ms.

3.7 Cortex-M3

3.7.1 Introduction

GW1NSR-2C is a system-on-chip FPGA device that incorporates a microprocessor system hard core, Gowin FPGA fabric, and other standard peripherals and featured hard cores, including USB2.0 PHY, ADC, 128 K-Byte Flash, 8 KB Block RAM, PLL, and OSC. The embedded microprocessor system contains a low-power, low-cost and high-performance ARM Cortex-M3 32-bit RISC. The flexible FPGA fabric serves as user programmable peripherals, or soft-core IPs.

The embedded microprocessor system consists of the processor block, with ARM Cortex-M3 32-bit RISC core and associated supporting bus system that connects to harden standard peripherals. The FPGA fabric contains a rich programmable logic resource called a Configured Functional Unit (CFU). This offers a flexible architecture that allows the user to employ peripherals with the microprocessor system. This can be achieved either by parameterized soft-core IPs, I2C or I3C. The microprosessor system only interfaces with the FPGA fabric and JTAG config-core internally with no access to the I/O Blocks of GW1NSR-2C.

The bus system consists of AHB-Lite Bus, AHB2APB Bridge, and two APB Bus: APB1 and APB2.

The microprocessor system relies on AHB bus to access FPGA side sub-memory system which has a pre-implemented sub-memory system

controller for read-only-access 128 KB Flash-ROM and read/write-access 8 KB B-SRAM. Upon Power-On boot loading, Cortex-M3 loads instructions and data that are pre-stored in the Flash-ROM, and transfers it to the B-SRAM before initiating the execution.

In addition, there are two AHB bus extension ports: INTEXP0 and TARGEXP0. Each of these AHB extension ports provides a 126-bit AHB bus interconnecting to any high-speed User programmable peripherals implemented within the FPGA. A GPIO block interconnects the AHB bus with the FPGA fabric to allow the user to implement general purpose I/O functions in FPGA.

In terms of the two APB Bus (APB1 and APB2), APB1 interconnects with two timers (Timer0 and Timer1), two UARTs (Uart0 and Uart1), and one watchdog. Two UARTs connect to the FPGA directly. The two timers and the watchdog are controlled and used within the microprocessor system and are accessed through REG. The APB2 bus connects directly to the FPGA.

The processor block consists of Cortex-M3 core, bus matrix, Nested Vector Interrupt Controller (NVIC), Debug Access Port (DAP), and time stamp.

The Cortex-M3 core relies on the bus-matrix to access its supporting bus system (AHB-Lite Bus, AHB2APB Bridge, and two APB Bus: APB1 and APB2).

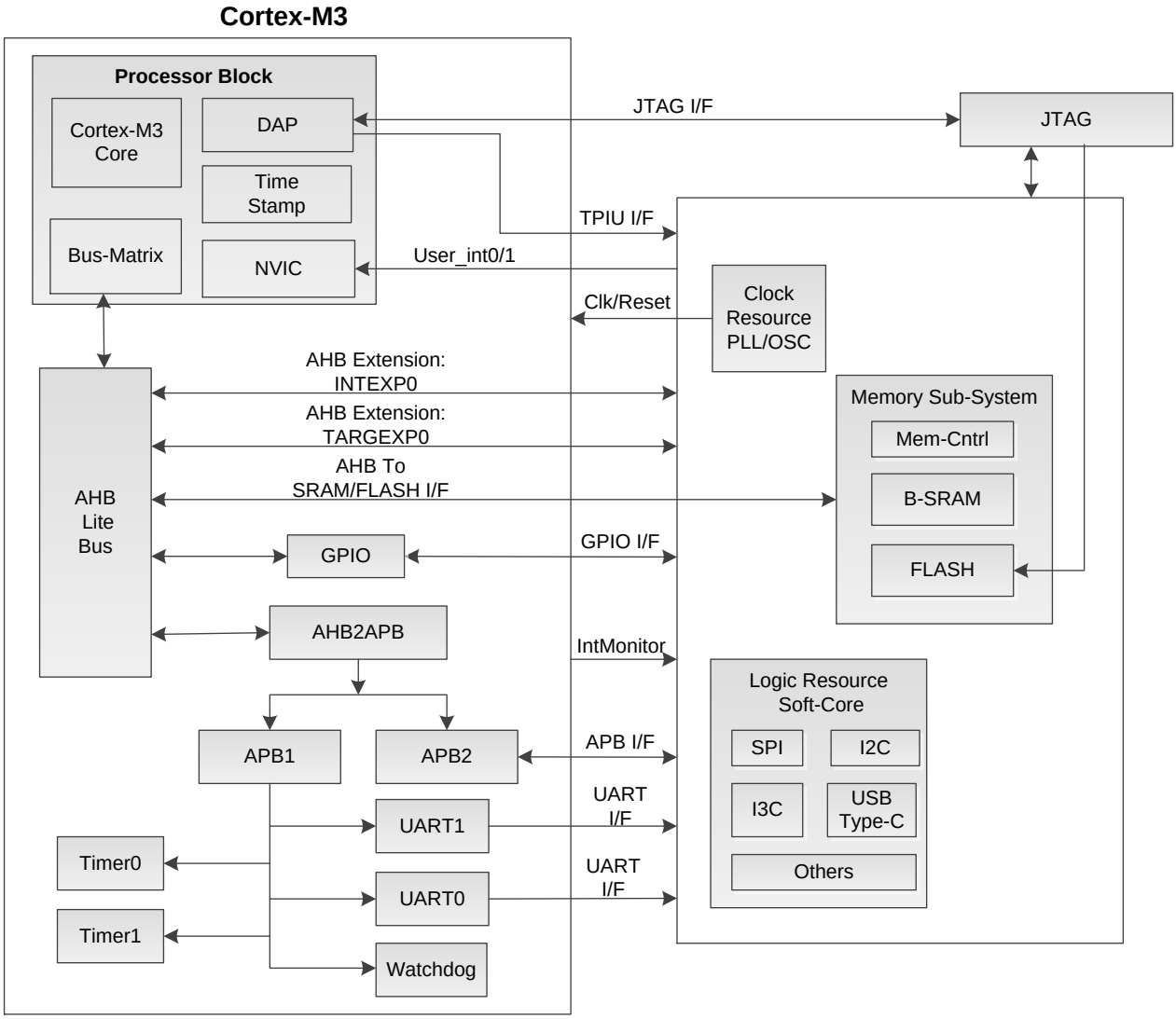
NVIC offers USER_INT0 and USER_INT1, serving as interrupt requests to NVIC from user implementing peripherals in FPGA fabric. The DAP contains JTAG DAP and also Trace-Port-Interface-Unit (TPIU).

The Microprocessor System also provides an interrupt monitor signal, which combines GPIO interrupts as well as APB1 peripherals (UART0, UART1, Timer0, Timer1, Watchdog) interrupts, back to the FPGA fabric to report the current run-time interrupt Status of the Microprocessor System.

FPGA fabric takes advantage of its rich Clocking Resource (PLL, OSC) and provides the Main Clock, Power-On Reset and System Reset signals to the embedded microprocessor system.

See Figure 3-36 for the Cortex-M3 architecture.

Figure 3-36 Cortex-M3 Architecture



3.7.2 Cortex-M3

Features:

- Compact core
- Thumb-2 instruction set, delivering the high-performance expected of an ARM core in the memory size usually
- Associated with 8 bits and 16 bits devices; typically, in the range of a few kilobytes of memory for microcontroller class applications
- Rapid application execution through Harvard architecture characterized by separate buses for instruction and data
- Achieves exceptional interrupt handling, by implementing the register manipulations required for handling an interrupt in hardware.
- Deterministic, fast interrupt processing.
- Memory protection unit (MPU), providing a privileged mode for protecting operation system functionality
- Migration from the ARM7™ processor family for better performance and power efficiency
- Full-featured debug solution

- JTAG Debug Port (JTAG)
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
- Data Watchpoint and Trigger (DWT) unit for implementing watchpoints, trigger resources, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of print style debugging
- Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

3.7.3 Bus-Matrix

The bus-matrix is used to connect the Cortex-M3 processor and debug port with an external AHB bus. **Connections between bus-matrix and AHB bus:**

- ICode bus: 32bit AHBLite bus, used for fetching instructions and vectors from code space;
- DCode bus: 32bit AHBLite bus, used for data loading/storage and debug access;
- System bus: 32bit AHBLite bus, used for fetching instructions and vectors from system space, data loading/storage and debug access;
- APB: 32bit APB bus, used for external space data loading/storage and debug access.

The bus-matrix controls the following functions as below:

- Unaligned accesses: Converts the unaligned processor access to aligned access;
- Bit-banding: converts the alias access of Bit_band to Bit_band space access;
- Write buffer: Bus-matrix contains one write-buffer, ensuring that the processor core is not affected by bus delay.

3.7.4 NVIC

NVIC features:

- Supports low-latency interrupt processing up to 26 interrupts
- Two external user defined interrupts: USER_INT0 and USER_INT1
- A programmable priority level of 0-7 for each interrupts. A higher level corresponds to a lower priority; as such level 0 is the highest interrupt priority
- Low-latency exception and interrupt handling
- Dynamic reprioritization of interrupts
- The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead.

Table 3-17NVIC Address Table

Address	Name	Type	Description
0x00000000	_StackTop	Read only	Top of stack interrupt
0x00000004	Reset_Handler	Read only	Reset interrupt
0x00000008	NMI_Handler	Read only	NMI interrupt
0x0000000C	HardFault_Handler	Read only	Hard fault interrupt
0x00000010	MemMange_Handler	Read only	MPU fault interrupt
0x00000014	BusFault_Handler	Read/ Write	Bus fault interrupt
0x00000018	UsageFault_Handler	Read only	Usage fault interrupt
0x0000002C	SVC_Handler	Read/ Write	SVCall interrupt
0x00000030	DebugMon_Handler	Read only	Debug monitor interrupt
0x00000038	PendSV_Handler	Read / Write / Read only	Pending interrupt
0x0000003C	SysTick_Handler	Read/ Write	System timer interrupt
External interrupt			
0x00000040	UART0_Handler	Read/ Write	UART0 reception and sending interrupt
0x00000048	UART1_Handler	Read/ Write	UART1 reception and sending interrupt
0x00000058	PORT0_COMB_Handler	Read/ Write	GPIO0 interrupt
0x00000060	TIMER0_Handler	Read/ Write	TIMER0 interrupt
0x00000064	TIMER1_Handler	Read/ Write	TIMER1 interrupt
0x00000070	UARTOVF_Handler	Read/ Write	UART0/UART1 overflow interrupt
0x00000074	USER_INT0	Read/ Write	Flash system error interrupt
0x00000078	USER_INT1	Read/ Write	Embedded flash interrupt
0x00000080	PORT0_0_Handler	Read/ Write	GPIO0 Pin 0 interrupt
0x00000084	PORT0_1_Handler	Read/ Write	GPIO0 Pin 1 interrupt
0x00000088	PORT0_2_Handler	Read/ Write	GPIO0 Pin 2 interrupt
0x0000008C	PORT0_3_Handler	Read/ Write	GPIO0 Pin 3 interrupt
0x00000090	PORT0_4_Handler	Read/ Write	GPIO0 Pin 4 interrupt
0x00000094	PORT0_5_Handler	Read/ Write	GPIO0 Pin 5 interrupt

Address	Name	Type	Description
0x00000098	PORT0_6_Handler	Read/ Write	GPIO0 Pin 6 interrupt
0x0000009C	PORT0_7_Handler	Read/ Write	GPIO0 Pin 7 interrupt
0x000000A0	PORT0_8_Handler	Read/ Write	GPIO0 Pin 8 interrupt
0x000000A4	PORT0_9_Handler	Read/ Write	GPIO0 Pin 9 interrupt
0x000000A8	PORT0_10_Handler	Read/ Write	GPIO0 Pin 10 interrupt
0x000000AC	PORT0_11_Handler	Read/ Write	GPIO0 Pin 11 interrupt
0x000000B0	PORT0_12_Handler	Read/ Write	GPIO0 Pin 12 interrupt
0x000000B4	PORT0_13_Handler	Read/ Write	GPIO0 Pin 13 interrupt
0x000000B8	PORT0_14_Handler	Read/ Write	GPIO0 Pin 14 interrupt
0x000000BC	PORT0_15_Handler	Read/ Write	GPIO0 Pin 15 interrupt

3.7.5 Boot Loader

The boot loader loads the initial stack pointer value from the program memory, and branches to the reset handler that the reset vector specifies in the program memory.

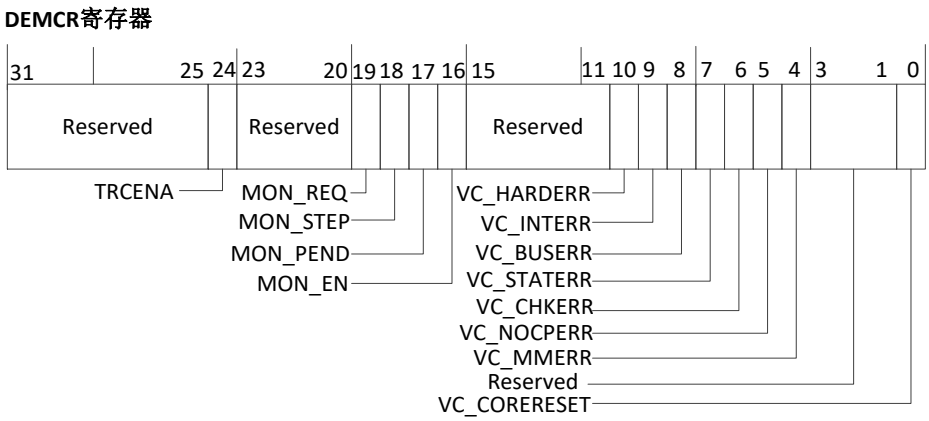
The current boot loader is based on UART Message Monitor which is easy to interface as a communication port with PC host. Below is an example of how to deploy the boot loader:

- Power-on reset to enter the reset handler to call the boot loader;
- Setup UART0 registers, such as BAUDIV and CTRL, to program the appropriate TX speed rate for the send and receive function;
- Begin Flash loader subroutine execution such as memory test, timer0, and timer1 tests etc;
- Write a 0x4 character (EOP) to terminate the program.

3.7.6 TimeStamp

A 48 bits timestamp counter is included and connected to the ITM. It is clock gated and enabled by the Trace Enable (TRCENA) bit of DEMCR (0xE000EDFC) Debug Exception and monitor control register, which is a global enable bit that enables both the Data Watch Trace (DWT) and Intrumental Trace Module (ITM) on behalf of the debug of the Cortex-M3 microprocessor. The time stamp generator is used during the debug process to set up the break point and marching step, etc.

Figure 3-37 DEMCR Register



Note!

TRCENA is the global enable for DWT and ITM features:

- 0: DWT and ITM units disabled.
- 1: DWT and ITM units enabled.

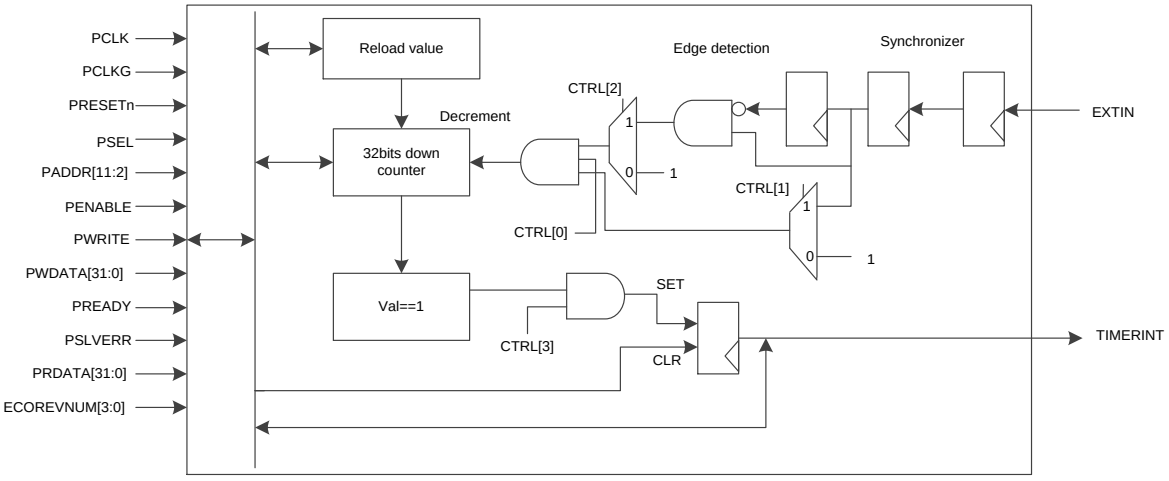
3.7.7 Timer

GW1NSR-2C offers an embedded microprocessor system that contains two synchronous standard timers: Timer0 and Timer1. These can be accessed and controlled through APB1 bus.

Timer0 and Timer1 are 32 bits down-counter with the following features:

- Users can generate an interrupt request signal, TIMERINT, when the counter reaches 0. The interrupt request is held until it is cleared by writing to the INTCLEAR Register.
- Users can employ the zero-to-one transition of the external input signal, EXTIN, as a timer enable.
- If the timer count reaches 0 and, at the same time, the software clears a previous interrupt status, the interrupt status is set to 1.
- The external clock, EXTIN, must be slower than half of the peripheral clock because it is sampled by a double flip-flop before going through edge-detection logic when the external inputs act as a clock.
- Timer0: EXTIN is hard-wired to GPIO[1]
- Timer1: EXTIN is hard-wired to GPIO[6]

Figure 3-38 Timer0/ Timer1 Structure View



The Timer0/Timer1 register is as shown in Table 3-18. The Timer0 base address is 0x40000000, and the Timer1 base address is 0x40001000.

Table 3-18 Timer0/Timer1 Register

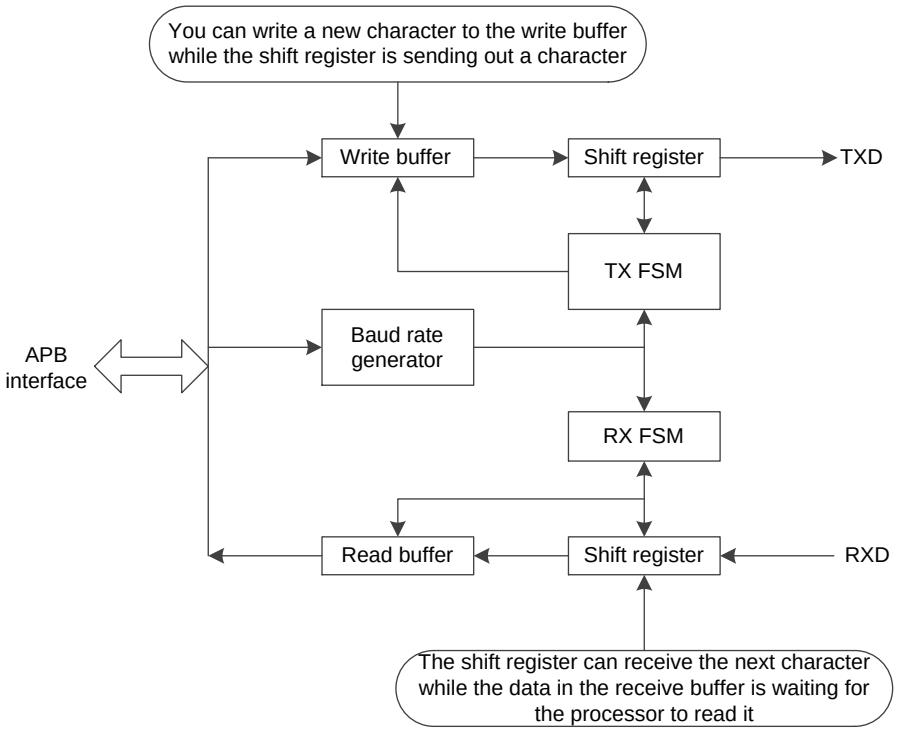
Name	Base Offset	Type	Data Width	Reset Value	Description
CTRL	0x000	Read/ Write	4	0x0	[3]: System timer interrupt enable [2]: Select external input as clock [1]: Select external input as enable [0]: Enable
VALUE	0x004	Read/ Write	32	0x00000000	Current value
RELOAD	0x008	Read/ Write	32	0x00000000	Reload value. Write to this register to set the current value.
INTSTATUS /INTCLEAR	0x00C	Read/ Write	1	0x0	[0]: Timer interrupt. Write one to clear.
PID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
PID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
PID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
PID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
PID0	0XFE0	Read only	8	0x22	Peripheral ID Register 0
PID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
PID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
PID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
CID0	0XFF0	Read only	8	0X0D	Component ID Register 0
CID1	0XFF4	Read only	8	0XF0	Component ID Register 1
CID2	0XFF8	Read only	8	0X05	Component ID Register 2
CID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.7.8 UART

The GW1NSR-2C embedded microprocessor system contains two UART: UART0 and UART1. These can be accessed and controlled through APB1 bus. The max. baud rate supported is 921.6Kbits/s.

UART0 and UART1support 8 bits communication without parity and one stop bit.

Figure 3-39 APB UART Buffering



UART0 and UART support a high-speed test mode. When CTRL[6] is set to 1, the serial data is transmitted at one bit per clock cycle. This enables you to send text messages in a much shorter simulation time. The APB interface always sends an "OK" response with no wait state. You must program the baud rate divider register BAUDDIV before enabling the UART.

The BAUDTICK output pulses at a frequency of 16 times that of the programmed baud rate. You can use this external signal for capturing UART data in a synchronous environment. The TXEN output signal indicates the status of CTRL[0]. You can use this signal to switch a bidirectional I/O pin in a silicon device to UART data output mode automatically when the UART transmission feature is enabled.

The buffer overrun status in the STATE field is used to drive the overrun interrupt signals. Therefore, clearing the buffer overrun status de-asserts the overrun interrupt, and clearing the overrun interrupt bit also clears the buffer overrun status bit in the STATE field.

See Table 3-19 for the UART Register Description. The UART0 base address is 0x40004000, and the UART1 base address is 0x40005000.

Table 3-19UART0/UART1 Register

Name	Base Offset	Type	Data Width	Reset Value	Description
DATA	0x000	Read/ Write	8	0x--	8 bits data Read: Received data. Write: Transmit data.
STATE	0x004	Read/ Write	4	0x0	[3]: RX buffer overrun, write 1 to clear. [2]: TX buffer overrun, write 1 to clear. [1]: RX buffer full, read-only. [0]: TX buffer full, read-only.
CTRL	0x008	Read/ Write	7	0x00	[6]：High-speed test mode for TX only. [5]：RX overrun interrupt enable. [4]：TX overrun interrupt enable. [3]：RX interrupt enable. [2]：TX interrupt enable. [1]：RX enable. [0]：TX enable.
INTSTATUS /INTCLEAR	0x00C	Read/ Write	4	0x0	[3]：RX overrun interrupt, write 1 to clear. [2]：TX overrun interrupt, write 1 to clear. [1]：RX interrupt, write 1 to clear. [0]：TX interrupt, write 1 to clear.
BAUDDIV	0x010	Read/ Write	20	0x00000	[19:0]: Baud rate divider. The minimum number is 16.
PID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
PID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
PID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
PID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
PID0	0XFE0	Read only	8	0x21	Peripheral ID Register 0
PID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
PID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
PID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
CID0	0XFF0	Read only	8	0X0D	Component ID Register 0
CID1	0XFF4	Read only	8	0XF0	Component ID Register 1
CID2	0XFF8	Read only	8	0X05	Component ID Register 2
CID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.7.9 Watchdog

The GW1NSR-2C embedded microprocessor system contains one watchdog module. This can be accessed and controlled through the APB1 bus.

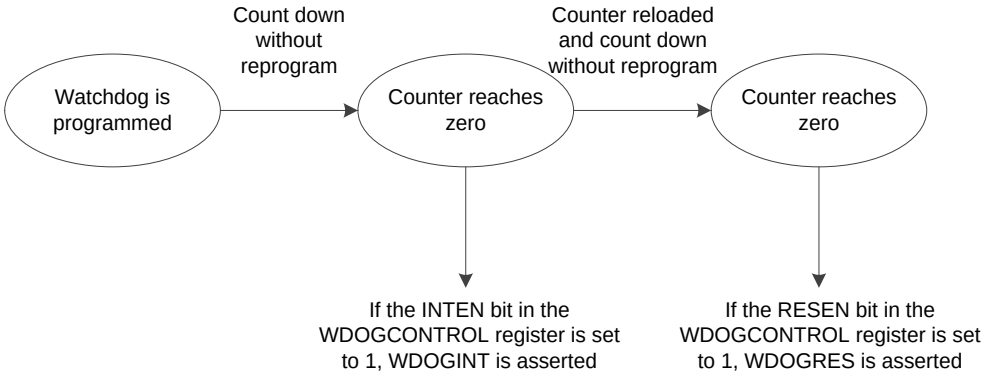
The APB watchdog module is based on a 32 bits down-counter that is initialized from the reload register, WDOGLOAD.

The watchdog module generates a regular interrupt, WDOGINT, depending on a programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is HIGH. The watchdog monitors the interrupt and asserts a reset request WDOGRES signal when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues.

The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes. For example, if the interrupt is not cleared by the time the counter next reaches 0, the watchdog module initiates the reset signal.

Figure 3-39 below depicts the watchdog operation.

Figure 3-40 Watchdog Operation



The watchdog register is as shown in Table 3-20. The watchdog base address is 0x40008000.

Table 3-20 Watchdog Register

Name	Base Offset	Type	Data Width	Reset Value	Description
WDOGLOAD	0x00	Read/ Write	32	0xFFFFFFFF	Watchdog Load Register
WDOGVALUE	0x04	Read only	32	0xFFFFFFFF	Watchdog Value Register
WDOGCONTROL	0x08	Read/ Write	2	0x0	Watchdog Control Register [1]： [0]：
WDOGINTCLR	0x0C	Write only	-	0x-	Watchdog Clear Interrupt Register
WDOGRIS	0x10	Read only	1	0x0	Watchdog Raw Interrupt Status Register
WDOGMIS	0x14	Read only	1	0x0	Watchdog Interrupt Status Register
WDOGLOCK	0xC00	Read/ Write	32	0x0	Watchdog Lock Register
WDOGTCR	0xF00	Read/ Write	1	0x0	Watchdog Integration Test Control Register
WDOGTOP	0xF04	Write only	2	0x0	Watchdog Integration Test Output Set Register
WDOGPERIPHID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
WDOGPERIPHID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
WDOGPERIPHID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6
WDOGPERIPHID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
WDOGPERIPHID0	0XFE0	Read only	8	0x24	Peripheral ID Register 0
WDOGPERIPHID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
WDOGPERIPHID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
WDOGPERIPHID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
WDOGPCELLID0	0XFF0	Read only	8	0X0D	Component ID Register 0
WDOGPCELLID1	0XFF4	Read only	8	0XF0	Component ID Register 1
WDOGPCELLID2	0XFF8	Read only	8	0X05	Component ID Register 2
WDOGPCELLID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.7.10 GPIO

The GW1NSR-2C microprocessor system communicates with the GPIO block through the AHB bus. The GIPO block interconnects with the FPGA. GPIO provides a 16 bits I/O interface with the following properties:

- Programmable interrupt generation capability. You can configure each bit of the I/O pins to generate interrupts;

- Bit masking support using address values;
- Registers for alternate function switching with pin multiplexing support;
- Thread safe operation by providing separate set and clear addresses for control registers.

The GPIO register is as shown in Table 3-21. The GPIO base address is 0x40010000.

Table 3-21GPIO Register

Name	Base Offset	Type	Data Width	Reset Value	Description
DATA	0x0000	Read/ Write	16	0x----	Data value [15:0]
DATAOUT	0x0004	Read/ Write	16	0x0000	Data output register value [15:0]
OUTENSET	0x0010	Read/ Write	16	0x0000	Output enable set [15:0] Write 1: Set the output enable bit. Write 0: No effect. Read 1: Indicates the signal direction as output. Read 0: Indicates the signal direction as input.
OUTENCLR	0x0014	Read/ Write	16	0x0000	Output enable clear [15:0]
ALTFUNCSET	0x0018	Read/ Write	16	0x0000	Alternative function set [15:0] Write 1: Sets the ALTFUNC bit. Write 0: No effect. Read 0: GPIO as I/O Read 1: ALTFUNC Function
ALTFUNCCLR	0x001C	Read/ Write	16	0x0000	Alternative function clear [15:0]
INTENSET	0x0020	Read/ Write	16	0x0000	Interrupt enable set [15:0] Write 1: Sets the enable bit. Write 0: No effect. Read 0: Interrupt disabled. Read 1: Interrupt enabled.
INTENCLR	0x0024	Read/ Write	16	0x0000	Interrupt enable clear [15:0] Write 1: Clear the enable bit. Write 0: No effect. Read 0: Interrupt disabled. Read 1: Interrupt enabled.
INTTYPESET	0x0028	Read/ Write	16	0x0000	Interrupt type set [15:0]
INTTYPECLR	0x002C	Read/ Write	16	0x0000	Interrupt type clear [15:0]
INTPOLSET	0x0030	Read/ Write	16	0x0000	Polarity-level, edge interrupt request configuration [15:0]
INTPOLCLR	0x0034	Read/ Write	16	0x0000	Polarity-level, edge interrupt request configuration [15:0]
INTSTATUS/ INTCLEAR	0x0038	Read/ Write	16	0x0000	Read interrupt status register Write 1: Clear the interrupt request
MASKLOWBYTE	0x0400-0x07FC	Read/ Write	16	0x0000	–
MASKHIGHBYTE	0x0800-0x0BFC	Read/ Write	16	0x0000	–
Reserved	0x0C00-0x0FCF	–	–	–	Reserved
PID4	0XFD0	Read only	8	0x04	Peripheral ID Register 4
PID5	0XFD4	Read only	8	0x00	Peripheral ID Register 5
PID6	0XFD8	Read only	8	0x00	Peripheral ID Register 6

Name	Base Offset	Type	Data Width	Reset Value	Description
PID7	0XFDC	Read only	8	0x00	Peripheral ID Register 7
PID0	0XFE0	Read only	8	0x20	Peripheral ID Register 0
PID1	0XFE4	Read only	8	0XB8	Peripheral ID Register 1
PID2	0XFE8	Read only	8	0X1B	Peripheral ID Register 2
PID3	0XFEC	Read only	8	0X00	Peripheral ID Register 3
CID0	0XFF0	Read only	8	0X0D	Component ID Register 0
CID1	0XFF4	Read only	8	0XF0	Component ID Register 1
CID2	0XFF8	Read only	8	0X05	Component ID Register 2
CID3	0XFFC	Read only	8	0XB1	Component ID Register 3

3.7.11 Debug Access Port

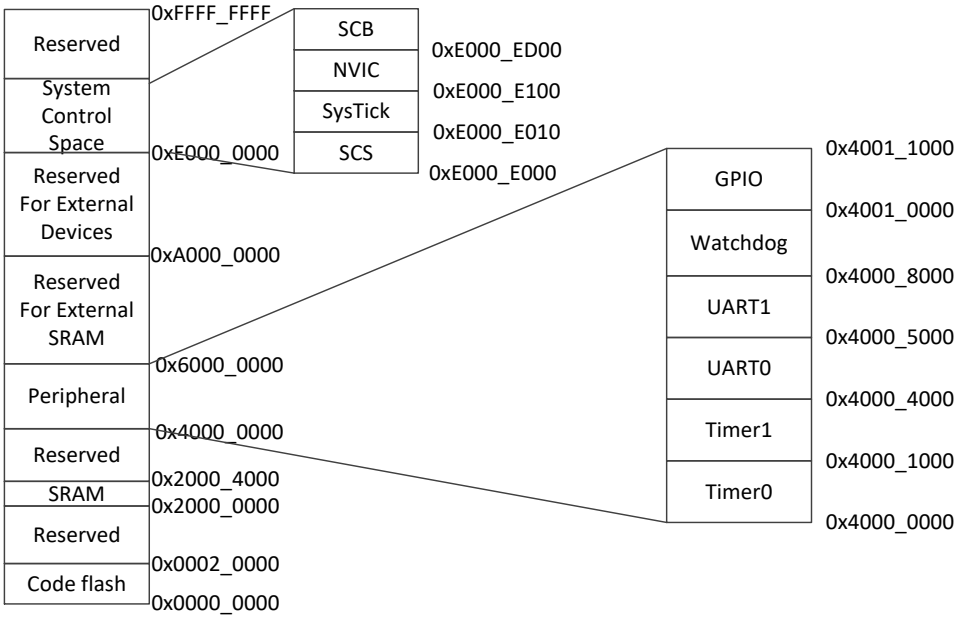
The Cortex-M3 processor block contains a DAP that consist of a JTAG DAP and a TPIU port. Both interface to the FPGA Fabric. The JTAG-DAP is based on the IEEE1149.1 Joint Test Action Group Boundary-Scan Standard.

JTAG-DP functions consist of the following three parts:

- JTAG-DP sate machine
- Instruction register (IR) and the related IR scan chain, which are used to control JTAG and the current register actions
- DR register and the related DR scan chain, which connect with the JTAG-DP register.

3.7.12 Memory Mapping

Figure 3-41 Memory Mapping



3.7.13 Ports Signal Description

Table 3-22 Cortex-M3 Ports Signal

Port Name	I/O	Description
Clock and Reset signal		
FCLK	I	Clock signal
PORESETN	I	Power on reset
SYSRESETN	I	System Reset
GPIO signals		
IOEXPOUTPUTO [15:0]	Output	GPIO output
IOEXPOUTPUTENO [15:0]	Output	GPIO output enable
IOEXPINPUTI [15:0]	I	GPIO input
UART signal		
UART0TXDO	Output	UART0 sends signals
UART1TXDO	Output	UART1 sends signals
UART0BAUDTICK	Output	UART0 Baud rate clock
UART1BAUDTICK	Output	UART0 Baud rate clock
UART0RXDI	Input	UART0 receives signals
UART1RXDI	Input	UART1 receives signals
AHB Lite TO SRAM signals		
MTXHRESETN	Output	SRAM reset signal
SRAM0ADDR [12:0]	Output	SRAM read/write address

Port Name	I/O	Description
SRAM0WREN	Output	SRAM read/write enable
SRAM0WDATA [31:0]	Output	SRAM writes data
SRAM0CS	Output	SRAM chip select
SRAM0RDATA	Input	SRAM reads data
AHB Lite TO Flash interface signals		
TARGFLASH0HSEL	Output	Flash transmits the select signals
TARGFLASH0HADDR[28:0]	Output	Flash transmits read/write address
TARGFLASH0HTRANS[1:0]	Output	Flash transmission types
TARGFLASH0HWRITE	Output	Flash transmits read/write enable
TARGFLASH0HSIZE[2:0]	Output	Flash transmits data width
TARGFLASH0HBURST[2:0]	Output	Flash transmits burst length configuration signals
TARGFLASH0HPROT[3:0]	Output	Flash transmits protection and control types
TARGFLASH0MEMATTR[1:0]	Output	Flash transmits memory attributes
TARGFLASH0EXREQ	Output	Flash transmits exclusive request
TARGFLASH0HMASTER[3:0]	Output	Flash transmits master selection
TARGFLASH0HWDATA[31:0]	Output	Flash transmits the written data
TARGFLASH0HMASTLOCK	Output	Flash transmits the locked signals
TARGFLASH0HREADYMUX	Output	Flash transmission done
TARGFLASH0HAUSER	Output	Flash transmits user read/write address
TARGFLASH0HWUSER[3:0]	Output	Flash transmits the user's written data
TARGFLASH0HRDATA[31:0]	Input	Flash transmits the readout data
TARGFLASH0HRUSER[2:0]	Input	Flash transmits the user readout data
TARGFLASH0HRESP	Input	Flash transmits the slave response
TARGFLASH0EXRESP	Input	Flash transmits the exclusive response
TARGFLASH0HREADYOUT	Input	The feedback signal of the Flash transmission done
AHB Lite TARGEXP0 extension interface signals		
TARGEXP0HSEL	Output	Flash transmits the selected signals
TARGEXP0HADDR[31:0]	Output	Flash transmits read/write address
TARGEXP0HTRANS[1:0]	Output	Transmission extension types
TARGEXP0HWRITE	Output	Read/write enable transmission extension
TARGEXP0HSIZE[2:0]	Output	Data width transmission extension
TARGEXP0HBURST[2:0]	Output	Burst types transmission extension
TARGEXP0HPROT[3:0]	Output	Protection types transmission extension
TARGEXP0MEMATTR[1:0]	Output	Memory attributes transmission

Port Name	I/O	Description
		extension
TARGEXP0EXREQ	Output	Exclusive request transmission extension
TARGEXP0HMASTER[3:0]	Output	Master selection transmission extension
TARGEXP0HWDATA[31:0]	Output	Written data transmission extension
TARGEXP0HMASTLOCK	Output	Locked signals transmission extension, used for bit band
TARGEXP0HREADYMUX	Output	Transmission extension done
TARGEXP0HAUSER	Output	User read/write address transmission extension
TARGEXP0HWUSER[3:0]	Output	User written data transmission extension
TARGEXP0HRDATA[31:0]	Input	Read-out data transmission extension
TARGEXP0HREADYOUT	Input	The feedback signal of transmission extension done
TARGEXP0HRESP	Input	The slave response transmission extension
TARGEXP0EXRESP	Input	The exclusive response transmission extension
TARGEXP0HRUSER[2:0]	Input	The user read-out data transmission extension
Initialization extension interface of AHB Lite INTEXP0		
INITEXP0HRDATA[31:0]	Output	Initialization of read-out data transmission extension
INITEXP0HREADY	Output	Initialization of normal indication transmission extension
INITEXP0HRESP	Output	Initialization of response transmission extension
INITEXP0EXRESP	Output	Initialization of exclusive response transmission extension
INITEXP0HRUSER[2:0]	Output	Initialization of the user read-out data transmission extension
INITEXP0HSEL	Input	Initialization of the selected signals transmission extension
INITEXP0HADDR[31:0]	Input	Initialization of the read/write address transmission extension
INITEXP0HTRANS[1:0]	Input	Initialization of transmission extension types
INITEXP0HWRITE	Input	Initialization of read/write enable transmission extension
INITEXP0HSIZE[2:0]	Input	Initialization of data width transmission extension
INITEXP0HBURST[2:0]	Input	Initialization of burst types setting transmission extension
INITEXP0HPROT[3:0]	Input	Initialization of protection types transmission extension
INITEXP0MEMATTR[1:0]	Input	Initialization of memory attributes transmission extension
INITEXP0EXREQ	Input	Initialization of exclusive request transmission extension
INITEXP0HMASTER[3:0]	Input	Initialization of master selection

Port Name	I/O	Description
		transmission extension
INITEXP0HWDATA[31:0]	Input	Initialization of written data transmission extension
INITEXP0HMASTLOCK	Input	Initialization of master locked signals transmission extension
INITEXP0HAUSER	Input	Initialization of user read/write address transmission extension
INITEXP0HWUSER	Input	Initialization of user's written data transmission extension
APB interface signal		
APBTARGEXP2PSTRB[3:0]	Output	APB transmission of write gate
APBTARGEXP2PPROT[2:0]	Output	APB transmission of protection types
APBTARGEXP2PSEL	Output	APB transmission of slave selection
APBTARGEXP2PENABLE	Output	The second clock cycle of APB transmission
APBTARGEXP2PADDR[11:0]	Output	APB transmission of write address
APBTARGEXP2PWRITE	Output	APB transmission of read/write enable
APBTARGEXP2PWDATA[31:0]	Output	APB transmission of the written data
APBTARGEXP2PRDATA[31:0]	Input	APB transmission of the readout data
APBTARGEXP2PREADY	Input	Pulled down if slave needs extra waiting
APBTARGEXP2PSLVERR	Input	SLVERR response
System reset response signal		

Port Name	I/O	Description
MTX_HRESET_N	Output	Automatically activated by SYSRESETN, indicating MCU to start from Flash
JTAG debug port signal		
DAPTDO	Output	JTAG data output
DAPJTAGNSW	Output	Output 1'b1，JTAG mode
DAPNTDOEN	Output	Control signals of JTAG data output pins
DAPSWDITMS	Input	JTAG status selection
DAPTDI	Input	JTAG data input
DAPNTRST	Input	JTAG reset signal
DAPSWCLKTCK	Input	JTAG clock signal
TRACE interface signal		
TPIUTRACEDATA[3:0]	Output	Trace output data
TPIUTRACECLK	Output	Trace output Clock
Interrupt request signal		
USER_INT0	Input	Flash error interrupt request
USER_INT1	Input	Flash interrupt request
Monitor signal of interrupt status		
INTMONITOR	Output	Monitor signal of peripherals interrupt

3.8 USB2.0 PHY

3.8.1 Features

GW1NSR-2 contains USB2.0 PHY, with the features as below:

- 480Mbps data speed, compatible with USB1.1 1.5/12Mbps data speed
- Plug and play
- Hot socket

3.8.2 Interfaces and Ports Signal

The USB2.0 PHY module includes UTMI+digital and UTMI+AFE (Analog Front End), which are mainly used to connect the USB controller and USB PHY.

Table 3-23USB2.0 PHY Ports Signal

Port Name	I/O	Description
CLK	O	Used for receiving and sending clock signals Data bit width is 8bit : 60MHz Data bit width is 16bit : 30MHz
RESET	I	Reset signal, active-high.
XCVRSEL	I	Transceiver select. This signal selects between the LS, FS, and HS transceivers: 2'b00: HS Transceiver 2'b01: FS Transceiver 2'b10: LS Transceiver 2'b11: Send a LS packet on a FS bus or receive a LS packet.
TERMSEL	I	Termination select. This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDM	I	Suspend.
LINESTATE[1:0]	O	Line state. These signals reflect the current state of the single ended receivers. 2'b00：SE0 2'b01：'J' state 2'b10：'K' state 2'b11：SE1
CLKSEL [1:0]	I	Operational mode. These signals select between various operational modes: 2'b00: Normal operation 2'b01：Non-driving 2'b10：Disable bit stuffing and NRZI encoding 2'b11：Normal operation without automatic generation of start and end signals
DP	IO	USB data pin
DM	IO	USB data pin
DATAIN[7:0]	I	Lower 8 bits USB sends data input
DATAIN[15:8]	I	Higher 8 bits USB sends data input
TXVLD	I	Lower 8 bits sends data enable signal, DATAIN[7:0] data valid indication
TXVLDH	I	Higher 8 bits sends data enable signal, DATAIN[15:8] data valid indication
TXREADY	O	Transmit data ready.
DATAOUT[7:0]	O	Lower 8 bits USB receives data output
DATAOUT[15:8]	O	Higher 8 bits USB receives data output
RXVLD	O	Lower 8 bits receives data enable signal, DATAIN[7:0] data valid indication
RXVLDH	O	Higher 8 bits receives data enable signal, DATAIN[15:8] data valid indication
RXACTIVE	O	Receive active. Indicates that the receive state machine has detected SYNC and is active.

Port Name	I/O	Description
RXERROR	O	Receive Error. High-level indicates that a receive error has been detected.
IDPULLUP	I	Signal that enables the sampling of the analog Id line, active-high.
IDDIG	O	Indicates whether the connected plug is a mini-A or mini-B. 0：mini-A 1：mini-B
SESSVLD	O	Indicates if the session for an A/B-peripheral is valid. 0：Vbus < 0.8V 1：Vbus > 2V
VBUSVLD	O	Indicates if the voltage on Vbus is at a valid level for operation (4.4V < Vth < 4.75V). 0：Vbus < 4.4V 1：Vbus > 4.75V
ADPSNS	O	Indicates the voltage on Vbus. 0：Vbus < 0.2 V 1：Vbus > 0.55V
ADP_PRBEN	I	Enables/disables the ADP Probe comparator. 1：enable 0：disable
ADPPRB	O	Indicates the voltage on Vbus. 0：Vbus < 0.6V 1：Vbus > 0.75V
CHARGVBUS	I	This signal enables charging Vbus. 0：do not charge Vbus through a resistor 1：charge Vbus through a resistor
DISCHARGEVBUS	I	This signal enables charging Vbus. 0: do not discharge Vbus through a resistor 1: discharge Vbus through a resistor
DPPD	I	This signal enables the 15k Ohm pull-down resistor on the DP line. 0: Pull-down resistor not connected to DP 1: Pull-down resistor connected to DP
DMPD	I	This signal enables the 15k Ohm pull-down resistor on the DM line. 0: Pull-down resistor not connected to DM 1: Pull-down resistor connected to DM
HOSTDIS	O	This signal is used for all types of peripherals connected to it. It is only valid when DPPD and DMPD are 1. 0: there is peripherals connected 1: there is no peripheral connected
TXBITSTUFFEN	I	Indicates if the data on the DataOut[7:0] lines needs to be bitstuffed or not. 0: Bitstuffing is disabled 1: Bitstuffing is enabled
TXBITSTUFFENH	I	Indicates if the data on the DataOut[15:8] lines needs to be bitstuffed or not.

Port Name	I/O	Description
		0: Bitstuffing is disabled 1: Bitstuffing is enabled
FSLSSERIAL	I	0: FS and LS packets are sent using the parallel interface. 1: FS and LS packets are sent using the serial interface.
TXENN	I	Active low enable signal. Only used when FSLSSERIAL is set to 1b.
TXDAT	I	Serial data. Only used when FSLSSERIAL is set to 1.
TXSE0	I	Force single-ended zero. Only used when FSLSSERIAL is set to 1.
RXDP	O	Single-ended receive data. This signal is only valid when FSLSSERIAL is set to 1.
RXDM	O	Single-ended receive data. This signal is only valid when FSLSSERIAL is set to 1.
RXRCV	O	Single-ended receive data. This signal is only valid when FSLSSERIAL is set to 1.
VBUS	IO	VBUS signal
ID	I	ID signal
XIN	I	Crystal in signals, supported range is 12MHZ~24MHZ.
XOUT	O	Crystal out signals
REXT	I	1% precision 12.7K pull-down register
LBKERR	O	0: no BIST error 1: Error during BIST occurs
INTCLK	I	Clock signals provided internally of the SoC.
CLKRDY	O	Observation/debug signal to show that the internal PLL has locked and is ready.
CLK480PAD	O	480 MHZ clock output for observation
Scan signals		
SCANCLK	I	Clock signals for scan mode
SCANEN	I	Select to shift mode
SCANMODE	I	High effective signal to enter scan mode
TRESETN	I	Low effective reset signal for scan mode.
SCANIN1	I	Scan chain input
SCANIN2	I	Scan chain input
SCANIN3	I	Scan chain input
SCANIN4	I	Scan chain input
SCANIN5	I	Scan chain input
SCANIN6	I	Scan chain input
SCANOUT1	O	Scan chain output
SCANOUT2	O	Scan chain output
SCANOUT3	O	Scan chain output

Port Name	I/O	Description
SCANOUT4	O	Scan chain output
SCANOUT5	O	Scan chain output
SCANOUT6	O	Scan chain output

Table 3-24USB2.0 PHY Parameters

Name	Description
DATABUS16_8	Selects between 8 bits and 16 bits data transfers. 1: 16 bits data path operation enabled. CLK is 30MHz. 0: 8 bits data path operation enabled. CLK is 60MHz.
ADP_PRBEN	Enables/disables the ADP probe comparator.
TEST_MODE[0]	Enables/disables BIST test
TEST_MODE[4] TEST_MODE[1]	BIST modes selection 2'b00：high speed BIST mode 2'b01：full speed BIST mode 2'b10：low speed BIST mode 2'b11：Low speed packet on FSBUS BIST
TEST_MODE[2]	0: 8 bits interface BIST 1: 16 bits interface BIST
TEST_MODE[3]	0: digital loop back BIST 1: analog loop back BIST
HSDRV1	High speed drive adjustment. Please connect to 0 for normal operation.
HSDRV0	High speed drive adjustment. Please connect to 0 for normal operation.
CLK_SEL	Source select for clock 0: external crystal oscillator XIN/XOUT 1：SoC internal clock INTCLK
M[3：0]	Used for test, M division factor, default value 0 0：1 frequency division 1：disabled 2：2 frequency division 3：3 frequency division ..... 15：15 frequency division
N[5：0]	Used for test, N division factor, default value 0 Supports 2 - 63 0 and 1: disabled 2：2 frequency division 3：3 frequency division ..... 63：63 frequency division
C[1：0]	Used for test, charge pump current control signal, default 40uA 2'b00：30uA 2'b01：40uA 2'b10：50uA 2'b11：60uA
FOC_LOCK	Used for test, default 0

Name	Description
	0: LOCK is generated by PLL lock detector 1: LOCK is always high(always lock)

3.9 ADC

3.9.1 Features

GW1NSR series of FPGA products integrate an eight-channel single-ended 12 bits SAR ADC. It is a medium-speed ADC with low-power, low-leakage current, and high-speed.

The dynamic performance is as below:

- Slew Rate: Max. 1MHz
- Dynamic range: >81 dB SFDR，>62 db SINAD
- Linear performance: INL<1 LSB, DNL<0.5 LSB, no missing codes

3.9.2 Port Signal

Table 3-25 ADC Port Signal

Port Name	I/O	Description
CLK	I	Clock input signal. fclk is greater than or equal to 16 times of sampling frequency Max. Clock frequency: 16MHz
PD	I	Power down signal, output 0 when the signal value is 1.
SoC	I	Sampling frequency, max. Frequency is 1MHz.
S[2：0]	I	Channel selection signal
CH[7:0]	I	Eight-channel analog input
EOC	O	End conversion.
B[11：0]	O	A/D conversion result

Table 3-26 Channel Selection Truth Table

S[2：0]	Selected Input Channel
3’b111	CH[7]
3’b110	CH[6]
3’b101	CH[5]
3’b100	CH[4]
3’b011	CH[3]
3’b010	CH[2]
3’b001	CH[1]
3’b000	CH[0]

3.10 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. GW1NSR series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW1NSR series of FPGA products provide high-speed clock HCLK. PLL, DLL, etc are also provided .

3.10.1 Global Clock

The GCLK is distributed in GW1NSR devices as four quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

Figure3-42 GW1NSR-2 Clock Resources

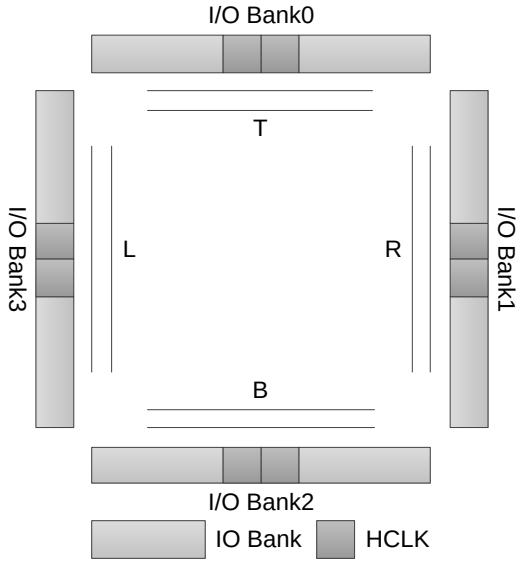
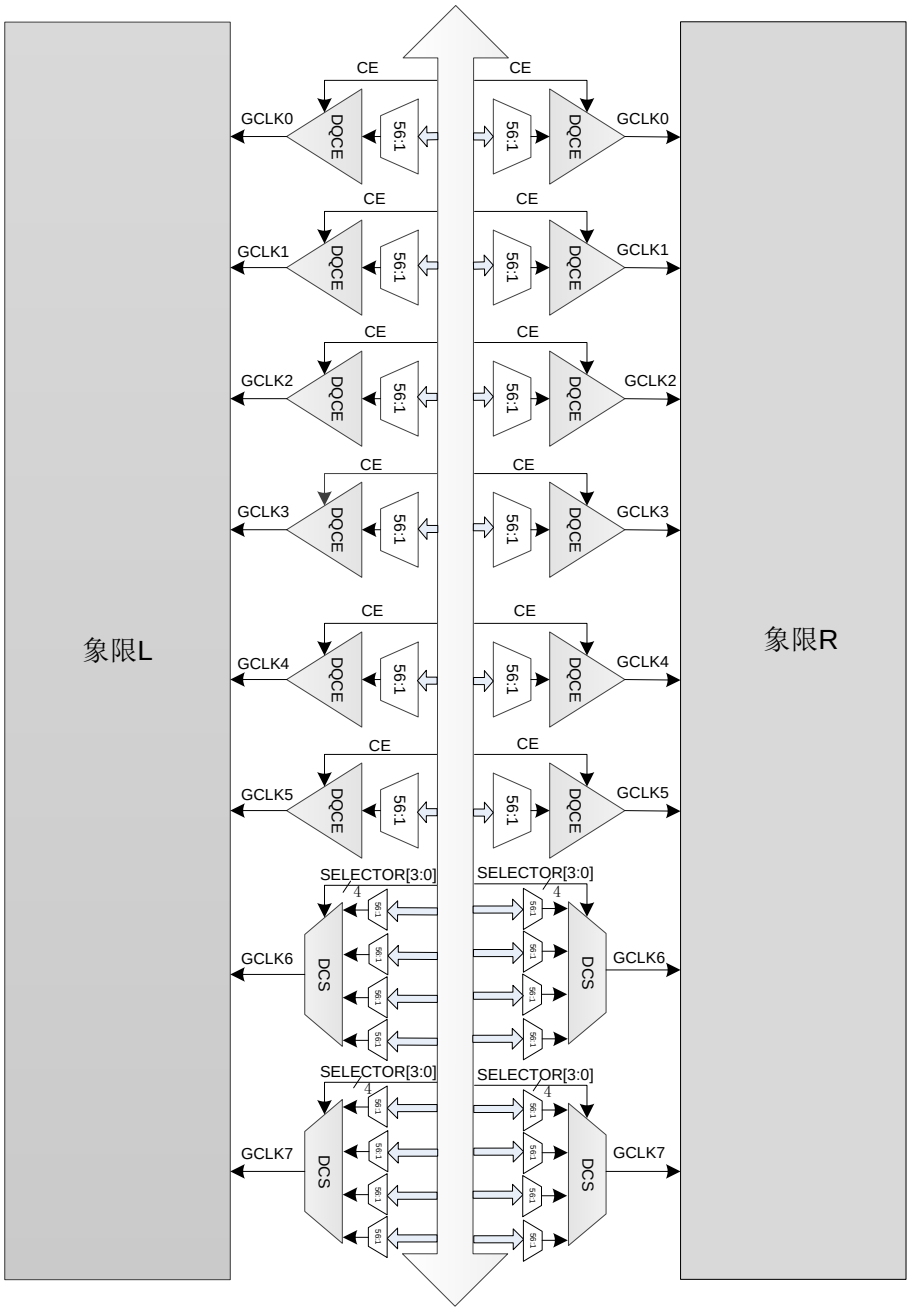
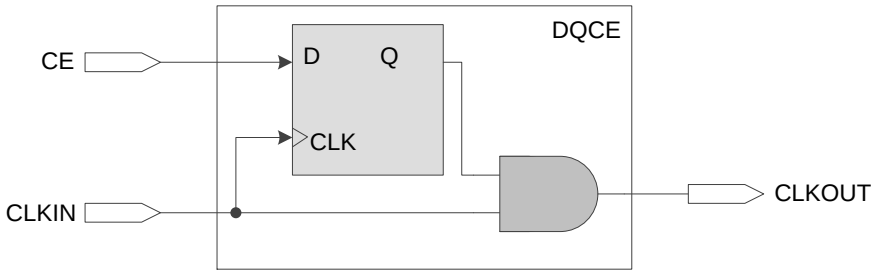


Figure 3-43 GCLK Quadrant Distribution



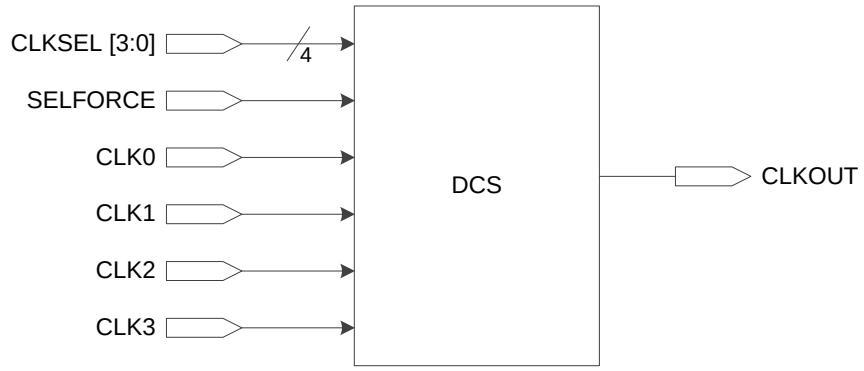
GCLK0~GCLK5 can be turned on or off by Dynamic Quadrant Clock Enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

Figure 3-44 DQCE Concept



GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-45. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

Figure 3-45 DCS Concept

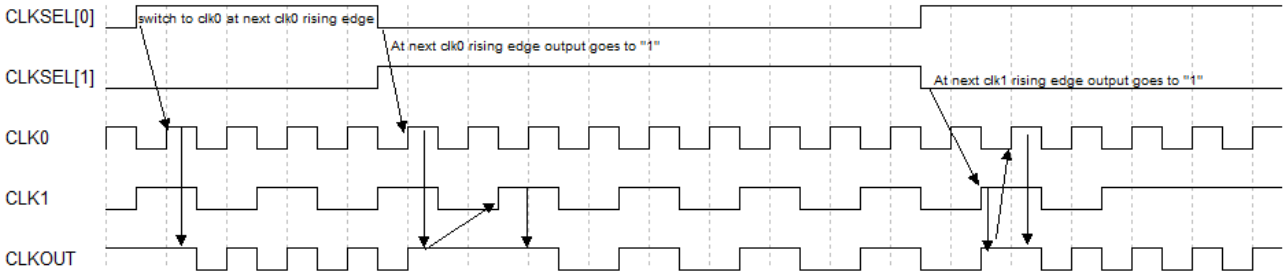


DCS can be configured in the following modes:

1. DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-46.

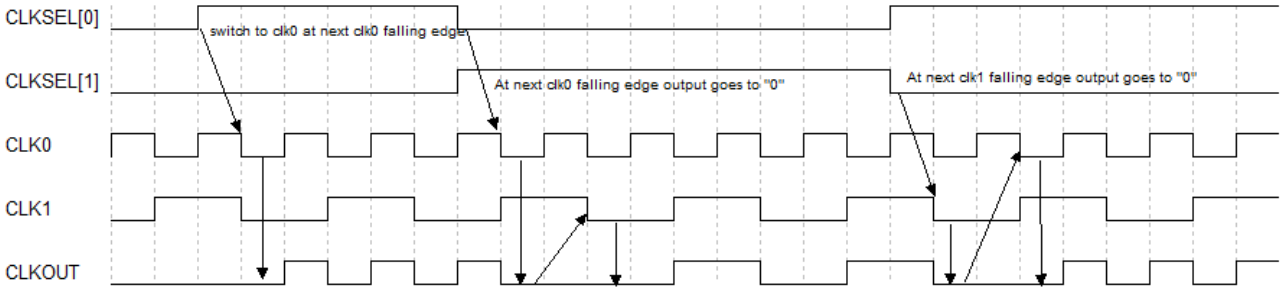
Figure 3-46 DCS Rising Edge



2. DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-47.

Figure 3-47 DCS Falling Edge



3. Clock Buffer Mode

In this mode, DCS acts as a clock buffer.

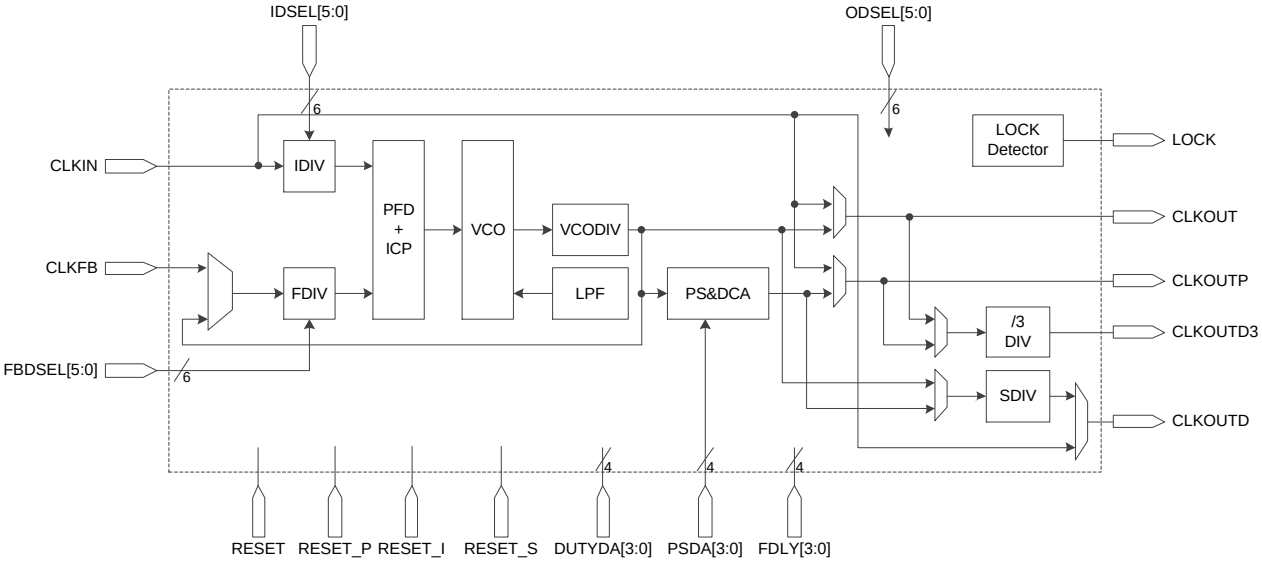
3.10.2 PLL

Phase-locked Loop (PLL) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-48 for the PLL structure.

Figure 3-48 PLL Structure



The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

PLL features are as follows:

- Input frequency:3MHz~450MHz
- VCO vibration frequency: 400MHz~1500MHz
- CLKOUT output frequency: 3.125MHz~750MHz

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1. $f_{CLKOUT} = (f_{CLKIN}*FDIV)/IDIV$
2. $f_{VCO} = f_{CLKOUT}*ODIV$
3. $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
4. $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FDIV$

Note!

- f_{CLKIN}: The frequency of the input clock CLKIN
- f_{CLKOUT}: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD}: PFD Phase Comparison Frequency

Adjust IDIV, FDIV, ODIV, and SDIV to achieve the required clock frequency.

See Table 3-27 for a definition of the PLL ports.

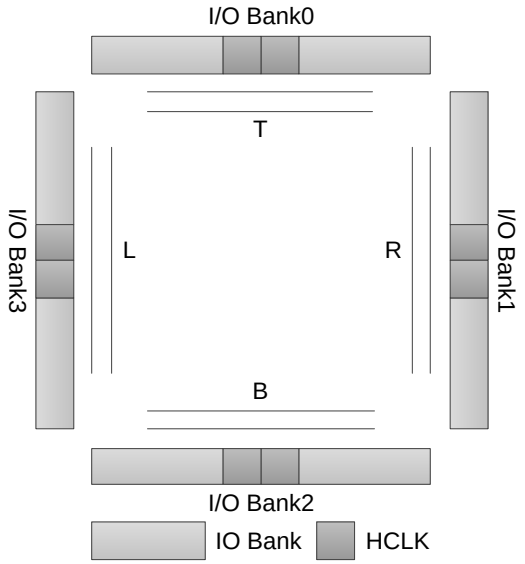
Table 3-27 Definition of the PLL Ports

Port Name	Signal	Description
CLKIN [5：0]	Input	Reference clock input
CLKFB	Input	Feedback clock input
RESET	Input	PLL reset
RESET_P	Input	PLL Power Down
RESET_I	Input	IDIV reset
RESET_S	Input	SDIV and DIV3 reset
IDSEL [5：0]	Input	Dynamic IDIV control: 1~64
FBDSEL [5：0]	Input	Dynamic FDIV control:1~64
PSDA [3：0]	Input	Dynamic phase control (rising edge effective)
DUTYDA [3：0]	Input	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	Input	CLKOUTP dynamic delay control
CLKOUT	Output	Clock output with no phase and duty cycle adjustment
CLKOUTP	Output	Clock output with phase and duty cycle adjustment
CLKOUTD	Output	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	Output	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	Output	PLL lock status: 1: locked, 0: unlocked

3.10.3 HCLK

HCLK is the high-speed clock in the GW1NSR series of FPGA products. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure Figure 3-49.

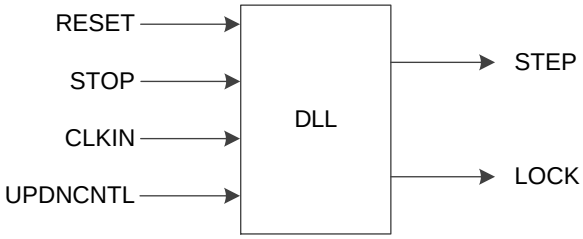
Figure 3-49 GW1NSR-2/GW1NSR-2C HCLK Distribution



3.10.4 DLL

The GW1NSR series of FPGA products support DLL. For DLL function, see Figure 3-50.

Figure 3-50 GW1NSR-2 DLL Function



The source of CLKIN can come from GCLK and the neighboring HCLK.

The calculated STEP will be sent to the four BANKs. At the same time, the signal STEP can also be sent to user logic through the CRU.

3.11 Long Wire (LW)

As a supplement to the CRU, the GW1NSR series of FPGA products provides another routing resource, Long wire, which can be used as clock, clock enable, set/reset,or other high fan out signals.

3.12 Global Set/Reset (GSR)

A global set/rest (GSR) network is built into the GW1NSR series of FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset, registers in CFU and I/O can be configured independently.

3.13 Programming Configuration

The GW1NSR series of FPGA products support SRAM and Flash. Flash programming mode supports on-chip Flash and off-chip Flash. GW1NSR series support on-chip DUAL BOOT, providing a selection for users to backup data to off-chip Flash according to requirements.

Besides JTAG, the GW1NSR series of FPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For more detailed information, please refer to *Gowin series FPGA Products Programming and Configuration User Guide*.

3.13.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the device.

3.13.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the

Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”. The GW1NSR series of FPGA products also support off-chip Flash configuration and dual-boot. Please refer to *Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

3.14 On Chip Oscillator

There is an internal oscillator in each of the GW1NSR series of FPGA product. This provides programmable user clock with clock precision ±5%. During the configuration process, it can provide a clock for MSPI mode. There is an internal oscillator in each of the GW1NSR series of FPGA product. During the configuration process, it can provide a clock for the MSPI mode. See Table 328 for the output frequency.

Table 328 GW1NSR-2 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.5MHz	16	15.0MHz
1	5.4MHz	9	8.0MHz	17	17.1MHz
2	5.7MHz	10	8.6MHz	18	20.0MHz
3	6.0MHz	11	9.2MHz	19	24.0MHz
4	6.3MHz	12	10.0MHz	20	30.0MHz
5	6.6MHz	13	10.9MHz	21	40.0MHz
6	6.9MHz	14	12.0MHz	22	60.0MHz
7	7.4MHz	15	13.3MHz	23	120MHz[2]

Note!

- [1] Default frequency
- [2] 125MHz is not suitable for MSPI.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is employed to get the output clock frequency:f_{out}=240 MHz/Param.

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

4 AC/DC Characteristic

Note!

Please ensure that you use GOWINSEMI devices within the recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate normally beyond the operating conditions and range.

4.1 Operating Conditions

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage	-0.5V	1.32V
V_{CCOx}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	LX Auxiliary voltage	-0.5V	1.98V
	UX Auxiliary voltage	-0.5V	3.75V
Operating Temperature (Industrial)	Operating Temperature	-40 ℃	+125 ℃
Storage Temperature	Storage Temperature	-65 ℃	+150 ℃

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	Core voltage	1.14V	1.26V
V_{CCX}	LX Auxiliary voltage	1.71V	1.89V
	UX Auxiliary voltage	2.375V	3.465V
V_{CCOx}	I/O Bank Power	1.14V	3.465V
T_{JCOM}	Junction temperature Commercial operation (Junction temperature Commercial operation)	0 ℃	+85 ℃
T_{JIND}	Junction temperature Industrial operation (Junction temperature Commercial operation)	-40 ℃	+100 ℃
T_{RAMP}	Power supply ramp rates for all power supplies (Power supply ramp rates for all power supplies)	0.01mV/μs	10mV/μs

Note!

- For the power supply information for different packages, please refer to *GW1NSR-2&2C Pinout*.

Table 4-3 Hot Socket Specifications

Name	Description	Condition	Max.
I_{HS}	Input or I/O leakage current (Input or I/O leakage current)	$V_{IN}=V_{IL}$ (MAX)	TBD

4.2 ESD

Table 4-4 GW1NSR ESD - HBM

Device	CS36	QN32	QN48	LQ144
GW1NSR-2C	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V
GW1NSR-2	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V

Table 4-5 GW1NSR ESD - CDM

Device	QN48
GW1NSR-2C	CDM>500V
GW1NSR-2	CDM>500V

Table 4-6 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$ (MAX)	-	-	210μA
		$0V<V_{IN}<V_{CCO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current (I/O Active Pull-up Current)	$0<V_{IN}<0.7V_{CCO}$	-30 μA	-	-150 μA
I_{PD}	I/O Active Pull-down Current (I/O Active Pull-up Current)	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current (Bus Hold Low Sustaining Current)	$V_{IN}=V_{IL}$ (MAX)	30μA	-	-
I_{BHHO}	Bus Hold High Sustaining Current (Bus Hold Low Sustaining Current)	$V_{IN}=0.7V_{CCO}$	-30 μA	-	-
I_{BHLO}	Bud HoldLow Overdrive Current (Bus Hold Low Sustaining Current)	$0≤V_{IN}≤V_{CCO}$	-	-	150μA
I_{BHHO}	Bus HoldHigh Overdrive Current	$0≤V_{IN}≤V_{CCO}$	-	-	-150 μA
V_{BHT}	Bus hold trip points		V_{IL} (MAX)	-	V_{IH} (MIN)
C1	I/O Capacitance (I/O Capacitance)			5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigge inputs	V_{CCO}=3.3V, Hysteresis= Large	-	482mV	-
		V_{CCO}=2.5V, Hysteresis= Large	-	302mV	-
		V_{CCO}=1.8V, Hysteresis= Large	-	152mV	-
		V_{CCO}=1.5V, Hysteresis= Large	-	94mV	-
		V_{CCO}=3.3V, Hysteresis= Small	-	240mV	-
		V_{CCO}=2.5V, Hysteresis= Small	-	150mV	-
		V_{CCO}=1.8V, Hysteresis= Small	-	75mV	-
		V_{CCO}=1.5V, Hysteresis= Small	-	47mV	-

Table 4-7 Static Supply Current

Name	Description	LV/UV	Device	Min.	Typ.	Max.
I_{CC}	Core current V_{CCX}=3.3V, V_{CCX}=2.5V	UX	GW1NSR-2	TBD	TBD	TBD
I_{CCX}	V_{CCX} current（V_{CCX}=3.3V)	UX	GW1NSR-2	TBD	TBD	TBD
	V_{CCX} current（V_{CCX}=2.5V)	UX	GW1NSR-2	TBD	TBD	TBD
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	UX	GW1NSR-2	TBD	TBD	TBD
I_{CC}	Core current under load（V_{CCX}=3.3V）	UX	GW1NSR-2	TBD	TBD	TBD
I_{CCX}	Core current under load（VCCX=3.3V）	UX	GW1NSR-2	TBD	TBD	TBD
I_{CCO}	I/O Bank current under load(V_{CCO}=2.5V)	UX	GW1NSR-2	TBD	TBD	TBD

4.3 DC Characteristic

Table 4-8 Recommended I/O Operating Conditions

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Table 4-9 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Table 4-10 I/O Differential Electrical Characteristics

LVDS25

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage (Input Voltage)		0	-	2.4	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	-	mV
I_{IN}	Input Current	Power On or Power Off	-	-	± 10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristic

4.4.1 Internal Switching Characteristics

Table 4-11 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{LUT5_CFU}	LUT5 delay	-	1.388	ns
t_{LUT6_CFU}	LUT6 delay	-	2.01	ns
t_{LUT7_CFU}	LUT7 delay	-	2.632	ns
t_{LUT8_CFU}	LUT8 delay	-	3.254	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

Table 4-12 B-SRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

Table 4-13 DSP Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from output register	-	4.80	ns
t_{COPR_DSP}	Clock to output from output register	-	2.40	ns
t_{COOR_DSP}	Clock to output from output register	-	0.84	ns

Table 4-14GearboxInternal Timing Parameters

Name	Description	Typ.	Unit
FMAXIDDR	2:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IDES4}$	4:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IDES8}$	8:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IVIDEO}$	7:1 Gearbox maximum input frequency	390	MHz
$FMAX_{IDES10}$	10:1 Gearbox maximum input frequency	410	MHz
$FMAX_{ODDR}$	1:2 Gearbox maximum input frequency	355	MHz
$FMAX_{OSER4}$	1:4 Gearbox maximum input frequency	360	MHz
$FMAX_{OSER8}$	1:8 Gearbox maximum input frequency	355	MHz
$FMAX_{OVIDEO}$	1:7 Gearbox maximum input frequency	355	MHz
$FMAX_{OSER10}$	1:10 Gearbox maximum input frequency	355	MHz

4.4.2 External Switching Characteristics

Table 4-15 LUT External Switching Characteristics

Name	Description	Device	-5		-6		Unit
			Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	

Table 4-16IO Parameters

Name	Description		Min	Max	Unit
f_{MAX}	IO Max. Frequency	GW1NSR-2/ GW1NSR-2 C	-	150M	Hz
f_{MAX_LVDS}	LVDS Max. Frequency	GW1NSR-2/ GW1NSR-2 C	-	400M	Hz

Table 4-17 On chip Oscillator Output Frequency

Name	Description		Min.	Typ.	Max.
f_{MAX}	On chip Oscillator Output Frequency (0 ~ +85℃)	GW1NSR-2/GW1NSR-2C	114MHz	120MHz	126MHz
	On chip Oscillator Output Frequency (-40 ~ +100℃)	GW1NSR-2/GW1NSR-2C	108MHz	120MHz	132MHz
t_{DT}	Clock Duty Cycle		43%	50%	57%
t_{OPJIT}	Clock Period Jitter		0.01UIPP	0.012UIPP	0.02UIPP

Table4-18 PLL Parameters

Name	Description	Min.	Typ.	Max.
F_{in}	Input clock frequency	3MHz	-	450MHz
F_{out}	Output clock frequency	Fvco/128	-	Fvco/2
F_{vco}	Voltage-controlled oscillator clock frequency	400MHz	-	1500MHz
t_{DT}	Output Clock Duty Cycle	-	$0.0625T_{pll}$	
T_{PAS}	Phase adjustment step	-	$0.0625T_{pll}$	

4.5 Cortex-M3 Electrical Specification

4.5.1 DC Characteristic

Table 4-19 Current Characteristic

Name	Description	Spec.		Unit
		Min.	Max.	
I_{VCC}	Max. current of VCC	-	100	mA
I_{VSS}	Max. current of VSS	-	⩾100	mA
I_{INJ}	Leakage current	-	+/-5	mA

4.5.2 AC Characteristic

Table 4-20 Clock Parameters

Name	Description	Spec.		Unit
		Min.	Max.	
f_{HCLK}	AHB clock frequency	0	30	MHz
f_{PCLK}	APB clock frequency	0	70	MHz

4.6 User Flash Characteristic

4.6.1 DC Characteristic

Table 4-21 User Flash DC Characteristic

Name	Description	Spec.		Unit
		Min.	Max.	
$IVCC_{read}$	V_{CC} read operation current	-	1.4	mA
$IVCCX_{read}$	V_{CCX} read operation current	-	0.6	mA
$IVCC_{prog}$	V_{CC} write operation current	-	0.2	mA
$IVCCX_{prog}$	V_{CCX} write operation current	-	2.2	mA
$IVCC_{erase}$	V_{CC} erase operation current	-	0.2	mA
$IVCCX_{erase}$	V_{CCX} erase operation current	-	2.3	mA
$I_{IDLE-VCC}$	V_{CC} IDLE current	-	10	uA
$I_{IDLE-VCCX}$	V_{CCX} IDLE current	-	100	uA
I_{LI}	Input leakage current	-	0.1	uA
I_{LO}	Output leakage current	-	0.1	uA
V_{VREF}	Before setting configuration register.	1.14	1.26	V
	After setting configuration register.	1.176	1.224	V
V_{VREF1V}	Before setting configuration register.	0.94	1.06	V
	After setting configuration register.	0.97	1.03	V
V_{IL}	Input low level	-	$0.1*V_{CC}$	V
V_{IH}	Input high level	$0.9*V_{CC}$	-	V
V_{OL}	Output low level	-	$0.1*V_{CC}$	V
V_{OH}	Output high level	$0.9*V_{CC}$	-	V
t_{PROG}	Write operation time	-	30	us
t_{SER}	Page erasure time	-	2	mA
t_{MER}	Macro erasure time	-	10	mA

4.6.2 AC Characteristic

Table 4-22 User Flash Timing Parameters

Name	Description	Spec.		Unit
		Min.	Max.	
tAS	Address set up time	2	-	ns
tHS	Address hold-up time	2	-	ns
tS	Write and erase setup time	5	-	ns
tH	Write and erase hold time	5	-	ns
tDS	Data set up time	5	-	ns
tDH	Data hold-up time	5	-	ns
tAC	Data read time	-	30	ns
tACR		-	80	ns
tHZ	Time from high resistance to OE turning low	3	-	ns
tAE	High-level time of AE	10	-	ns
tAEL	Low-level time of AE	10	-	ns
tAAD	Delay time from AE to AE during read operation	30	-	ns
tAADR	Delay time from AE to AE in readback state	80	-	ns
tTR	Time of TBIT rising edge after NVSTR rising edge	-	100	ns
tTF	Time from NVSTR rising edge to IBIT falling edge during write operation	-	30	us
tTF	Time from NVSTR rising edge to IBIT falling edge during page erasure operation	-	2	ms
tTF	Time from NVSTR rising edge to IBIT falling edge during macro erasure operation	-	10	ms
tNVSTRH	Hold time from NVSTR rising edge to AE rising edge	10	-	ns
tNVSTRL	Hold time from NVSTR rising edge to IBIT falling edge	50	-	ns
tCS	CS setup time	10	-	ns
tRCH	CS hold-up time during read operation	0	-	ns
tWCH	CS hold-up time during write operation	10	-	ns
tECH	CS hold-up time during erasure operation	10	-	ns
tDOH	Time from AE enabled to data output time	5	-	ns
tOS	Read enable setup time	1	-	ns
tOH	Read enable hold-up time	30	-	ns
tOHR	Read enable hold-up time	80	-	ns

4.6.3 Operation Timing Diagrams

Figure 4-1 Read Mode

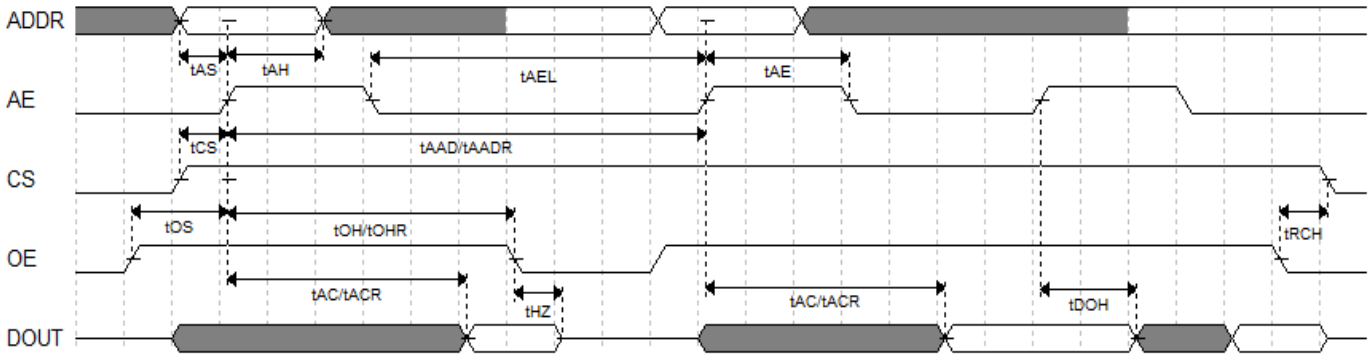


Figure 4-2 Write Mode

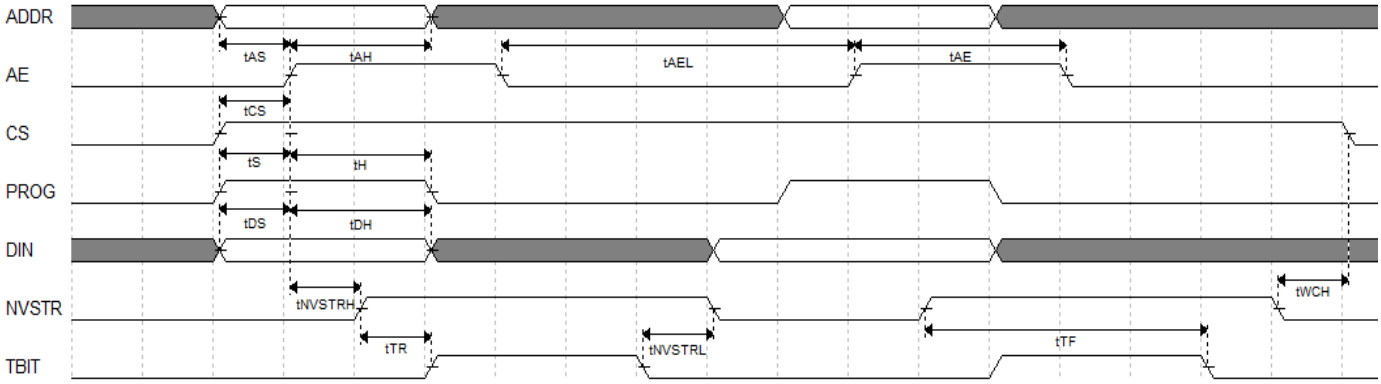


Figure 4-3 Page Erasure Mode

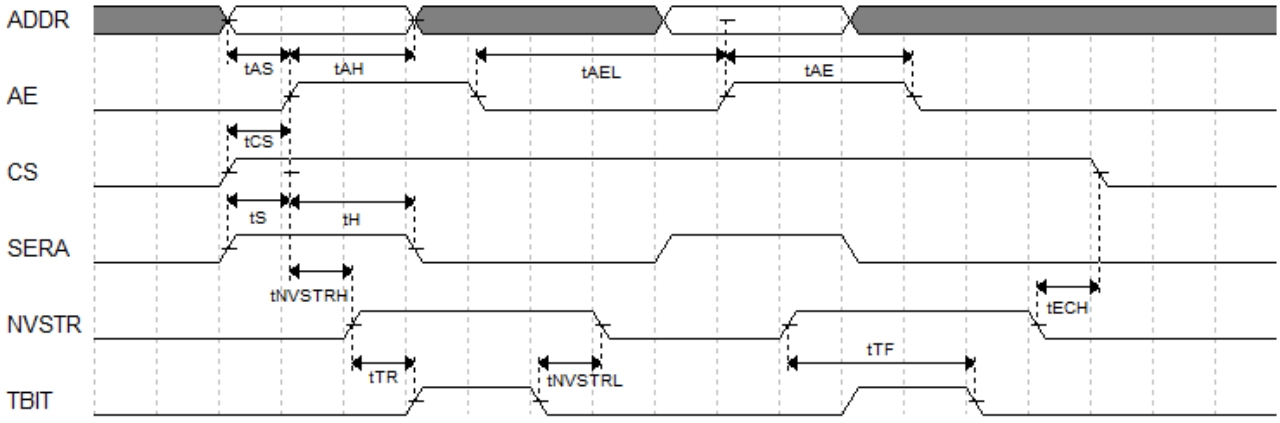
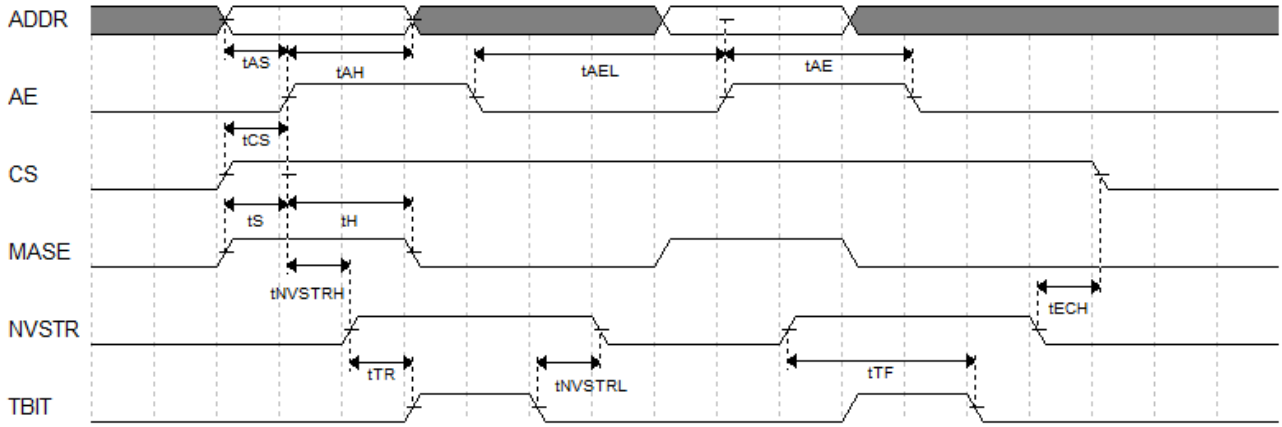


Figure 4-4 Module Rrasure Mode



4.7 ADC Characteristics

4.7.1 ADC Timing

In total, 16 clock cycles are needed for ADC to sample analog input signals and convert them to output digital signals. The first four clock cycles are used to sample and hold; the latter twelve clock cycles are used for the SAR algorithm to generate the required output signals. If the ECO signal becomes high at the 16th clock cycle, the conversion is complete, and the converted digital data will output at the EOC rising edge.

Figure 4-5ADC Timing

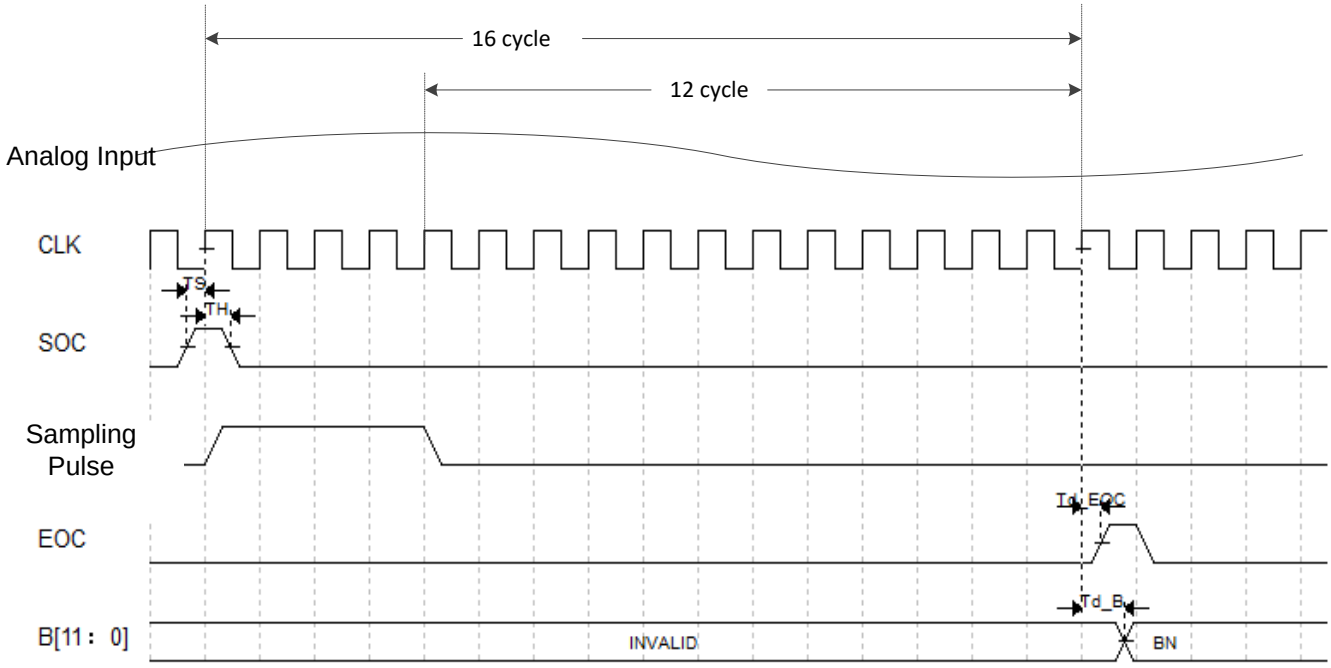


Table 4-23 ADC Timing Parameters

Name	Description	Spec.		Unit
		Min.	Max.	
CLK	Clock cycle	62.5	-	ns
T_S	SOCsetup time	0	-	ns
T_H	SOC hold-up time	10	-	ns
T_{D_EOC}	EOC delay time	-	13.5	ns
T_{D_B}	Data-out delay time	-	16	ns

4.7.2 Electrical Characteristic Parameters

Table 4-24ADC Parameters

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
DC Precision					
Output	Data output bits		12		bit
INL	Integral nonlinearity		+/- 0.84		LSB
DNL	Differential nonlinearity		+/- 0.46		LSB
Offset error	Offset error		0.45		%FS
Gain error	Gain error		0.02		%FS
Analog Input					
CH[7：0]	Single-ended input range	0.01*VREF		0.99*VREF	V
CIN	Input capacitance		11.52		pF
Slew Rate					
SoC	Sample frequency			1	MHz
CLK	Main clock			16	MHz
Date-out delay	Date-out delay		12		Clock cycle
Dynamic Characteristic Parameters					
SINAD	Signal Noise Ratio		64.8(Fin=1.47K)		DB
			62.6(Fin=107K)		DB
SFDR	Spurious-free dynamic range		84.9(Fin=1.47K)		DB
			81.7(Fin=107K)		DB
HD2	Second harmonic distortion		-104(Fin=1.47K)		DB
			-87.1(Fin=107K)		DB
HD3	Third harmonic distortion		-94.1(Fin=1.47K)		DB
			-80.6(Fin=107K)		DB
THD	Total harmonic distortion (Fifth)		-87.2(Fin=1.47K)		DB
			-79.3(Fin=107K)		DB
ENOB	Valid data-out bits		10.5(Fin=1.47K)		bit
			10.1(Fin=107K)		bit

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
Reference Voltage					
VREF	Reference Voltage	0.5*V_{CCO0}		V_{CCO0}	V
Digital Input					
V_{IH}	Input high level	0.7*V_{CC}	V_{CC}		V
V_{IL}	Input low level		0	0.3*V_{CC}	V
Digital output B[11：0]					
V_{OH}	Output high level	0.7*V_{CC}			V
V_{OL}	Output low level			0.3*V_{CC}	V
Supply voltage					
V_{CCO0}	Analog/digital voltage	2.97	3.3	3.63	V
V_{CC}	Digital voltage	1.08	1.2	1.32	V
I_{VCCO0}	Analog/digital current		750(Fin=107K)		uA
I_{VCC}	Digital current		4(Fin=107K)		uA
I_{pd}	Turning off current		0.15		mA

4.8 Configuration Interface Timing Specification

The GW1NSR series of FPGA products GowinCONFIG support six configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For detailed information, please refer to *Gowin FPGA Products Programming and Configuration* User Guide.

4.8.1 JTAG Port Timing Specifications

The JTAG mode of the GW1NSR series of FPGA products complies with IEEE1532 and IEEE1149.1 boundary scan standards.

JTAG mode downloads the bitstream to SRAM, and the data is lost after power off.

See Figure 4-6 for JTAG timing.

Figure 4-6 JTAG Timing

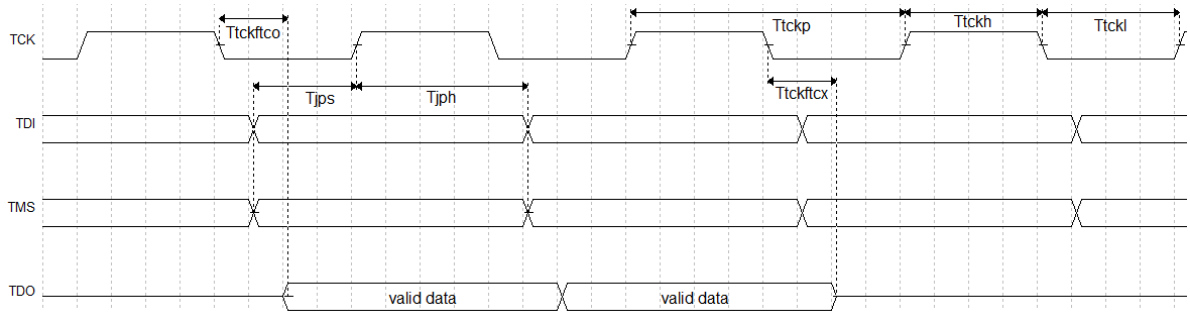


Table 4 - 25 JTAG Timing Parameters

Name	Description	Min.	Max.
$T_{tckftco}$	Time from TCK falling edge to output		10ns
$T_{tckftcx}$	Time from TCK falling edge to high impedance		10ns
T_{tckp}	TCK clock period	40ns	-
T_{tckh}	TCK clock high time	20ns	-
T_{tckl}	TCK clock low time	20ns	-
T_{jps}	JTAG PORT setup time	10ns	
T_{jph}	JTAG PORT hold time	8ns	

Other than the power requirements, the following conditions need to be met to use the MSPI configuration mode:

- MSPI port enable

Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.

- Initiate new program

Power-up again or provide one low pulse for programming pin RECONFIG_N.

4.8.2 AUTO BOOT Port Timing Specifications

The AUTOBOOT mode offers instant-on feature for the GW1NSR series of FPGA products. In this mode, FPGA reads data from the on-chip Flash directly for the program to load after the chip is powered on.

On-chip Flash is configured via the JTAG interface. After the configuration, RECONFIG_N is triggered by a low level pulse, or auto boot configuration starts after power recycle. Figure 4-7 shows the timing.

Figure 4-7 Power Recycle Timing

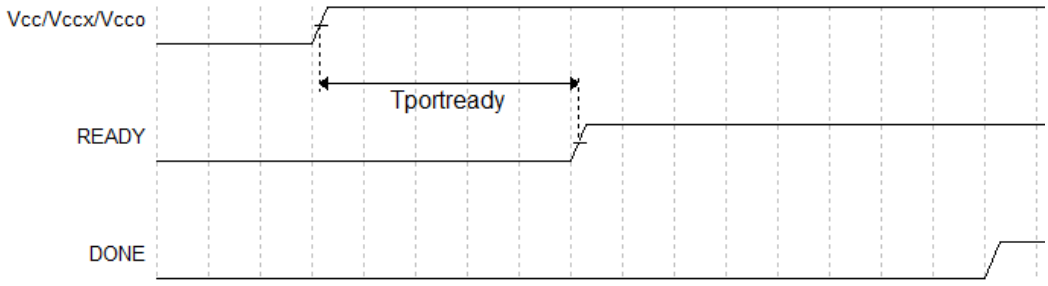


Figure 4-8 RECONFIG_N Trigger Timing

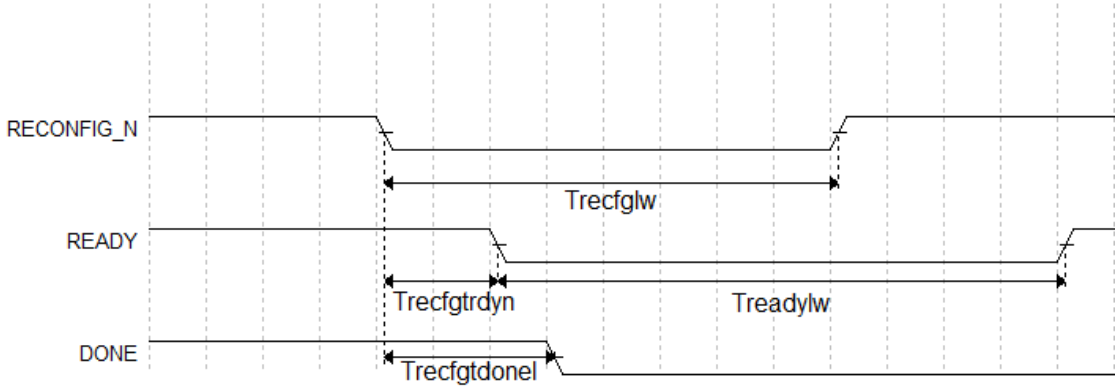


Table 4-26 shows the timing parameters.

Table 4-26 Parameters for Power Recycle and RECONFIG_N Trigger Timing

Name	Description	Min.	Max.
$T_{portready}$ [1]	Time from application of V_{CC}, V_{CCX} and V_{CCO} to the rising edge of READY	50μs	200μs
$T_{recfglw}$	RECONFIG_N low pulse width	25ns	
$T_{recfgtrdyn}$	Time from RECONFIG_N falling edge to READY low	-	70ns
$T_{readylw}$	READY low pulse width	TBD	
$T_{recfgtdonel}$	Time from RECONFIG_N falling edge to DONE low	-	80ns

Note!

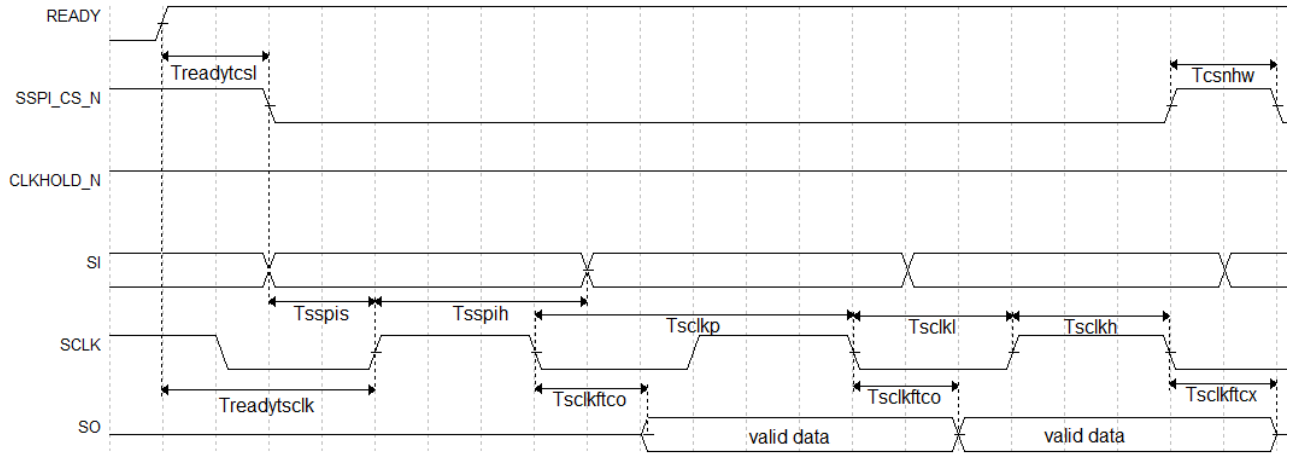
In the case of MODE0=0, the device power-up waiting time is 200 μs; For MODE0=1, the device power-up waiting time is 50 μs.

4.8.3 SSPI Port Timing Specifications

In the SSPI mode, the GW1NSR series of FPGA products are configured by the hardware processor via SPI.

See Figure 4-9 for the SSPI timing diagram.

Figure 4-9 SSPI Timing Diagram



See Table 4-27 for the timing parameters.

Table 4-27 Timing Parameters

Name	Description	Min.	Max.
T_{sclkp}	SCLK clock period	15ns	-
T_{sclkh}	SCLK clock high time	7.5ns	-
T_{sclkl}	SCLK clock low time	7.5ns	-
T_{sspis}	SSPI PORT setup time	2ns	-
T_{sspih}	SSPI PORT hold time	0ns	-
$T_{sclkftco}$	Time from SCLK falling edge to output	-	10ns
$T_{sclkftcx}$	Time from SCLK falling edge to high impedance	-	10ns
T_{csnhw}	CSN high time	25ns	-
$T_{readytcsl}$	Time from READY rising edge to CSN low		
$T_{readytsclk}$	Time from READY rising edge to first SCLK edge	TBD	-

Other than the power requirements, the following conditions need to be met to use the SSPI configuration mode:

- SSPI port enabled

Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.

- Initiate new program

Power-up again or provide one low pulse for programming pin RECONFIG_N.

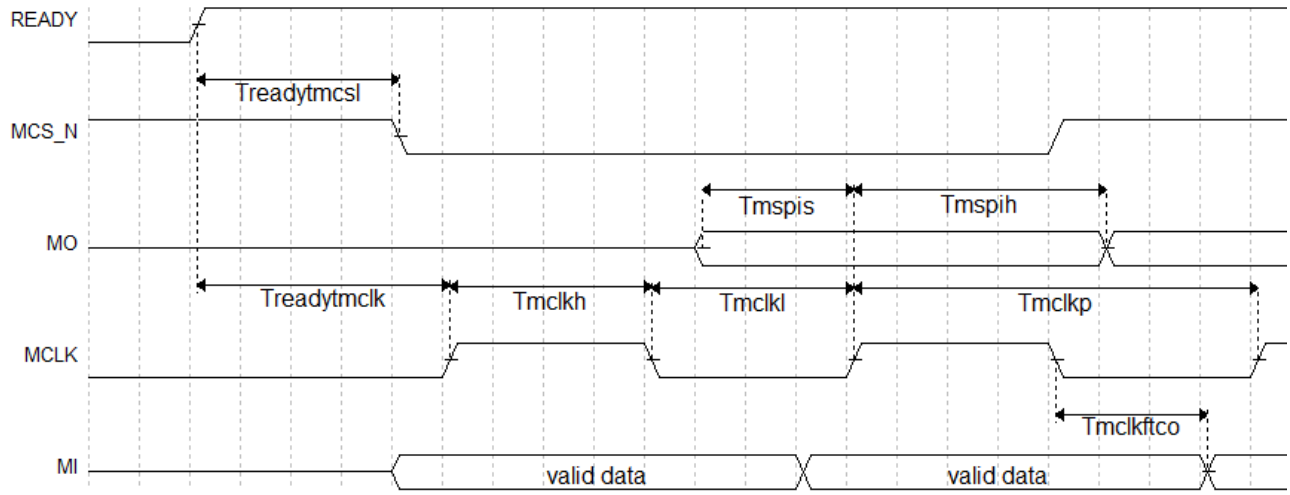
4.8.4 MSPI Port Timing Specifications

In master MSPI mode, the configuration data is retrieved automatically from the off chip SPI Flash. The default MCLK frequency of the GW1NSR-2 and GW1NSR-2C is 2.1 MHz. The MCLK accuracy is +/- 5%.

After MSPI writes the configuration data to the off-chip Flash, power recycle or RECONFIG_N will trigger device configuration. GW1NSR-2 and GW1NSR-2C only support one auto MSPI configuration; if this fails, power recycle or RECONFIG_N will trigger the device configuration again.

See Figure 4-10 for the MSPI Timing Diagram.

Figure 4-10 MSPI Timing Diagram



See Table 4-28 for the MSPI timing diagram.

Table 4-28 MSPI Timing Parameters

Name	Description	Min.	Max.
T_{mclkp}	MCLK clock period	15ns	-
T_{mclkh}	MCLK clock high time	7.5ns	-
T_{mclkl}	MCLK clock low time	7.5ns	-
T_{mspis}	MSPI PORT setup time	5ns	-
T_{mspih}	MSPI PORT hold time	1ns	-
$T_{mclkftco}$	Time from MCLK falling edge to output	-	10ns
$T_{readytmcsl}$	Time from READY rising edge to MCS_N low	100ns	200ns
$T_{readytmclk}$	Time from READY rising edge to first MCLK edge	2.8μs	4.4μs

4.8.5 DUAL BOOT

DUAL BOOT supports two modes of configuration: When Mode is "100", GW1NS-R2 and GW1NSR-2C preferentially choose to start from the User Flash. When the User Flash fails to configure, the device chooses to read data from the built-in Flash for configuration.

In addition, when the Mode is "110", GW1NSR series of FPGA products preferentially choose to start from the external Flash. When the external Flash fails to configure, the device chooses to read the data stored on the built-in Flash for configuration. When the external Flash is empty, the device will not be configured.

4.8.6 CPU

In CPU mode, the GW1NSR series of FPGA products are configured by hardware processor via DBUS interface. Other than the power requirements, the following conditions need to be met to use the CPU configuration mode:

- CPU port enable

Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.

- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.8.7 SERIAL

In SERIAL mode, the GW1NSR series FPGA products are configured by the hardware processor via serial interface. Other than the power requirements, the following conditions need to be met to use the SERIAL configuration mode:

- SERIAL port enable
  Set RECONFIG_N as “NON-RECOVERY″for the first programming activity after power-up or the previous programming activity.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

5 Ordering Information

5.1 Part Name

Figure 5-1 GW1NSR-2 Part Naming–ES

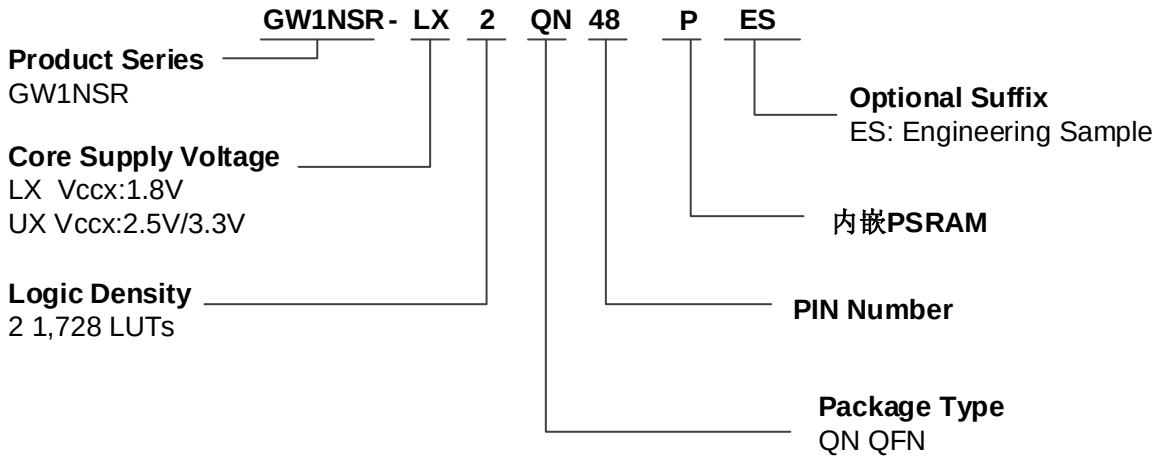


Figure 5-2 GW1NSR-2C Part Naming–ES

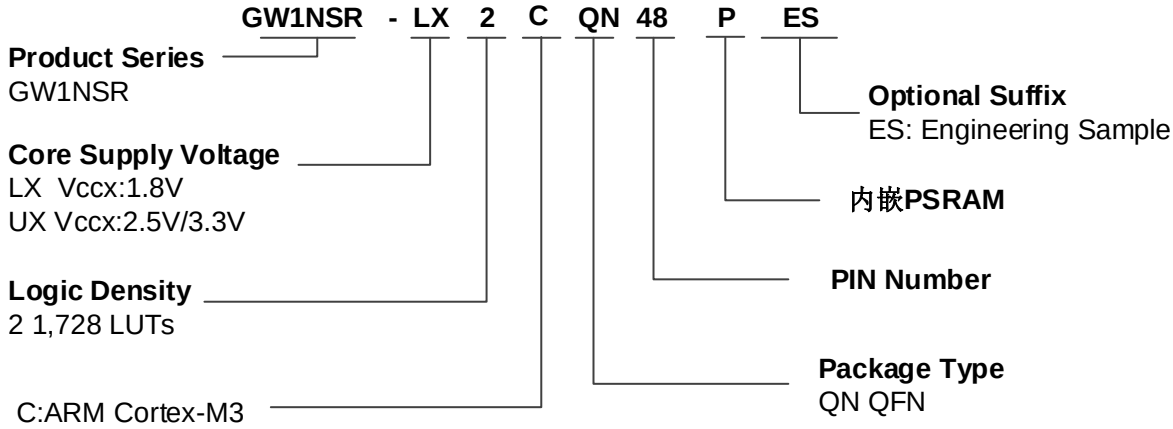


Figure 5-3 GW1NSR-2 Part Naming – Production

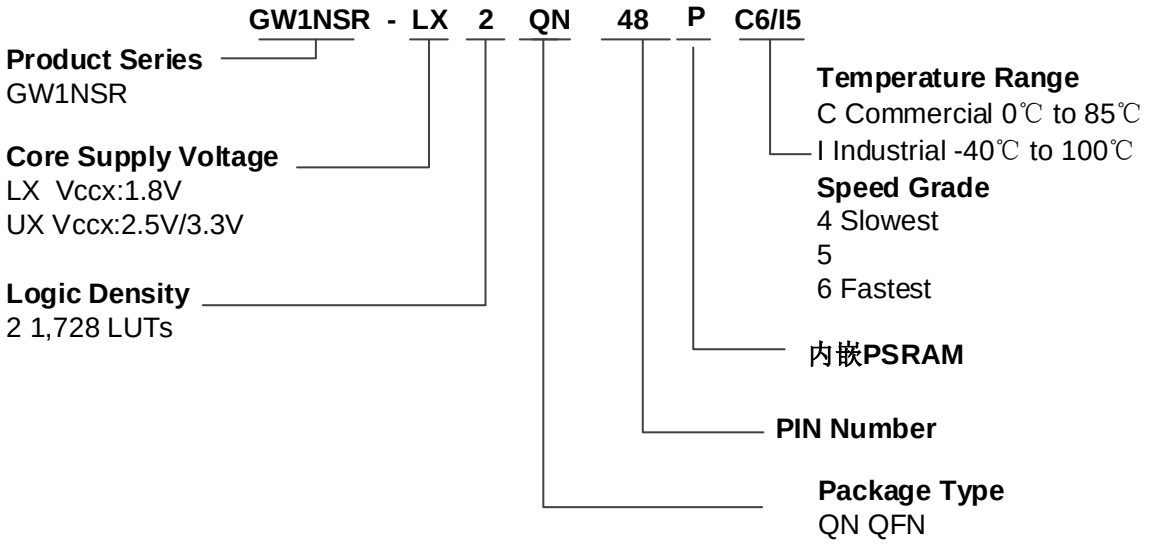
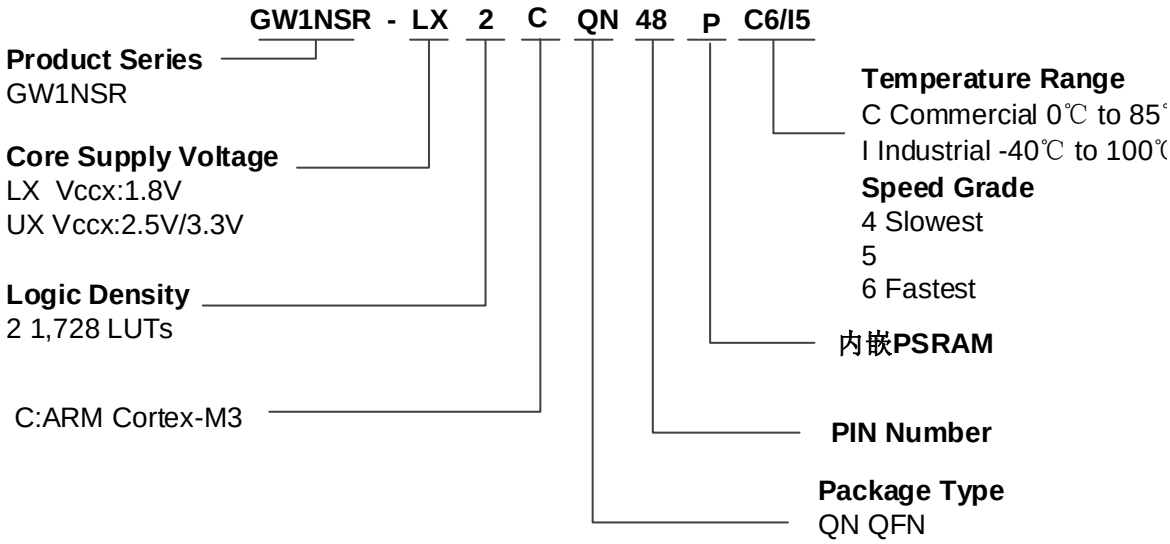


Figure 5-4 GW1NSR-2C Part Naming – Production



Note!

Speed grade is used for both LV and UV.

5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-5.

Figure 5-5 GW1NSR-2 Package Mark

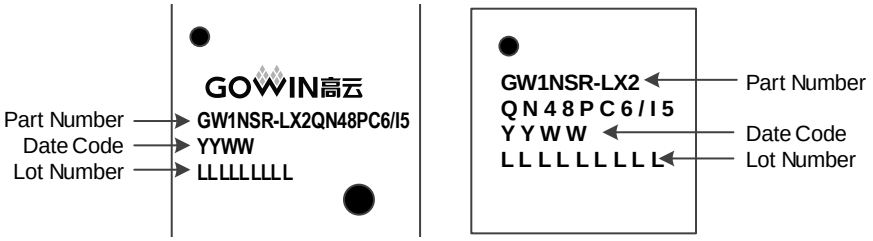
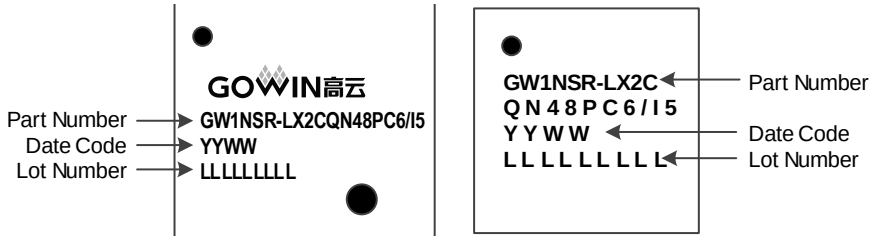


Figure 5-6 GW1NSR-2C Package Mark



Note!

The first two lines in the Figure 5-5 and Figure 5-6 above are the "Part Number".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