Simple Design Techniques for Optimizing Efficiency and Overvoltage Spike of Synchronous Rectification in DC to DC Converters

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1 Abstract

Due to continuous increase of the packaging density and the more and more restricted energy guidelines (80PLUS® [1]), the efficiency of switched-mode power supplies (SMPS) has to be successively improved to go above 90 %. One of the main losses are the diode forward losses of the secondary side rectification of an isolated power converter. Thus, reaching high efficiency is only possible with synchronous rectification (SR), using modern power MOSFETs. This measure can be a trade-off between low efficiency at light output loads due to increased switching losses and high voltage overshoots violating the maximum voltage rating of the synchronous MOSFETs versus efficiency gain. This paper proposes simple to implement design techniques for optimizing overall system efficiency and reducing voltage overshoots for speeding up the SMPS design process.

2 Introduction

The secondary side rectification stage of a switched-mode power supply is typically realized with power diodes. As these diodes have a forward voltage drop of 0.5 V and higher they lead, in combination with the large output currents, to huge conduction losses. To reduce these losses modern power MOSFETs with on-state resistances of few milliohms can be used, which offer a big potential to improve overall system efficiency, especially at high-current operation. A closer comparison of these two variations of rectification shows, that replacing the power diodes by MOSFETs can lead to issues like low efficiency at light output loads or high voltage overshoots at turn-off. This comes from the switching capacitances, which are typically higher for MOSFETs than for diodes [4]. To overcome this drawback a detailed analysis of the optimum $R_{DS(on)}$ has to be performed. Another important issue is the gate timing of the SR MOSFETs. This parameter can highly influence efficiency and overvoltage spike of the converter. To get the whole advantage of modern silicon technologies, the right choice of the package is also an essential topic. Leadless SMD packages help to improve efficiency and dynamic behavior by reducing the parasitic resistive and inductive part of the package.

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3 Choosing the optimum $R_{DS(on)}$

For choosing the optimum $R_{DS(on)}$ of a given MOSFET technology and therefore optimizing for highest efficiency, a well balanced ratio between switching losses and conduction losses has to be found. The description to calculate these losses can be found in a separate paper [2]. At low output loads, the conduction losses play only a minor role while switching losses are the dominant factor. Going for higher loads the ratio turns around and conduction losses become dominant. For an easy calculation of the optimum $R_{DS(on)}$ class for a given SR MOSFET technology, a model is developed. Therefore a MOSFET technology parameter, FOM (figure of merit), is introduced. This FOM gives an indication how the technology will perform in the system, e.g. FOM_{Qg} or FOM_{Qoss}. The FOM is an indicator for the expected gate drive losses or losses from the output capacitance. As the capacitances of a MOSFET are inverse proportional to the $R_{DS(on)}$ this product will stay the same over the whole $R_{DS(on)}$ classes of one fixed technology.

Knowing the switching frequency f_{sw}, the gate driving voltage V_g, the secondary side transformer voltage V_T, the FOM_{Qg} and the FOM_{Qoss}, the optimum $R_{DS(on)}$ can be calculated at a defined MOSFET current I_{RMS}. Following FOMs have to be defined:

$$FOM_{Qg} = R_{DS(on)} \cdot Q_{g\,@\,V_g}$$

Equation 1

$$FOM_{Qoss} = R_{DS(on} \cdot Q_{oss@V_T}$$

Equation 2

The charge always has to be calculated at the respective voltage, meaning Q_{oss} at the transformer voltage V_T and Q_g at the gate driving voltage V_g. Every formula for calculating the power losses can be expressed via the $R_{DS(on)}$ of the MOSFET by introducing constant terms.

$$P_{v\_cond} = I_{RMS}^2 \cdot R_{DS(on)}$$

Equation 3

$$P_{v\_gate} = Q_g \cdot V_g \cdot f_{sw}$$

Equation 4

$$P_{v\_oss} = \frac{1}{2} \cdot V_T \cdot Q_{oss@V_T} \cdot f_{sw}$$

Equation 5

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Following constant terms can be defined for each of the above mentioned formulas:

$$c_{cond} = I^2$$

Equation 6

$$c_{gate} = FOM_{Qg} \cdot f_{sw} \cdot V_g$$

Equation 7

$$c_{oss} = FOM_{Qoss} \cdot \frac{1}{2} \cdot V_T \cdot f_{sw}$$

Equation 8

The total power losses are now defined:

$$P_v = c_{cond} \cdot R_{DS(on)} + c_{gate} \cdot \frac{1}{R_{DS(on)}} + c_{oss} \cdot \frac{1}{R_{DS(on)}}$$

Equation 9

By calculating the derivation of this formula, the optimum $R_{DS(on)}$ is defined.

$$\frac{dP_v}{dR_{DS(on)}} = c_{cond} - c_{gate} \cdot \frac{1}{R_{DS(on)}^2} - c_{oss} \cdot \frac{1}{R_{DS(on)}^2} = 0$$

Equation 10

$$R_{DS(on)\_opt} = \sqrt{\frac{c_{gate} + c_{oss}}{c_{cond}}} = \sqrt{\frac{FOM_{Qg} \cdot f_{sw} \cdot V_g + \frac{1}{2} \cdot FOM_{Qoss} \cdot V_T \cdot f_{sw}}{I_{RMS}^2}}$$

Equation 11

To achieve a balanced efficiency over the whole load range, a reasonable choice of the MOSFET current has to be done. Going for a full load optimization will give good efficiency results at high output currents. But this approach will dramatically decrease efficiency at low loads and increase the number of parallel MOSFETs to a not acceptable value. Therefore an optimum has to be found, in order to achieve a relative constant efficiency value over the whole output current range. To illustrate this issue, efficiency with different optimization approaches can be seen in figure 1. These efficiency charts show the calculated efficiency of a 12V synchronous rectification stage with a transformer voltage of 40V, a gate driving voltage of 10V and a switching frequency of 100kHz. Taking a 75V SR MOSFET technology and calculating the optimum $R_{DS(on)}$ for 10A MOSFET current, gives high efficiency at low currents but very low efficiency at high currents. Going for a 50A optimization will give non acceptable efficiency at low currents, but reaches the maximum at full load. An optimum solution for this setup would be an optimization for 20A, which gives an overall balanced efficiency.
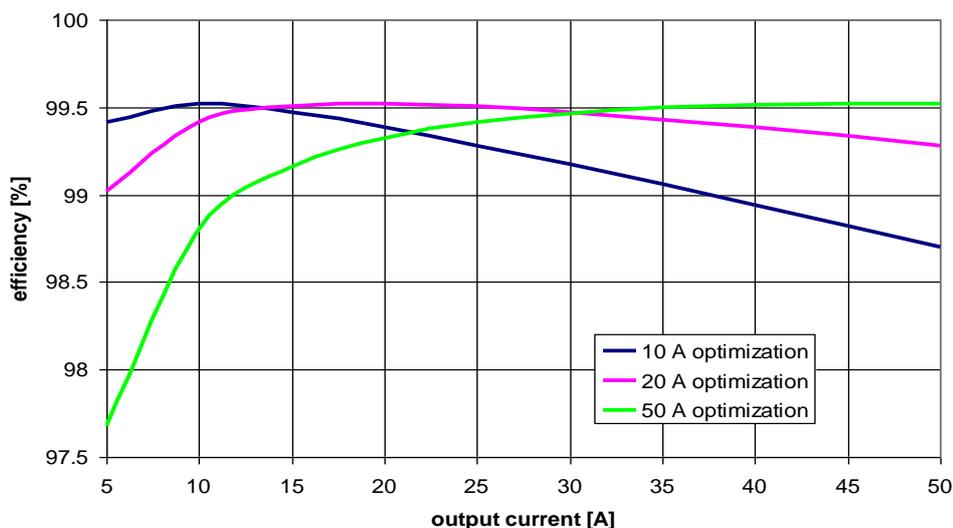
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Figure 1: Calculated efficiency of an SR stage varying point of optimization

4   Optimizing the Snubber Network

A second lever for performance optimization is the choice and design of the snubber network (figure 2), which is responsible for the damping of the voltage overshoot at the SR MOSFET [3]. Taking a simple RC snubber network, which is a series RC combination in parallel to the output capacitance of the MOSFET, creates extra losses. Reason for this is that the snubber capacitance has to be charged and discharged every switching cycle, resulting in switching losses:

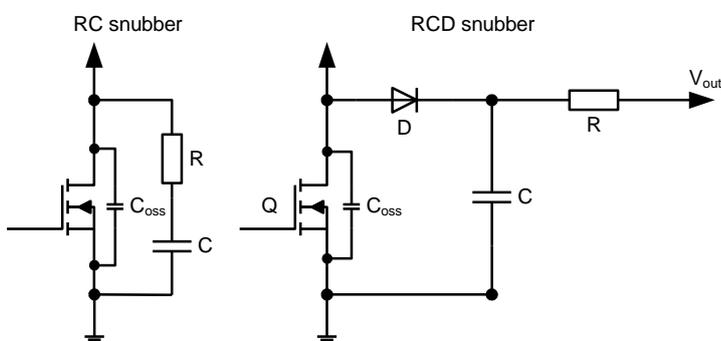$$P_{snub\_loss} = \frac{1}{2} \cdot C_{snub} \cdot V_T^2 \cdot f_{sw}$$

Equation 12

Figure 2: RC vs. RCD snubber network

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Going from this RC combination to a RCD snubber network, losses can be reduced. If the voltage over the MOSFET is rising above the voltage over the snubber capacitance, the diode becomes conductive and the energy is transferred into this capacitance, clamping the overvoltage level (figure 3).
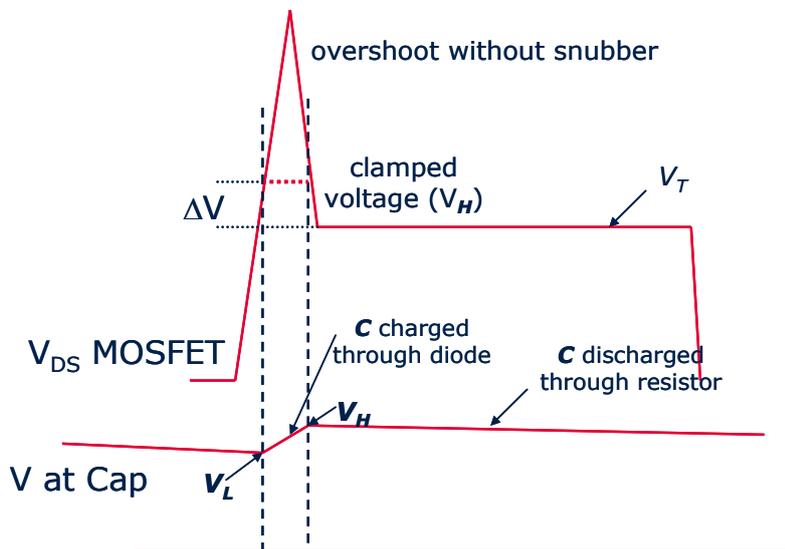

Figure 3: RCD snubber waveforms

The RC time constant has to be adjusted properly, in a way that the voltage over C is not lower than the transformer voltage. In this case the snubber capacitance is decoupled from the MOSFET output capacitance and therefore does not contribute to the capacitive turn off losses. Additionally, it's possible to recover a part of the energy stored in the RCD snubber capacitance by discharging it to the output of the converter, instead to ground. With this method an increase of efficiency of the tested DC/DC converter in low load range up to 0.6% was achieved (figure 4).
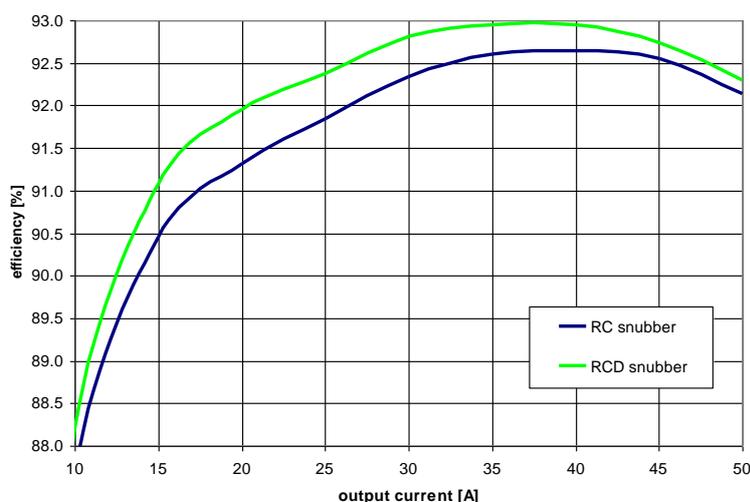

Figure 4: Experimental verification of efficiency - RC vs. RCD snubber

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To get an optimized behavior of this RCD network, the loop MOSFET – diode - capacitor has to me minimized. The lower the inductance, the higher the response time and therefore the higher the effectiveness of the snubber. For the application this means low inductive SMD components have to be used and placed as near as possible to the MOSFET. Ideally this RCD network avoids any additional losses, while allowing to recover some part of the energy of the overshoot.

With the following calculation a rough estimation of the values for the resistance and the capacitance can be done. First of all the energy which is stored in the voltage overshoot has to be known [2].

$$E = V_T \cdot \left(\tfrac{1}{2} \cdot Q_{oss@V_T} + Q_{rr} \right)$$

Equation 13

This energy then gets transferred into the capacitance of the snubber network:

$$E = \tfrac{1}{2} \cdot \left(C_{FET@V_T} + C_{snub} \right) \cdot \left(V_H^2 - V_L^2 \right)$$

Equation 14

Out of this consideration, the capacitance of the snubber can be estimated.

$$C_{snub} = \frac{2 \cdot V_T \cdot \left(\tfrac{1}{2} \cdot Q_{oss} + Q_{rr} \right)}{V_H^2 - V_{L:}^2} - C_{FET@V_T}$$

Equation 15

Depending on C_{snub} the resistor for discharging the capacitor can be calculated:

$$V(t) = \left(V_H - V_{out} \right) \cdot e^{\frac{-t}{R_{snub} C_{snub}}} + V_{out} = V_L$$

$$\frac{V_L - V_{out}}{V_H - V_{out}} = e^{\frac{-t}{R_{snub} C_{snub}}}$$

$$\ln \left(\frac{V_L - V_{out}}{V_H - V_{out}} \right)^{-1} = \frac{t}{R_{snub} \cdot C_{snub}}$$

Equation 16

$$\Rightarrow R_{snub} = \left(f_{sw} \cdot C_{snub} \cdot \ln \frac{V_L - V_{out}}{V_H - V_{out}} \right)^{-1}$$

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These formulas will give a first estimation for the values R_{snub} and C_{snub}. An exact adjustment has to be done by trial and error in the application, as also a lot of external parasitics contribute to the behavior of the snubber network.

5   Optimizing the SR Gate Timing

Another important impact on the voltage overshoot is coming from the gate timing of the SR MOSFET. As typically the body diode is conductive before the SR MOSFET is turned off, special attention has to given to the on-time. The longer the body diode is flooded, the higher the Q_{rr} will be. Higher Q_{rr} means higher inductive turn-off energy, which directly impacts the height of the voltage overshoot. To assure minimum reverse recovery charge the body diode conduction time has to be minimized, see figure 5. Going from 150ns flooding time to 20ns will in this case decrease the voltage overshoot by 20V. Timings below 20ns are critical, as a current shoot through can easily occur. This means again higher overshoots and worse efficiency. A certain minimum dead time has to be guaranteed over the whole load range, as the timing will vary with current.
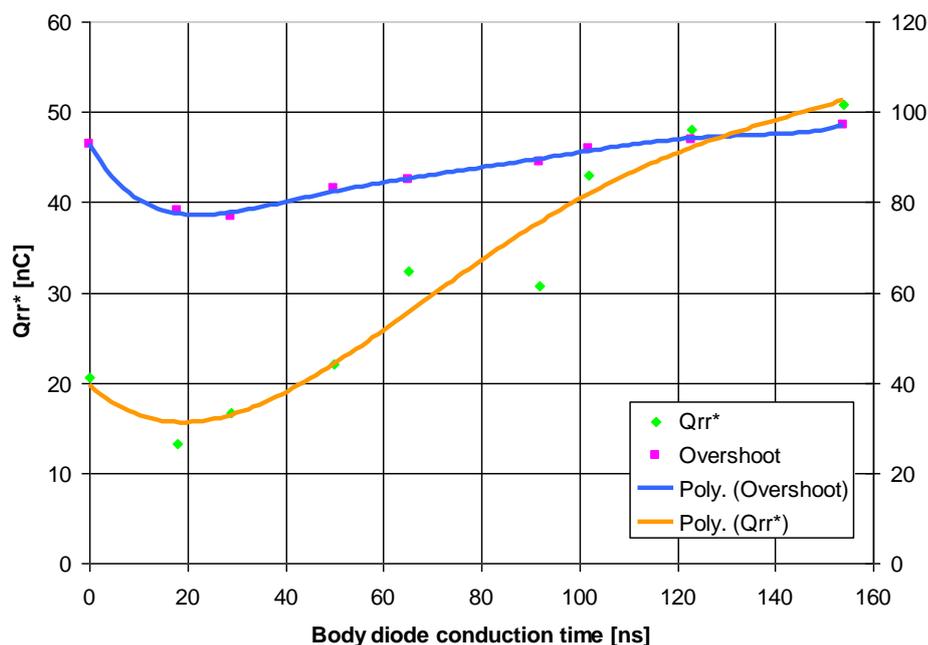
Figure 5: Voltage overshoot and Q_{rr} vs. body diode conduction time

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6 Optimizing the Package

Looking into the past, the standard package type for a power switch was the TO220 package. The reason for this was the excellent cooling capability and the easy handling at the mounting process. As nowadays the silicon technologies have dramatically improved, the on-state resistances of low voltage power switches are in the range of 2mOhms or less, but the resistive part of the same package stayed the same. This means, the percental resistive contribution of the package to the whole $R_{DS(on)}$ has dramatically increased. Standard through-hole types like the TO220 are now limiting modern silicon technologies. This requires to rethink the packaging strategy towards a lower resistive contribution to get out more of modern silicon switches. [6]

6.1   Package Contribution to the Product $R_{DS(on)}$

Taking modern MOSFET 30V technologies, an on-state resistance as low as 1.2mOhm can be reached in a TO-220 package. Taking into account, that the resistance of the packaging (TO-220) is in the range of 1mOhm, the package contribution to the total $R_{DS(on)}$ is roughly 80%, see figure 6. Accordingly, the resistive silicon content is only about 20%, which clarifies the today's situation of low ohmic MOSFET silicon. Not the silicon, but the package is hindering lower on-state resistances in standard through-hole packages [5]. Going to SMD package types, like the D²PAK, the influence of the package can already be decreased. A further, much more progressive step is to use leadless SMD package types. This cuts down the package contribution by 50% compared to a TO-220 and enables higher performances of the product.

This high resistive package contribution is primarily affecting MOSFETs with lower breakdown-voltage. The higher the MOSFET voltage class, the higher the $R_{DS(on)}$ will be. This in turn means a lower percental contribution of the package resistance to the total $R_{DS(on)}$. Taking a 150V technology, the package contribution is only in the range of 5% to 20%, while for 30V MOSFETs the range is 40% to 80%.
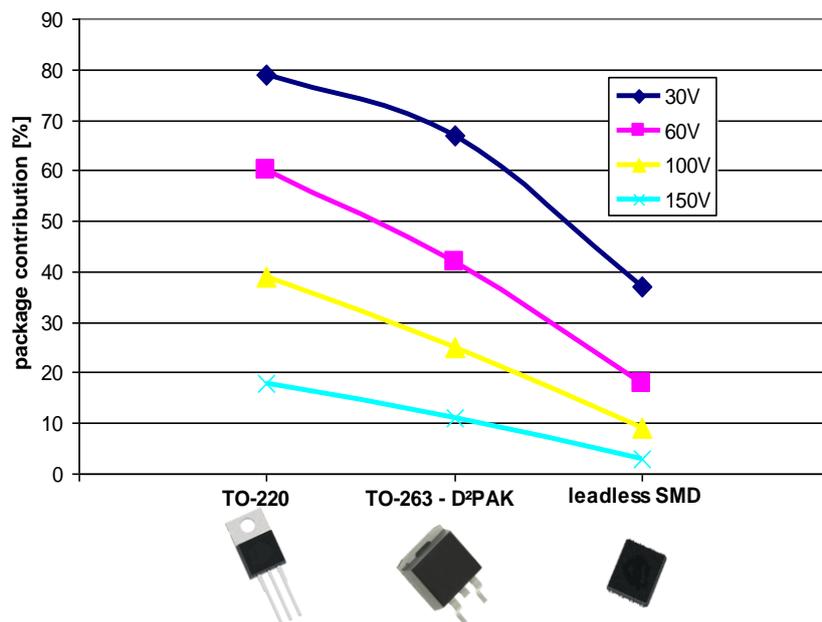
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Figure 6: Package contribution to the whole resistance of the product

6.2   Improving the Figure of Merit

To evaluate the performance of a MOSFET technology, the FOM_{Qg} can give an indication.

$$FOM_{Qg} = R_{silicon} \cdot Q_g$$

Equation 17

For a given silicon technology this parameter is a constant, as the capacitances of a MOSFET are indirect proportional to the $R_{DS(on)}$. Taking into account different package types, the FOM_{Qg} is not constant any more. The package resistance adds a constant value to the silicon resistance.

$$FOM_{Qg} = \left(R_{silicon} + R_{package} \right) \cdot Q_g$$

Equation 18

This results in different FOM_{Qg} values for different packages and different $R_{DS(on)}$ classes of a given MOSFET technology. The impact of the package resistance increases as the silicon resistance decreases, see figure 7. The left two bars show two different packages with the same silicon inside. The right side shows the same setup but a higher $R_{DS(on)}$ class.
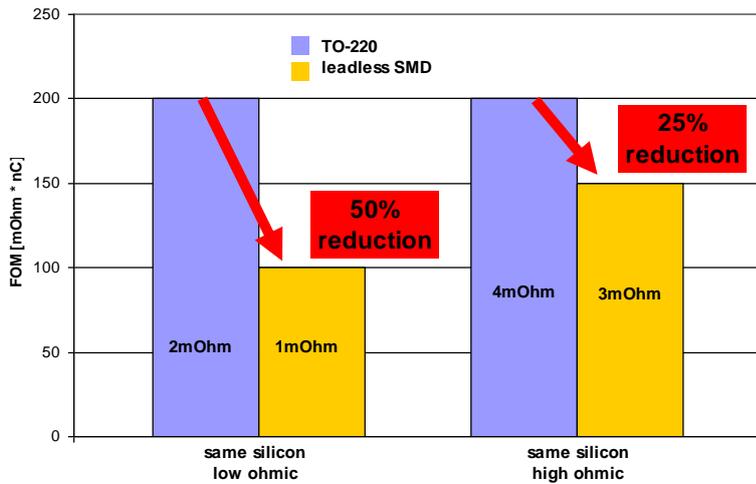
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Figure 7: Impact of the package and the $R_{DS(on)}$ class to the FOM_{Qg}

For the lower $R_{DS(on)}$ class the package has a much higher influence to the FOM_{Qg}. Changing the package from TO-220 to a leadless SMD version can reduce the FOM_{Qg} up to 50% in case of a 2mOhm switch. The higher the $R_{DS(on)}$, the lower the impact of the package.
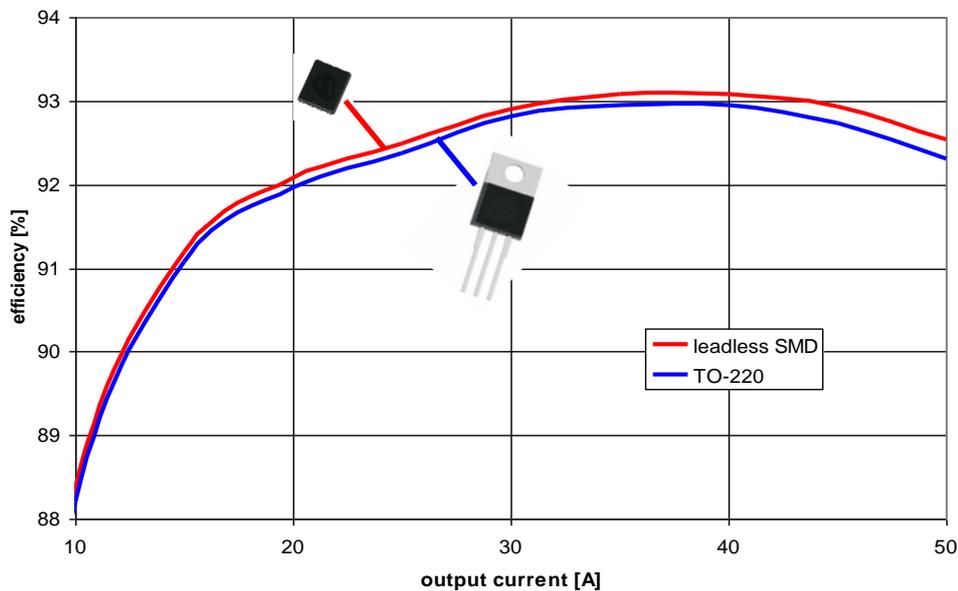

Figure 8: Experimental efficiency results for package comparison in a 12V SR stage

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Through an experimental verification of the theory, exactly the forecasted results can be seen (figure 8). The leadless SMD package shows a better efficiency over the whole output load range, although the same silicon is used.

6.3 Improving the Switching Behavior

Comparing a leadless package with a TO-220, not only the resistive package contribution is much lower, but also the parasitic inductances are smaller. Due to the leadless design and the bonding with a clip, inductances are fairly reduced and can reach values as low as 0.2nH while a TO-220 package is in the range of 10nH and more. This inductance combined with high di/dt values at the turn-off process of a MOSFET is inducing voltages at the gate connection, which can reach the threshold level. This can provoke an inductive turn-on, resulting in a shoot-through with bad efficiency or even destruction of the switch.

Not only inductive turn-on effects but also high voltage overshoots at the turn-off process can occur with TO-220 packages. Low inductive leadless SMD packages can minimize this effect. In a 12V synchronous rectification stage, a reduction of 10V could be realized just be replacing the TO-220 package with a low inductive one, see figure 9. With reduced voltage stress smaller voltage classes of the MOSFET can be used to further optimize the system.
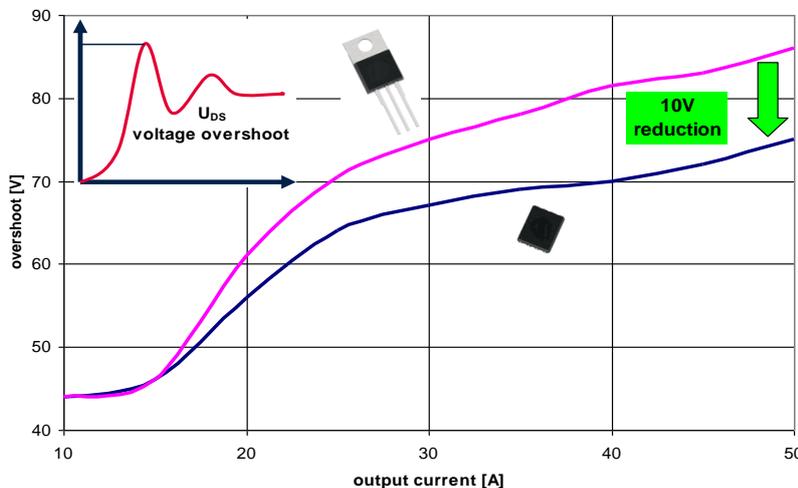

Figure 9: Experimental voltage overshoot results for package comparison in a 12V SR stage

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7   Conclusion

For achieving highest efficiency in synchronous rectification, simply replacing the diodes by MOSFETs will not lead to success. A careful and detailed analysis of the whole system is necessary. By choosing the optimum $R_{DS(on)}$ value of the MOSFET, adjusting the gate timing or adapting the snubber network, higher efficiencies can be achieved and the design process is simplified. A further high potential lever for improved performance is the right choice of the MOSFET package type. Modern silicon technologies are more and more hindered by standard packages and their parasitics. Leadless SMD packages help to improve efficiency and the dynamic behavior by reducing the parasitic resistive and inductive part. Switching losses are reduced and the risk of an inductive turn-on can be minimized, while at the same time voltage overshoots are limited. A combination of all mentioned methods can highly increase the potential for efficiency and improve switching behavior of the SR MOSFET.

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