Gowin HyperRAM Memory Interface IP
User Guide

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Disclaimer

Revision History

Date	Version	Description
07/30/2020	1.0E	Initial version published.
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1 About This Guide

1.1 Purpose

Gowin HyperRAM Memory Interface IP user guide includes the structure and function description, port description, timing description, configuration and call, reference design, etc. The guide helps you to quickly learn the features and usage of Gowin HyperRAM Memory Interface IP. The usage of HyperRAM Memory Interface external and HyperRAM Memory Interface embedded is basically the same, and this manual introduces the usage of HyperRAM Meomory Interface embedded as the main body, which can also be applied to HyperRAM Memory Interface external if not otherwise specified.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com/en:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS871, GW1NSE series of FPGA Products Data Sheet
- DS881, GW1NSER series of SecureFPGA Products Data Sheet
- DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
RAM	Random Access Memory
LUT	Look-up Table
GSR	Global System Reset

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin HyperRAM Memory Interface embedded IP is a common used HyperRAM interface IP, in compliance with HyperRAM standard protocol. The IP includes the HyperRAM MCL (Memory Controller Logic) and the corresponding PHY (Physical Interface) design. Gowin HyperRAM Memory Interface embedded IP provides you a common command interface to connect with the HyperRAM chip for data access and storage.

Table 2-1 Gowin HyperRAM Memory Interface Embedded IP

Gowin HyperRAM Memory Interface IP	
Supported Devices （HyperRAM Memory Interface embedded）	● GW1NSR-4C Series ● GW1NSER-4C Series
Supported Devices （HyperRAM Memory Interface external）	All Gowin devices (except GW1N-1/GW1N-1S/GW1NR-1/GW1NZ-1)
Logic Resource	Please refer to Table 3-1
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify Pro
Application Software	Gowin Software

3 Features and Performance

3.1 Features

- Compatible with interfaces of standard HyperRAM devices;;
- Supports memory data path width of 8 bits, 16 bits, 24 bits, 32 bits, 40 bits, 48 bits, 56 bits, and 64 bits.
- Supports x8 data width memory chip;
- Programs 16, 32, 64 or 128 burst lengths;
- The clock rate is 1:2;
- Supports the initial latency of six or seven clock cycles;
- Supports the fixed latency mode;
- Supports the power off option;
- Configurable drive strength;
- Configurable self-refresh area;
- Configurable refresh rate.

3.2 Operating Frequency and Bandwidth Efficiency

The data rate and efficiency of the Gowin HyperRAM Memory Interface embedded IP supports:

- Supports operating speeds of 166 MHz and 200 MHz.
- Maximum operating data rate 333Mbps, 400Mbps.
- 128 burst lengths with a bandwidth efficiency of 74 per cent.
- 64 burst lengths with a bandwidth efficiency of 59 per cent.
- 32 burst lengths with a bandwidth efficiency of 42 per cent.
- 16 burst lengths with a bandwidth efficiency of 26 per cent.

3.3 Resource Utilization

The Gowin HyperRAM Memory Interface embedded IP employs the Verilog language, which is used in the GW1NSR-4C and GW1NSER-4C FPGA devices. presents an overview of the resource utilization. For the applications on the other GOWINSEMI FPGA devices, please see the associated post-release information.

Table 3-1 Resource Utilization

DQ_WIDTH	LOGICs	REGs	I/O	f_{MAX}	Throughput	Device Series	Speed Level
8(x8)	615	541	16	333Mbps/ 400Mbps	f_{MAX} x DQ x work efficiency	GW1NSR-4C GW1NSER-4C	C7/I6 C6/I5 C5/I4
16(x8)	947	898	29				

Note!

In Table 3-2, the user address width of the Gowin HyperRAM Memory Interface embedded IP is 22 bits, the HyperRAM WITDH is x8, and the burst length is 32. The increased burst length will increase the resource utilization.

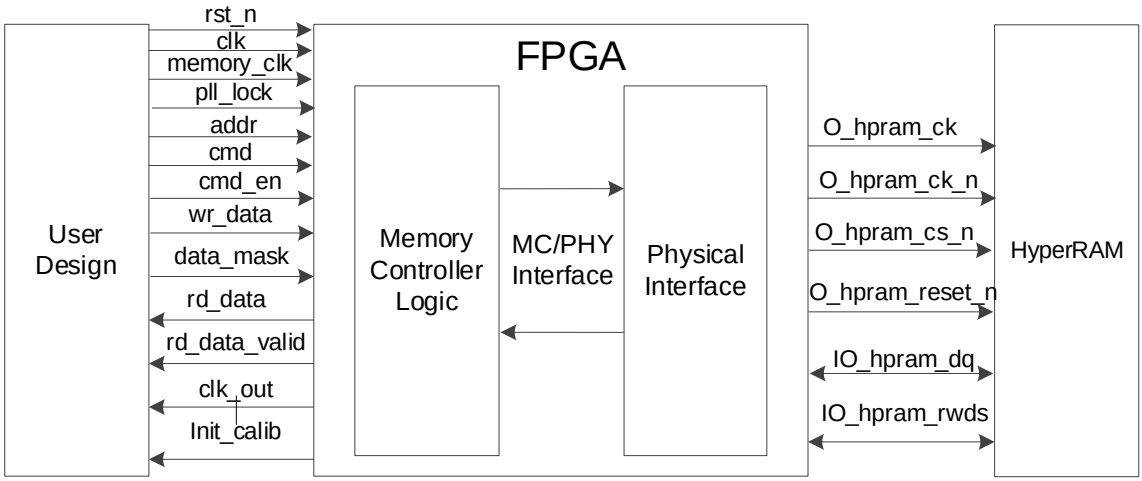
4 Functional Description

4.1 Architecture

As shown in Figure 4-1, the Gowin HyperRAM Memory Interface embedded IP mainly includes Memory Controller Logic, Physical Interface, etc.

Figure 4-1 The User Design module in is the module connected to the external HyperRAM chip in FPGA.

Figure 4-1 Gowin HyperRAM Memory Interface Embedded IP Structure



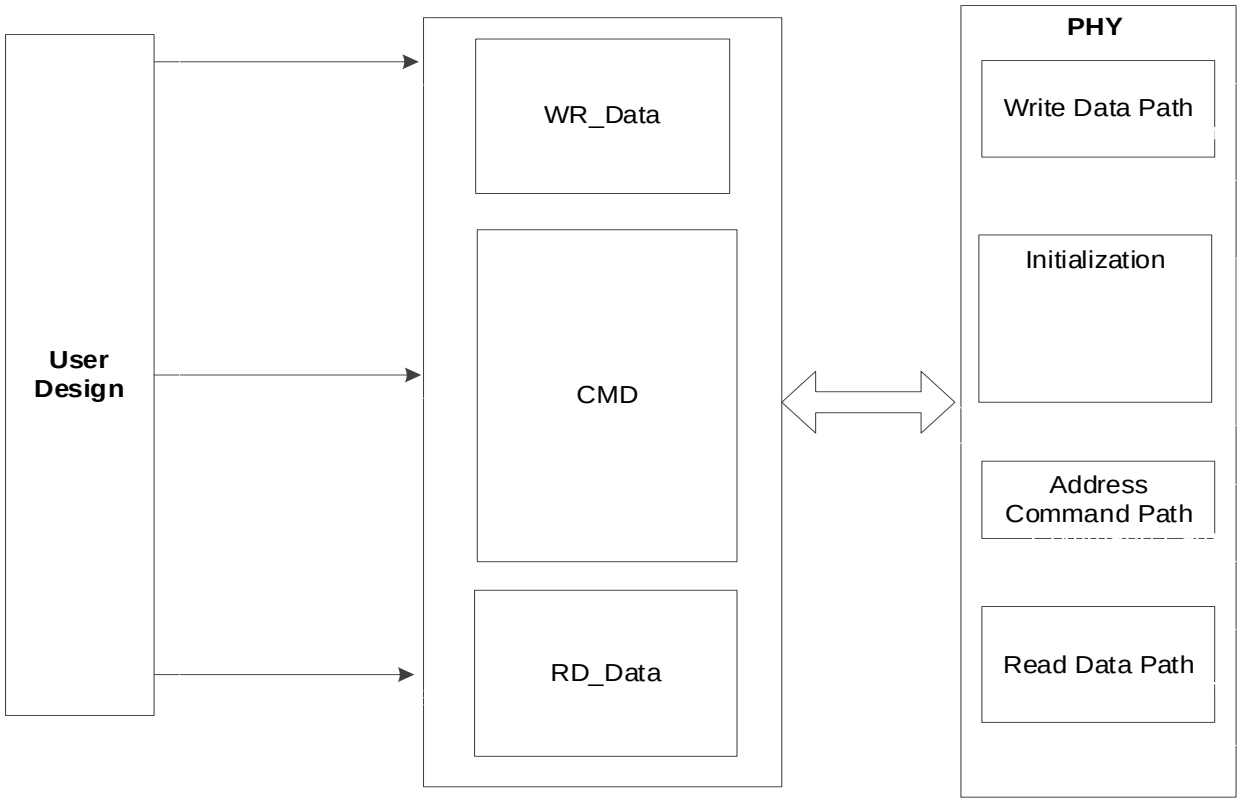
4.2 Memory Controller Logic

Memory Controller Logic is the logic module of Gowin HyperRAM Interface embedded IP, which locates between User Design and PHY. The Memory Controller Logic receives the command, address, and data from the user interface and stores them in logical order.

The write, read and other commands that you sent are sorted and reorganized in Memory Controller Logic to combine a data form that complies with the HyperRAM protocol. Meanwhile, when the Memory Controller Logic writes data, the data will be reorganized and cached to meet the initial delay value between the command and the data. When the Memory Controller Logic reads the data, the data will be sampled and reorganized to be the correct one.

The HyperRAM Memory Controller consists of the following main modules, including the CMD unit, the WR_Data unit, the RD_Data unit, etc. The main structure is shown in Figure 4-2.

Figure 4-2 HyperRAM Memory Controller Logic Basic Structure

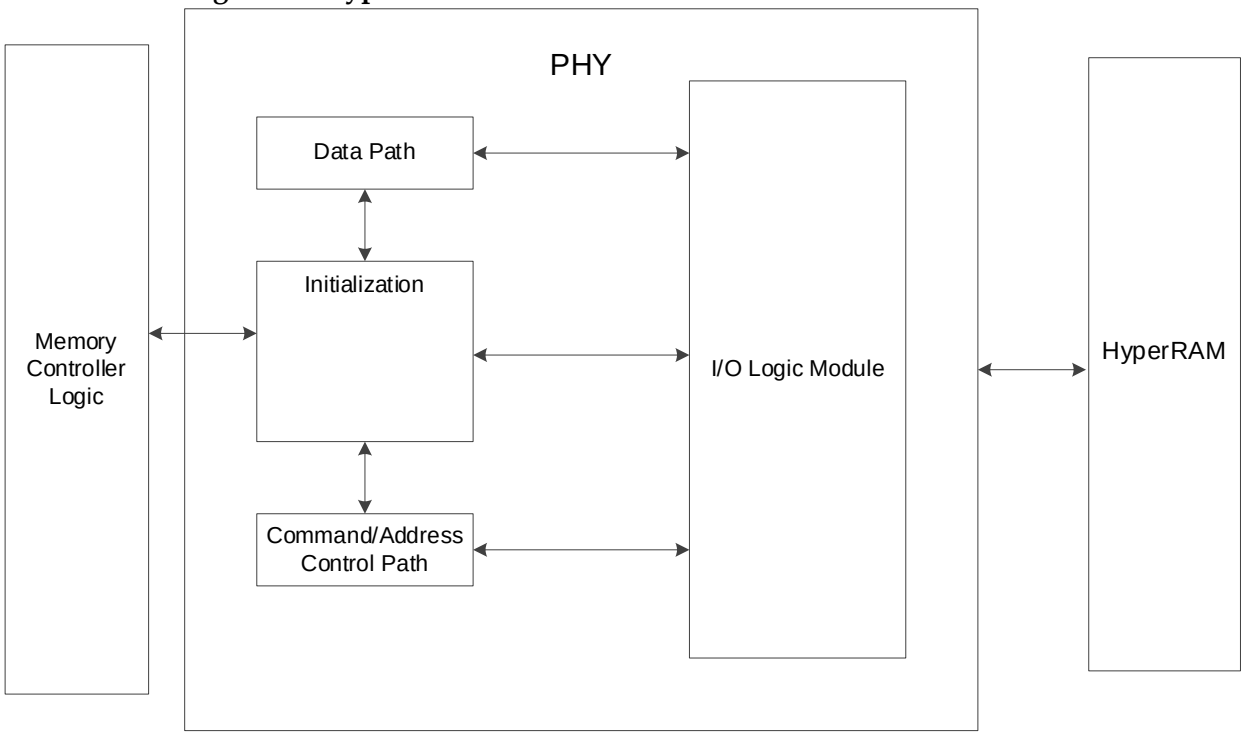


4.3 PHY

The PHY provides the physical layer definition and interface between Memory Controller Logic and the external HyperRAM. It receives the commands and data from the Memory Controller Logic and provides the HyperRAM interface with signals that meet the timing and sequence requirements.

The basic structure of the PHY includes four modules: initialization module, data path, command/address control path and I/O logic module, as shown in Figure 4-3.

Figure 4-3 HyperRAM PHY Basic Structure



4.3.1 Initialization Unit

The initialization module is mainly used for the initialization and read-calibration after power on of HyperRAM. After all initialization and read-calibration are finished, the signal "init_calib" will be high to indicate the completion of the initialization.

Power-on Initialization

According to the HyperRAM protocol standard, it needs to initialize the PSRAM after power on. This includes the reset, mode register configuration, and read calibration.

4.3.2 Data Path Unit

Data path includes write data and read data.

4.3.3 Control Path Unit

The command/address control path is a single pass that receives the command and address signals sent by the Memory Controller Logic and cooperates with the data path to process the write and read data delay parameters and sends the commands to the I/O logic module.

4.3.4 I/O Logic Unit

The Logic I/O module is mainly used to convert the clock domain of the data, command, and address signals received from the data path and command/address path.

4.4 Major Functions

The functions of the HyperRAM Memory Interface embedded IP are as follows:

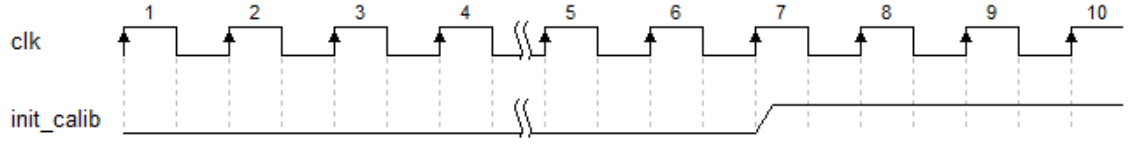
- Initializes the HyperRAM;
- Sends the addresses and commands;
- Writes data;
- Reads data;

4.4.1 Initialization

HyperRAM must be read calibrated to perform normal write and read operations. After power on, the HyperRAM will be initially read calibrated using the PHY and then returns the “init_calib” initialization mark.

The completion signal is returned to you after the initialization is completed, as shown in Figure 4-4.

Figure 4-4 Initialization Completion Signal Timing Diagram



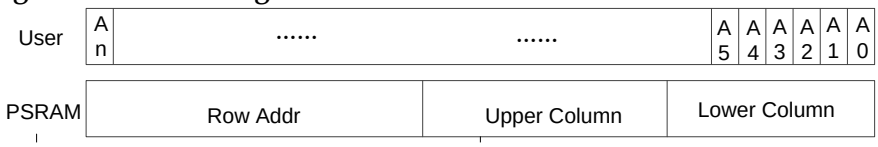
4.4.2 Send Addresses and Commands

You can send operation commands and addresses through the addr, cmd, and cmd_en interfaces.

- addr is the address data interface;
- Continuous address write operation, two adjacent operations address plus burst length/ 2, continuous address read operation is the same;
- cmd is the command data interface;
- cmd_en is the enable signal of the address and command, active high.

In the application, a mapping relationship exists between the address bus of user interface and the physical memory ROW, Upper Column, and Lower Column. In this design, it is in ROW-Upper Column-Lower Column order. The addressing scheme is as shown in Figure 4-5. In the application, you only need to give the address as needed, and the mapping relationship is excluded.

Figure 4-5 Addressing Scheme in Row-Column Order



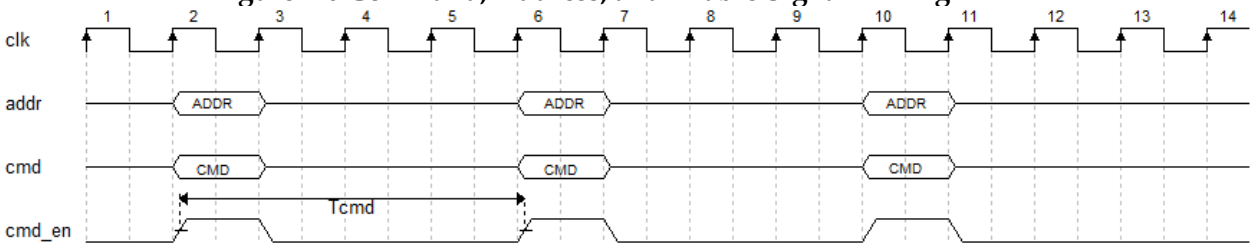
The commands that you sent through the cmd interface are as shown in Table 4-1:

Table 4-1 cmd Command

Command	cmd
Read	1'b0
Write	1'b1

At the user interface, the timing between the command, address, and enable signals is as shown in Figure 4-6.When the cmd_en is high, the cmd and the addr are valid at this time.

Figure 4-6 Command, Address, and Enable Signal Timing



When actually used by the client, the two commands (write-read/read-write/write-write/read-read) interval must satisfy the minimum interval period to the）, i.e., when the burst length is 16, the command interval is at least 15 clock cycles; when the burst length is 32, the command interval is at least 19 clock cycles; when the burst length is 64, the command interval is at least 27 clock cycles; when the burst length

is 128, the command interval is at least 43 clock cycles. High-speed read and write requires an appropriate increase in the number of Tcmd cycles, as shown in Table 4-2.

Table 4-2 Relationship between Tcmd period and burst length

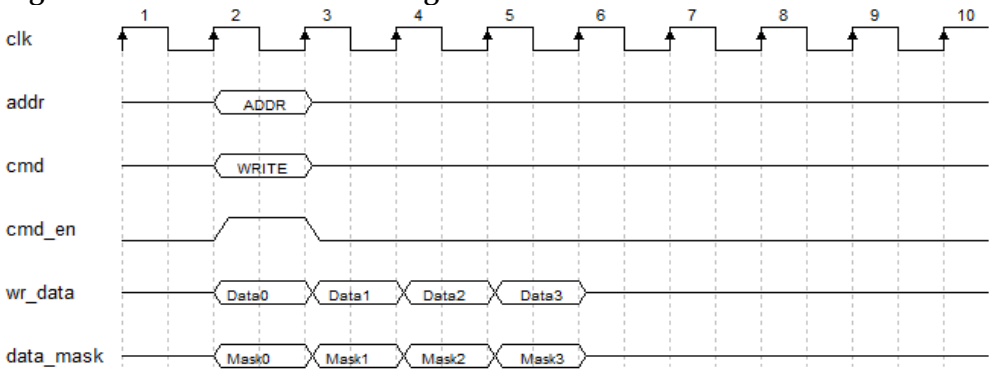
Burst length	Tcmd (interval before two commands, read/write indistinguishable), HyperRAM speed is 166M and below	Tcmd (interval before two commands, read/write indistinguishable), HyperRAM speed is Above 166M
128	43 user clocks	48 user clocks
64	27 user clocks	32 user clocks
32	19 user clocks	24 user clocks
16	15 user clocks	20 user clocks

4.4.3 Write Data

You can send the data to the Gowin HyperRAM Memory Interface IP through the user Interface of wr_data and data_mask, etc. The write data will be sent to the HyperRAM after being processed.

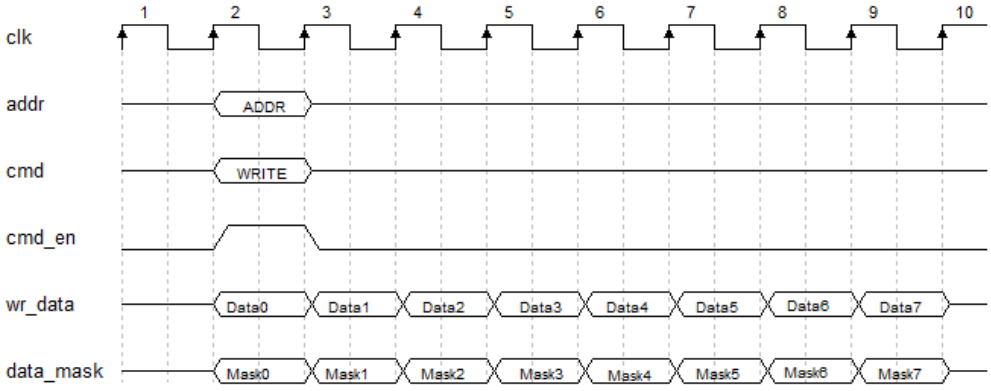
- The wr_data is a write data port;
- Data_mask a write mask port;
- There are many timing situations between the data channel and the command channel. Take the 16 burst length as an example;

Figure 4-7 Write Data Port Timing



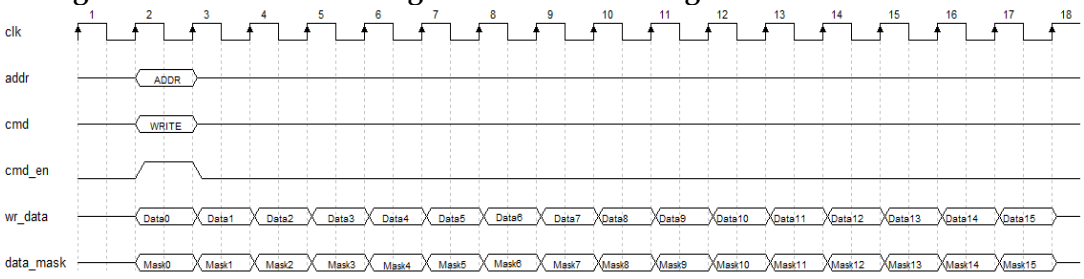
- The write data occupies 8 CLK cycles if the burst length is 32, as shown in Figure 4-8.
- If the mask function is not used, the data_mask can be 0.

Figure 4-8 Write Data Timing When the Burst Length is 32



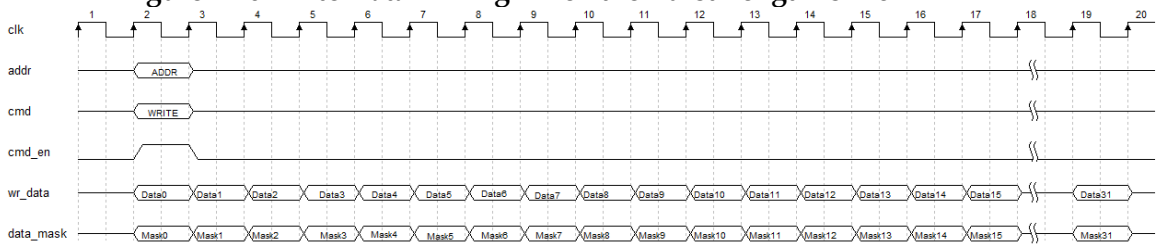
- The write data occupies 16 CLK cycles if the burst length is 64, as shown in Figure 4-9.
- If the mask function is not used, the data_mask can be 0.

Figure 4-9 Write Data Timing When the Burst Length is 64



- The write data occupies 32 CLK cycles if the burst length is 128, as shown in Figure 4-10.
- If the mask function is not used, the data_mask can be 0.

Figure 4-10 Write Data Timing When the Burst Length is 128

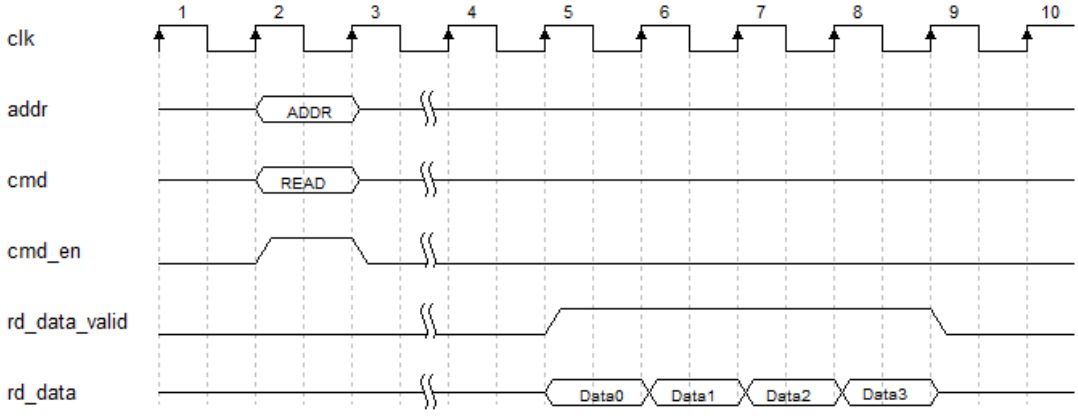


4.4.4 Read Data

You can read the data from the HyperRAM using the user interfaces rd_data and rd_data_valid.

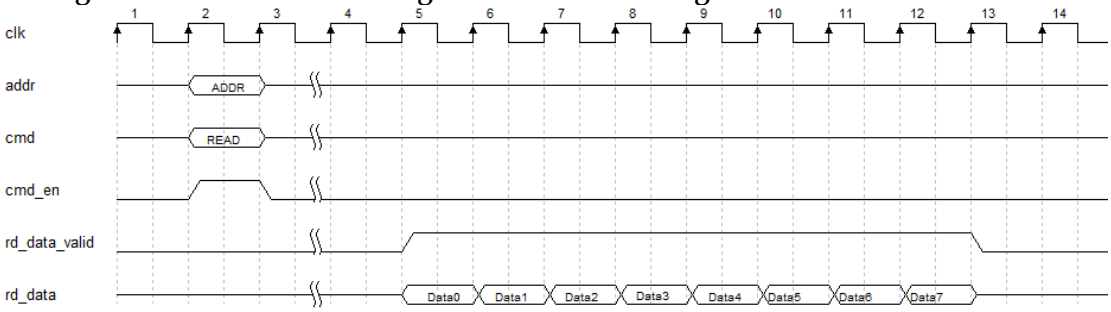
- The rd_data interface is the returned read data interface.
- The rd_data_valid interface signal is the valid read data interface. When it is high, the returned rd_data is valid at this time.
- There are many timing cases between the read data channel and the command channel. Take the 16 burst length as an example.

Figure 4-11 Read Data Port Timing



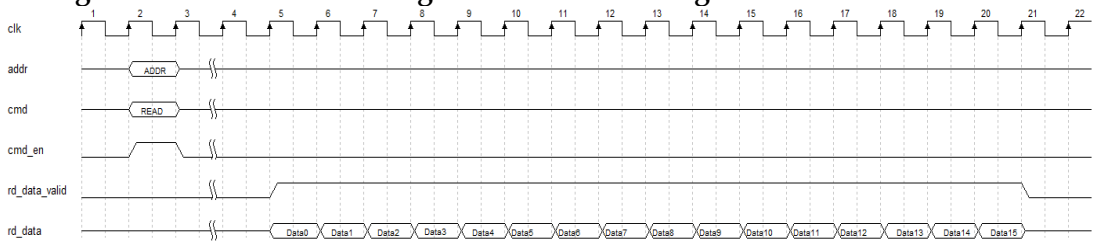
- The read data occupies 8 CLK cycles if the burst length is 32, as shown in Figure 4-12.

Figure 4-12 Read Data Timing When the Burst Length is 32



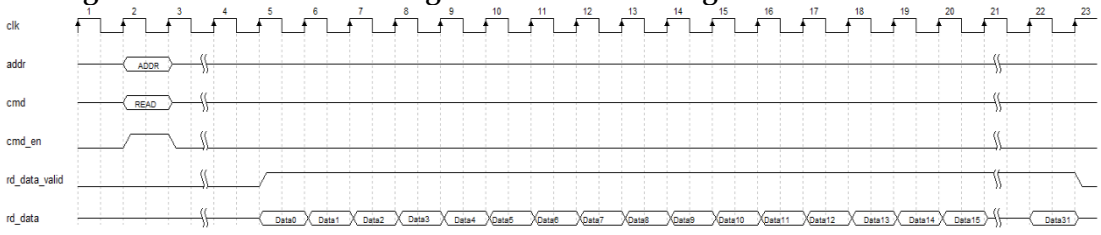
- The read data occupies 16 CLK cycles if the burst length is 64, as shown in Figure 4-13.

Figure 4-13 Read Data Timing When the Burst Length is 64



- The read data occupies 32 CLK cycles if the burst length is 128, as shown in Figure 4-14.

Figure 4-14 Read Data Timing When the Burst Length is 128



5 Ports List

The I/O ports of the Gowin HyperRAM Memory Interface embedded IP are shown in Table 5-1.

Table 5-1 IO Interface of Gowin HyperRAM Memory Inteface Embedded IP

Signal	Data Width	I/O	Description
User Interface			
addr	ADDR_WIDTH	Input	Address input
cmd	1	Input	Command channel
cmd_en	1	Input	Command and address enable signals: 0: invalid 1: valid
rd_data	4*DQ_WIDTH	Output	Read data channel
rd_data_valid	1	Output	rd_data valid signal: 0: invalid 1: valid
wr_data	4*DQ_WIDTH	Input	Write data channel
data_mask	MASK_WIDTH	Input	Provide the masking signals for wr_data
clk	1	Input	Reference input clock, it is usually on-board crystal oscillator clock
init_calib	1	Output	Initialization completed signal
clk_out	1	Output	The user-design clock, with a frequency of 1/2 Memory Clk
rst_n	1	Input	Input reset signal: 0: valid 1: invalid
memory_clk	1	Input	You can input chip working clock, which is generally a high clock of PLL frequency doubling, or not use PLL
pll_lock	1	Input	If memory_clk is PLL frequency doubling input, this interface is connected to PLL's

Signal	Data Width	I/O	Description
			pll_lock pin If you do not use PLL, this interface is connected to 1'b1
HyperRAM Interface			
O_hpram_cs_n	CS_WIDTH	Output	Chip selects, low valid
O_hpram_ck	CS_WIDTH	Output	A clock signal provided for HyperRAM
O_hpram_ck_n	CS_WIDTH	Output	Compose the difference signal with the O_hpram_ck
O_hpram_reset_n	CS_WIDTH	Output	HyperRAM reset signal
IO_hpram_dq	DQ_WIDTH	Bidirection	HyperRAM data
IO_hpram_rwds	RWDS_WIDTH	Bidirection	HyperRAM MCL data selection signal and mask signal

6 Parameters Configuration

The Gowin HyperRAM Memory Interface embedded IP supports HyperRAM devices. You need to configure various static parameters and timing parameters of the Gowin HyperRAM MCL Memory Interface according to the design requirements. The specific parameters are as shown in Table 6-1.

Table 6-1 Static Parameter Options of Gowin HyperRAM Memory Interface Embedded

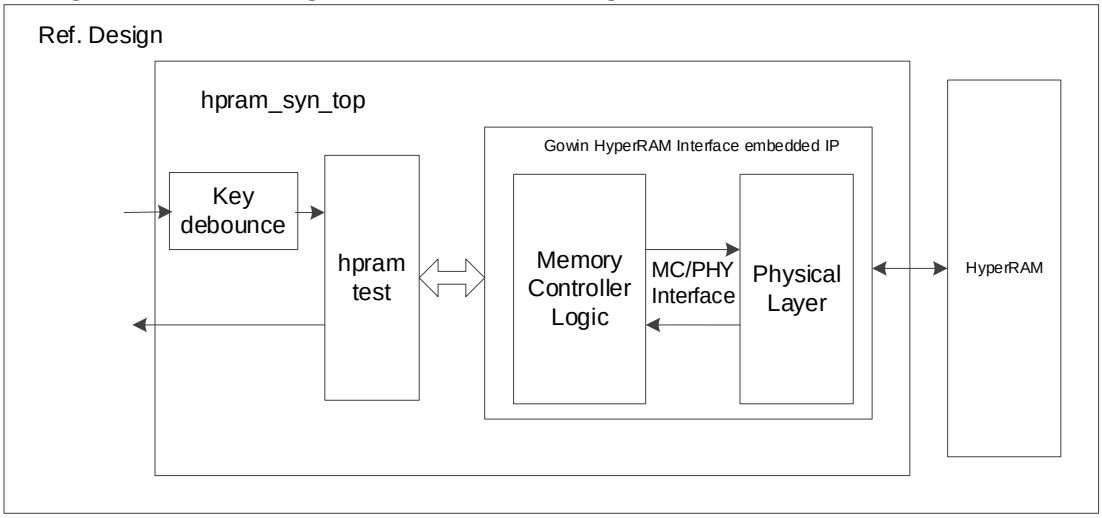
Name	Description	Options
Memory TYPE	HyperRAM models	W956x8MKY, Custom;
CLk Ratio	The CLK ratio of the PSRAM PHY to internal logic clock. You cannot operate it.	1:2;
Memory Clock	The operating frequency that you expected	50Mhz~250Mhz；
Psram Width	DQ width of HyperRAM	8;
Dq Width	The data bit width that you required	8,16, 24,32, 40,48, 56,64;
Addr Width	Address width that you filled according to the specific chip	22;
Data Width	User data bit width	4*Dq Width;
CS Width	Chip selection width	Dq Width/ Psram Width;
Mask Width	Mask width	Data Width/ Psram Width;
Burst Mode	Data burst length	16, 32, 64, 128;
Burst Num	Burst data number	Burst Mode/4;
Fixed Latency Enable	Fixed latency enable	“Fixed”;
Initial Latency	Initial latency	6, 7;
Drive Strength	Drive strength;	19, 22, 27,34, 46,67, 115;
Deep Power Down	Deep power down	“OFF”, “On”;
Hybrid Sleep Mode	Sleep mode	“OFF”, “On”;

Name	Description	Options
Memory TYPE	HyperRAM models	W956x8MKY, Custom;
Refresh Rate	Refresh rate	“Normal”, “Fast”
PASR	Self refresh area	full, bottom_1/2,bottom_1/4,bottom_1/8, top_1/2, top_1/4, top_1/8;

7 Reference Design

To quickly familiar with and use Gowin HyperRAM Memory Interface embedded IP, a simple reference design is provided for you. The basic structure of reference is shown in Table 7-1.

Figure 7-1 Block Diagram of Reference Design



In the reference design, the hpram_syn_top module is the top-level module unit, and its interfaces are connected to the input reference clocks, external reset signals, etc, as shown in Table 7-1. The hpram_test is used to generate the address, data, and read/write commands required by the Gowin HyperRAM Interface embedded IP, and the module can be synthesized. The Key_debounce module is a jitter elimination module that is used to eliminate the signal jitter generated by the key or dial switch when it controls the external excitation.

Table 7-1 hpram_syn_top Input Interface List

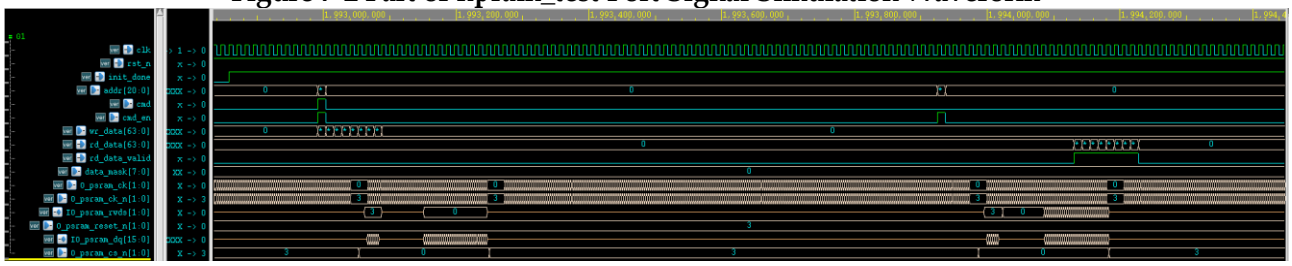
Name	Description
clk	Input reference clock, 50MHz by default
rst_n	Input reset signal

The hpram_test module generates n consecutive write signals and data, after which it performs consecutive read operations on the written

data, and checks the data. In this reference design, the memory granule is W956x8MKY, the Burst Mode is 128, and the DQ width is 8 bits.

The simulation waveforms of some signals between the psram_test and the HyperRAM Memory Interface embedded IP interfaces are shown in Figure 7-2.

Figure 7-2 Part of hpram_test Port Signal Simulation Waveform



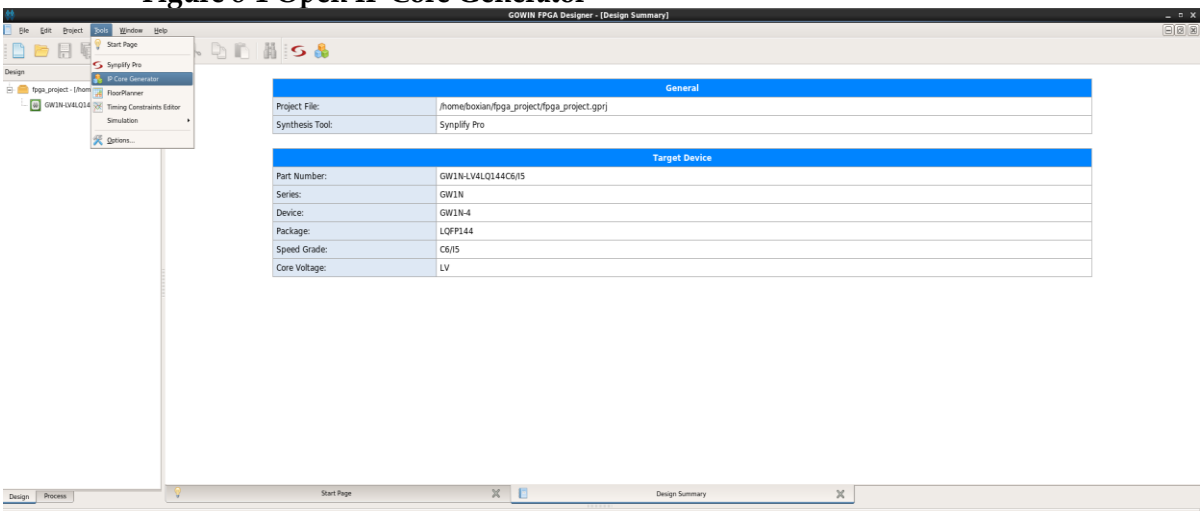
8 Interface Configuration

You can call and configure the Gowin HyperRAM Memory Interface embedded IP using the embedded IP Core Generator tool in the IDE. In this chapter, take the “winbond W956x8MKY HyperRAM” as an example, introduce the main configuration interface, configuration flow and the meaning of each configuration option.

1. Open IP Core Generator

After creating the project, you can click the “Tools” tab in the upper left, select and open the IP Core Generater via the drop-down list, as shown in Figure 8-1.

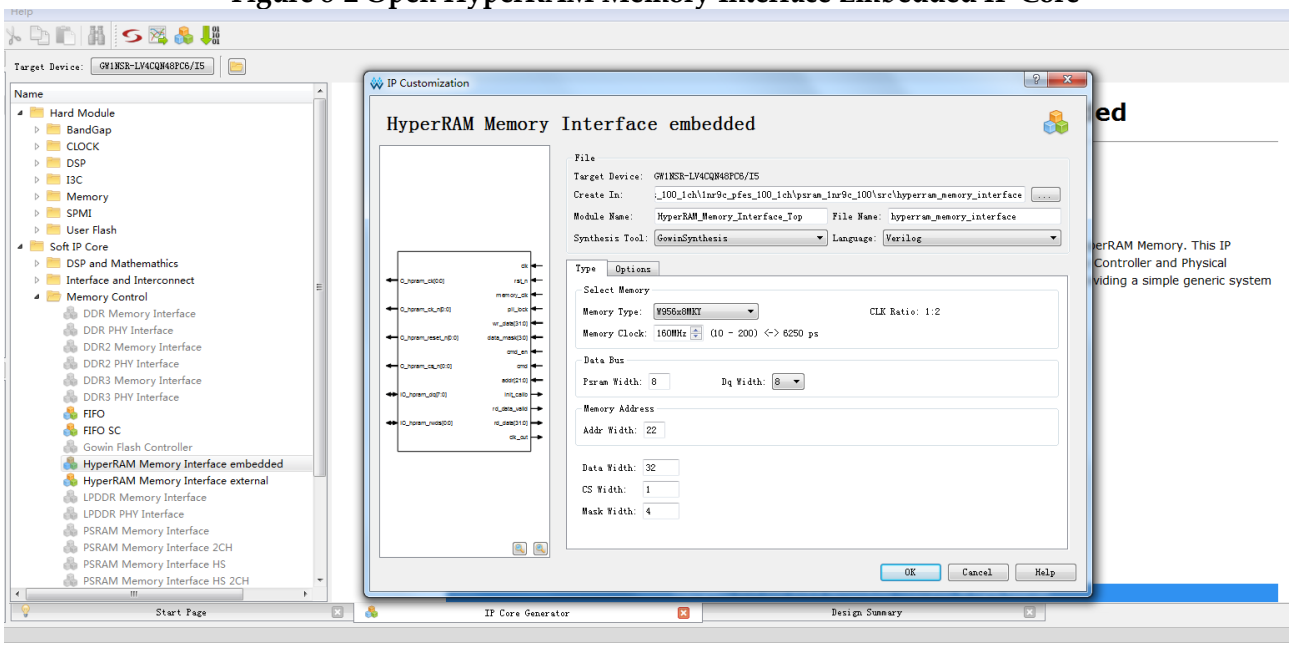
Figure 8-1 Open IP Core Generator



2. Open HyperRAM Memory Interface Embedded IP Core

Click the Memory Control option, double-click HyperRAM Memory Interface embedded.
HyperRAM Memory Interface embedded IP core opens, as shown in Figure 8-2.

Figure 8-2 Open HyperRAM Memory Interface Embedded IP Core

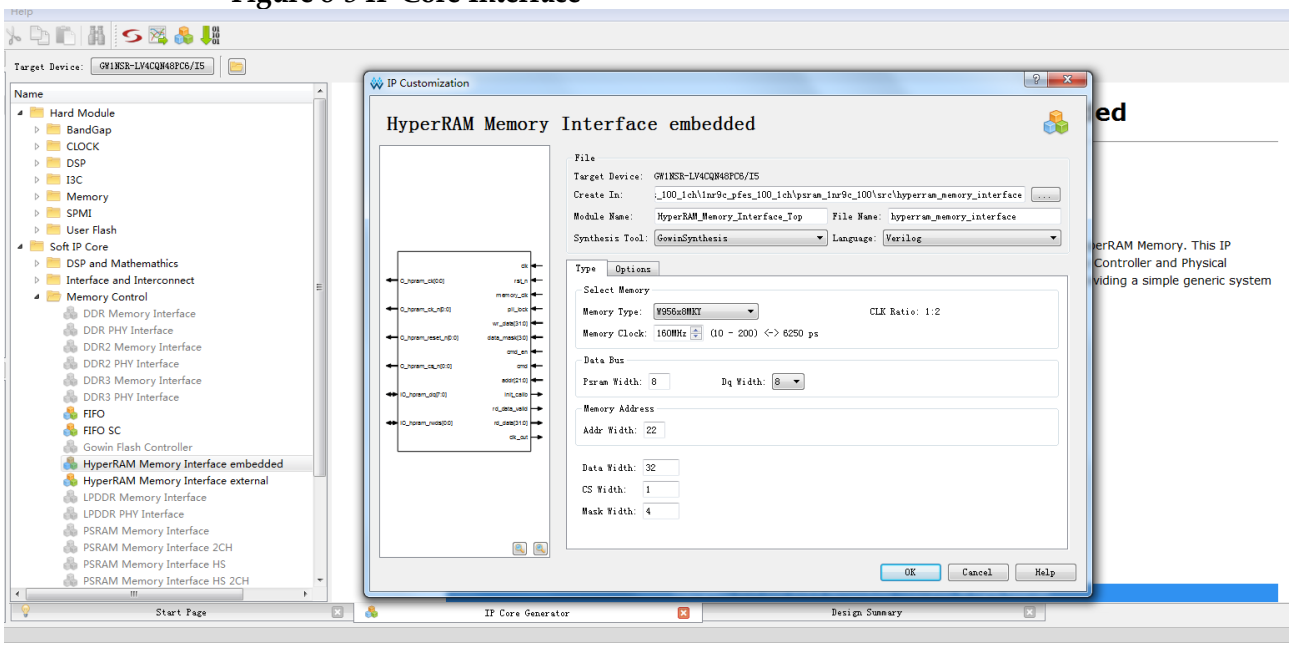


3. HyperRAM Memory Interface Embedded IP Core Port Interface

The Interface view of the HyperRAM Memory Interface embedded IP core is on the left, as shown in Figure 8-3.

The right side of the interface view is the interfaces between the HyperRAM Memory Controller and the user port. You can send/receive the commands and data through connecting your design to the Memory Interface IP. The left side of the interface view is the interface between the physical interface (PHY) and the memory. You can access and storage the data through connecting the HyperRAM Memory Interface embedded IP core to your required memory granule. With different configuration information, the signal bit-width and the signal number will change accordingly.

Figure 8-3 IP Core Interface



4. Open the Help file

You can click the Help button in the lower left of to check the English brief introduction of each option. The introduction order in the Help file and the order shown on the “IP Customization” are consistent, as shown in Figure 8-4.

Figure 8-4 Help File

HyperRAM Memory Interface embedded

Information

Type:	HyperRAM Memory Interface embedded
Vendor:	GOWIN Semiconductor
Summary:	The Gowin HyperRAM Memory Interface IP provides a complete solution for customers to use HyperRAM Memory. This IP located between the HyperRAM Memory and the user logic include with Gowin HyperRAM Memory Controller and Physical interface, reduces the user's effort to deal with the HyperRAM Memory command interface by providing a simple generic system interface to the user.

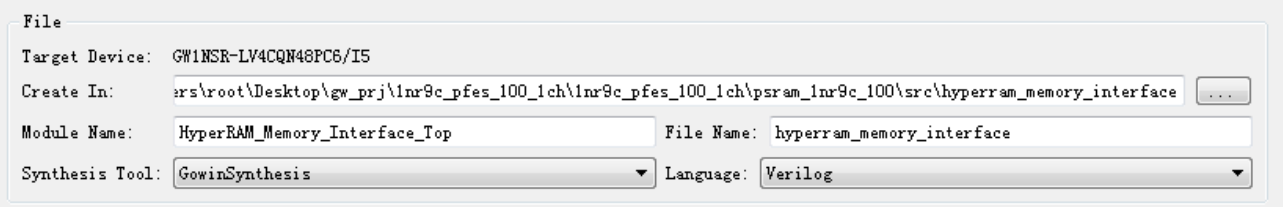
Options

Option	Description
Type	
Memory Type	Choose the type of HyperRAM Memory which consumer use.
CLK Ratio	This is the Memory Controller clock to HyperRAM Memory clock ratio.
Memory Clock	The consumer desire HyperRAM Memory working frequency.
Dq Width	This is the memory DQ bus width.
Psram Width	Only support 8 bit width.
Addr Width	This is the memory address bus width.
Data Width	It is equal to 4*Dq.
CS Width	It is equal to Dq Width/Psram Width.
Mask Width	It is equal to Data Width/Psram Width.
Burst Mode	This is the memory data burst length.
Burst Num	It is equal to Burst Mode/4 for cache write data.
Fixed Latency Enable	Control flag for fixed or unfixed latency.
Initial Latency	This is the basic latency from command to data.
Drive Strength	The x8 IO PSRAM support nominal impedance of 35, 50, 100 and 200 Ohms at VCC/2.
Deep Power Down	Deep power-down (DPD) operation disables all refresh-related activity.
Hybrid Sleep Mode	It will significantly decrease internal power consumption when staying at Hybrid Sleep Mode.
Refresh Rate	Refresh normal or faster.
PASR	Partial array self refresh.
Clk Type	Single clk or Diff clk.

5. Configure the Basic Information

See the basic information in the upper part of the configuration interface. Take the GW1NSR-4C chip as an example, and select the “QN88P” package. The “Module Name” option is the top-level file name of the generated project, and the default value is "HyperRam_Memory_Interface_Top". It can be modified. The "File Name" option is the folder used for saving the files required by the HyperRAM Memory Interface embedded IP core, and the default value is "hyperram_memory_interface". It can be modified. The “Create In” option is the the IP core files path, and the default is "…\src\hperram_memory_interface" under the project path. It can be modified. The "Add to Current Project" option in the lower right is used to ask whether directly added the generated IP to your project. The default is ticked, as shown in Figure 8-5.

Figure 8-5 Basic Information Configuration Interface



6. Type Options

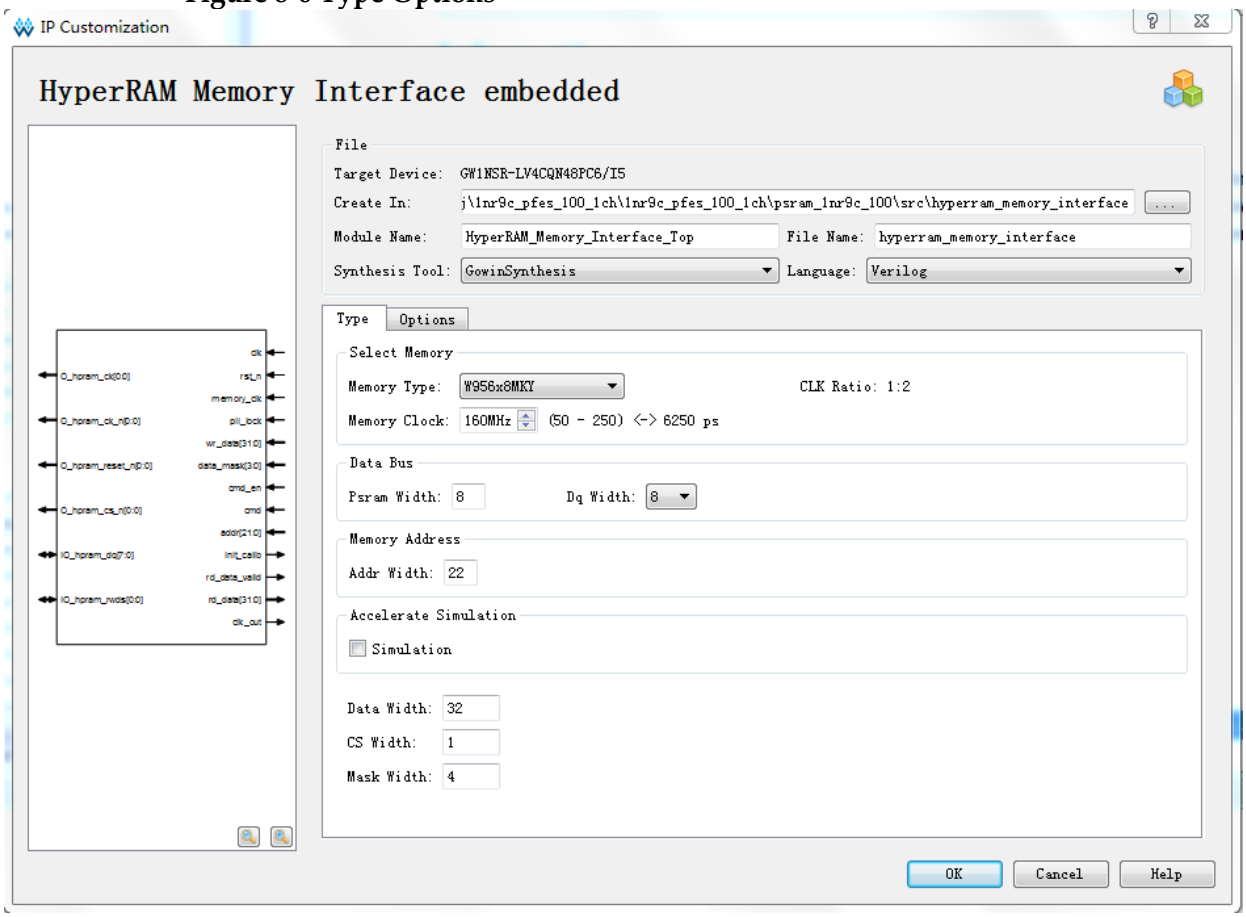
In the Type Options, you need to configure the basic information for the HyperRAM memory chip.

- Select Memory
- Data Bus
- Memory Address

In “Memory Address”, you can fill in the Address information of HyperRAM. You need to know the address width of the used; and the data equals to the ROW + Upper Column + Lower Column. After choosing the HyperRAM type, the software will be fill in the data automatically; if you choose “Custom”, you need to fill in the data according to your used HyperRAM memory type;

- Accelerrate Simulation
  This option is used to speed up user emulation and can be checked for user emulation, but unchecked for board-level testing and to regenerate the IP.
- Nonoperable

Figure 8-6 Type Options

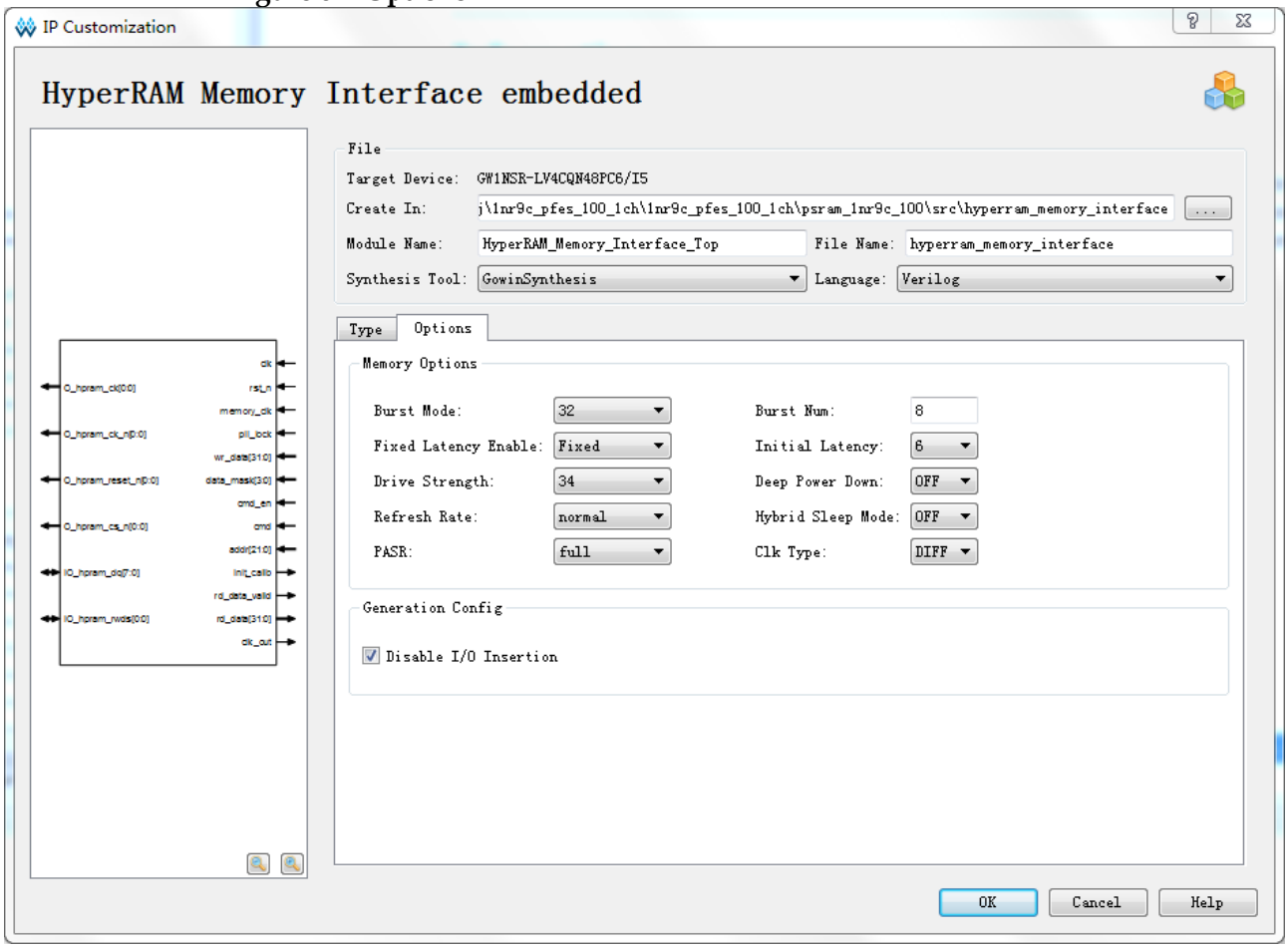


7. Options
   - Memory
   - Generation Config

In the IP generated after being checked, IBUF, OBUF and the other primitives are not inserted, and the logic is directly connected using the port, the default is checked by default.

Options is shown in Figure 8-7, and take “winbond W956x8MKY HyperRAM” as an example.

Figure 8-7 Options



9 File Delivery

The delivery files for the Gowin HyperRAM Memory Interface IP include the documents, the design source code, and the reference design.

9.1 Documents

The document folder mainly contains PDF file of the user guide.

Table 9-1 Documents List

Name	Description
IPUG944, Gowin HyperRAM Memory Interface IP User Guide	Gowin HyperRAM Memory Interface IP User Manual (this manual).
RN944, Gowin HyperRAM Memory Interface IP Release Note	_

9.2 Design Source Code (Encryption)

The Encryption Code Folder contains the RTL encryption code of Gowin HyperRAM Memory Interface IP used for the GUI, to generate the IP cores as needed.

Table 9-2 Design Source Code List

Name	Description
HPRAM_TOP.v	The top-level file of the IP core, which provides you with interface information, unencrypted.
Gowin HyperRAM Memory Interface partial code	
hpram_code.v	Gowin HyperRAM Memory Interface IP Design RTL Source File, encrypted
hpram_define.v	Gowin HyperRAM memory controller parameter definition module that you generated via GUI configuration, unencrypted.
hpram_local_define.v	Gowin HyperRAM memory controller parameter definition processing module, encrypted.
hpram_param.v	Gowin HyperRAM memory controller parameter configuration module that you generated via GUI configuration, unencrypted.
hpram_local_param.v	Gowin HyperRAM memory controller parameter processing module, which disposes the parameters passed from the GUI, encrypted.

9.3 Reference Design

The Ref. Design folder contains the netlist file for Gowin HyperRAM Memory Interface IP, the user reference design, the constraint file, the jitter elimination module, the top file, the project file folder, etc.

Table 9-3 Ref. Design Folder Contents

Name	Description
hpram_syn_top.v	The top module of reference design
key_debounce.v	Key jitter elimination module
hpram_test.v	Test stimulus generation module
HyperRam _Memory_Interface.vo	Gowin HyperRAM Memory Interface IP netlist file
hpram.cst	HyperRAM project physical constraints file
hpram.sdc	HyperRAM project timing constraints file
hpram.gao	Capture HyperRAM data
HyperRam _Memory_Interface	HyperRAM IP project file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